LMF100 Dual High-Performance Switched Capacitor Filters

Not Recommended for New Designs

1 Features

- Wide 4-V to 15-V Power Supply Range
- Operation up to 100 kHz
- Low Offset Voltage:
  - Typically (50:1 or 100:1 mode):
    - Vos1 = ±5 mV
    - Vos2 = ±15 mV
    - Vos3 = ±15 mV
- Low Crosstalk: –60 dB
- Clock to Center Frequency Ratio Accuracy ±0.2% (Typical)
- $f_0 \times Q$ Range up to 1.8 MHz
- Pin-Compatible With MF10

2 Applications

- Replacing Active RC Filters With Reduced Form Factors and Higher Accuracy and Tunability
- An Alternative to Integrated Continuous Time Filters

3 Description

The LMF100 device consists of two independent general-purpose, high-performance switched capacitor filters. With an external clock and two to four resistors, each filter block can realize various second-order and first-order filtering functions. Each block has three outputs. One output can be configured to perform either an allpass, highpass, or notch function. The other two outputs perform bandpass and lowpass functions. The center frequency of each filter stage is tuned by using an external clock or a combination of a clock and resistor ratio. Up to a fourth-order biquadratic function can be realized with one LMF100. Higher order filters are implemented by simply cascading additional packages, and all the classical filters (such as Butterworth, Bessel, Elliptic, and Chebyshev) can be realized.

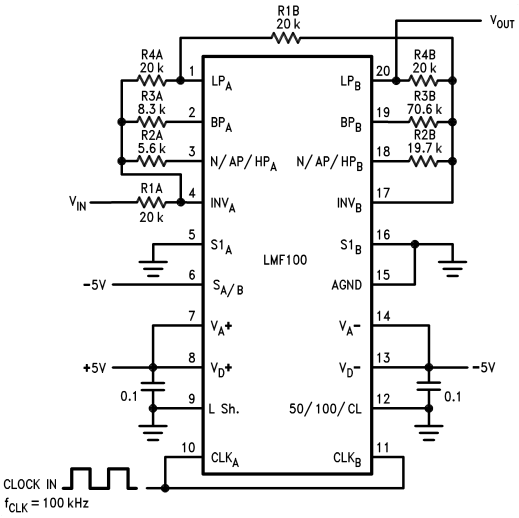
The LMF100 is fabricated on TI's high-performance analog silicon gate CMOS process, LMCMOS™. This allows for the production of a very low-offset, high-frequency filter building block. The LMF100 is pin-compatible with the industry standard MF10, but provides greatly improved performance.

Device Information(1)

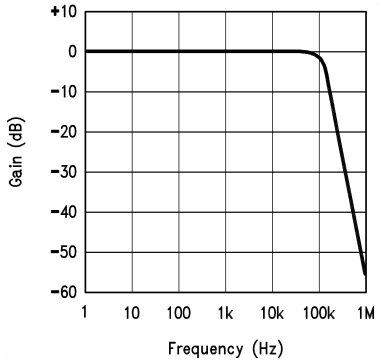
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMF100	SOIC (20)	12.60 mm × 10.00 mm
	PDIP (20)	24.33 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Fourth-Order 100-kHz Butterworth Lowpass Filter



Transfer Curve of Butterworth LP Filter Roll-Off Magnitude vs Frequency



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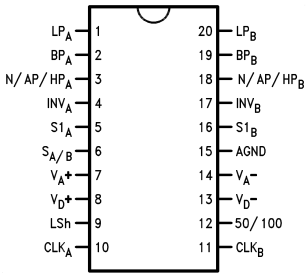
4 Revision History

Changes from Revision A (July 1999) to Revision B **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

5 Pin Configuration and Functions

DW and N Package
20-Pin SOIC and PDIP (N20 or M20B)
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
LP	1	I/O	The second order lowpass, bandpass and notch, allpass and highpass outputs. These outputs can typically swing to within 1 V of each supply when driving a 5-kΩ load. For optimum performance, capacitive loading on these outputs should be minimized. For signal frequencies above 15 kHz, the capacitance loading should be kept below 30 pF.
	20		
BP	2		
	19		
N/AP/HP	3		
	18		
INV	4	I	The inverting input of the summing op-amp of each filter. These are high impedance inputs. The noninverting input is internally tied to AGND so the opamp can be used only as an inverting amplifier.
	17		
S1	5	I	S1 is a signal input pin used in modes 1b, 4, and 5. The input impedance is $1/f_{CLK}$ x 1 pF. The pin should be driven with a source impedance of less than 1 kΩ. If S1 is not driven with a signal it should be tied to AGND (mid-supply).
	16		
$S_{A/B}$	6	I	This pin activates a switch that connects one of the inputs of each filter's second summer either to AGND ($S_{A/B}$ tied to V^-) or to the lowpass (LP) output ($S_{A/B}$ tied to V^+). This offers the flexibility needed for configuring the filter in its various modes of operation.
V_A^+	7 (1)	I	This is both the analog and digital positive supply.
V_D^+	8 (1)	I	Analog and digital negative supplies. V_A^- and V_D^- should be derived from the same source. They have been brought out separately so they can be bypassed by separate capacitors, if desired. They can also be tied together externally and bypassed with a single capacitor.
V_A^-	14	I	Analog and digital negative supplies. V_A^- and V_D^- should be derived from the same source. They have been brought out separately so they can be bypassed by separate capacitors, if desired. They can also be tied together externally and bypassed with a single capacitor.
V_D^-	13		
LSh	9	I	Level shift pin. This is used to accommodate various clock levels with dual or single supply operation. With dual ±5-V supplies and CMOS (±5 V) or TTL (0 V–5 V) clock levels, LSh should be tied to system ground. For 0-V to 10-V single-supply operation the AGND pin should be biased at +5 V and the LSh pin should be tied to the system ground for TTL clock levels. LSh should be biased at +5 V for ±5-V CMOS clock levels. The LSh pin is tied to system ground for ±2.5V operation. For single 5V operation the LSh and V_D^+ pins are tied to system ground for TTL clock levels.
CLK	10	I	Clock inputs for the two switched capacitor filter sections. Unipolar or bipolar clock levels may be applied to the CLK inputs according to the programming voltage applied to the LSh pin. The duty cycle of the clock should be close to 50%, especially when clock frequencies above 200 kHz are used. This allows the maximum time for the internal opamps to settle, which yields optimum filter performance.
	11		
50/100	12 (1)	I	By tying this pin to V+ a 50:1 clock to filter center frequency ratio is obtained. Tying this pin at mid-supply (i.e., system ground with dual supplies) or to V^- allows the filter to operate at a 100:1 clock to center frequency ratio.
AGND	15	I	This is the analog ground pin. This pin should be connected to the system ground for dual supply operation or biased to mid-supply for single-supply operation. For a further discussion of mid-supply biasing techniques see the Applications Information (Section 3.2). For optimum filter performance a "clean" ground must be provided.

(1) This device is pin-for-pin compatible with the MF10 except for the following changes:
(a) Unlike the MF10, the LMF100 has a single positive supply pin (V_A^+).
(b) On the LMF100 V_D^+ is a control pin and is not the digital positive supply as on the MF10.
(c) Unlike the MF10, the LMF100 does not support the current limiting mode. When the 50/100 pin is tied to V^- the LMF100 will remain in the 100:1 mode.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply Voltage ($V^+ - V^-$)				16	V
Voltage at any pin				$V^+ + 0.3$	V
				$V^- - 0.3$	
Input current at any pin(2)				5	mA
Package input current(2)				20	mA
Power dissipation(3)				500	mW
Soldering information(4)	N Package: 10 sec.			250	°C
	SOIC Package	Vapor Phase (60 sec)		215	
		Infrared (15 sec)		220	
Storage temperature, T_{stg}				150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or the absolute value of current at that pin should be limited to 5 mA or less. The sum of the currents at all pins that are driven beyond the power supply voltages should not exceed 20 mA.V_{IN}^+)
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/R_{\theta JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance of the LMF100CIN when board mounted is 55°C/W. For the LMF100CIWM this number is 66°C/W.
(4) See AN-450*Surface Mounting Methods and Their Effect on Product Reliability*(Appendix D) for other methods of soldering surface mount devices.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) A military RETS specification is available upon request.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Temperature	LMF100CCN	0		70	°C
	LMF100CIWM	–40		85	
Supply voltage		4	≤$V^+ - V^-$≤	15	V

6.4 Thermal Information

THERMAL METRIC[1]		LMF100		UNIT
		DW (SOIC)	N (PDIP)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.8	49.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.2	41.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.8	30.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.7	18.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.3	30.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics for $V^+ = +5$ V and $V^- = -5$ V

The following specifications apply for Mode 1, Q = 10 ($R_1 = R_3 = 100$ k, $R_2 = 10$ k), $V^+ = +5$ V and $V^- = -5$ V unless otherwise specified. All limits are $T_A = T_J = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS			LMF100CCN			LMF100CIWM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_s	Maximum supply current	f_{CLK} = 250 kHz, No Input Signal				9			9		mA
			Tested Limit[1]				13				
				T_{MIN} to T_{MAX}						13	
			Design Limit[2]	T_{MIN} to T_{MAX}			13				
f_0	Center frequency				0.1		100000	0.1		100000	Hz
f_{CLK}	Clock frequency				5		3500000	5		3500000	Hz
f_{CLK}/f_0	Clock to center frequency ratio deviation	V_{Pin12} = 5 V or 0 V, f_{CLK} = 1 MHz				±0.2%			±0.2%		
			Tested Limit[1]				±0.8%				
				T_{MIN} to T_{MAX}						±0.8%	
			Design Limit[2]	T_{MIN} to T_{MAX}			±0.8%				
$\frac{\Delta Q}{Q}$	Q Error (MAX) [3]	Q = 10, Mode 1, V_{Pin12} = 5 V or 0 V, f_{CLK} = 1 MHz				±0.5%			±0.5%		
			Tested Limit[1]				±5%				
				T_{MIN} to T_{MAX}						±6%	
			Design Limit[2]	T_{MIN} to T_{MAX}			±6%				
H_{OBP}	Bandpass gain at f_0	f_{CLK} = 1 MHz				0			0		dB
			Tested Limit[1]				±0.4				
				T_{MIN} to T_{MAX}						±0.4	
			Design Limit[2]	T_{MIN} to T_{MAX}			±0.4				
H_{OLP}	DC Lowpass gain	$R_1 = R_2 = 10$ k, f_{CLK} = 250 kHz				0			0		dB
			Tested Limit[1]				±0.2				
				T_{MIN} to T_{MAX}						±0.2	
			Design Limit[2]	T_{MIN} to T_{MAX}			±0.2				
V_{OS1}	DC Offset voltage[4]	f_{CLK} = 250 kHz				±5			±5		mV
			Tested Limit[1]				±15				
				T_{MIN} to T_{MAX}						±15	
			Design Limit[2]	T_{MIN} to T_{MAX}			±15				

(1) Tested limits are specified to Texas Instruments AOQL (Average Outgoing Quality Level).
(2) Design limits are specified to Texas Instruments AOQL (Average Outgoing Quality Level) but are not 100% tested.
(3) The accuracy of the Q value is a function of the center frequency (f_0). This is illustrated in the curves under the heading *Typical Characteristics*.
(4) V_{os1}, V_{os2}, and V_{os3} refer to the internal offsets as discussed in *Application Information*.

Electrical Characteristics for V^+ = +5 V and V^- = −5 V (continued)

The following specifications apply for Mode 1, Q = 10 (R_1 = R_3 = 100 k, R_2 = 10 k), V^+ = +5 V and V^- = −5 V unless otherwise specified. All limits are T_A = T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS				LMF100CCN			LMF100CIWM			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS2}	DC Offset voltage(4)	f_{CLK} = 250 kHz	$S_{A/B}$ = V^+				±30			±30		mV
				Tested Limit(1)				±80				
					T_{MIN} to T_{MAX}						±80	
				Design Limit(2)	T_{MIN} to T_{MAX}			±80				
			$S_{A/B}$ = V^-				±15			±15		mV
				Tested Limit(1)				±70				
					T_{MIN} to T_{MAX}						±70	
				Design Limit(2)	T_{MIN} to T_{MAX}			±70				
V_{OS3}	DC Offset voltage(4)	f_{CLK} = 250 kHz					±15			±15		mV
			Tested Limit(1)					±40				
				T_{MIN} to T_{MAX}							±60	
			Design Limit(2)	T_{MIN} to T_{MAX}				±60				
	Crosstalk(5)	A Side to B Side or B Side to A Side					–60			–60		dB
	Output noise(6)	f_{CLK} = 250 kHz	N				40			40		μV
		20 kHz Bandwidth	BP				320			320		
		100:1 Mode	LP				300			300		
	Clock feedthrough(7)	f_{CLK} = 250 kHz 100:1 Mode					6			6		mV
V_{OUT}	Minimum output voltage swing	R_L = 5 k (All Outputs)					4 −4.7			4 −4.7		V
			Tested Limit(1)					±3.8				
				T_{MIN} to T_{MAX}							±3.7	
			Design Limit(2)	T_{MIN} to T_{MAX}				±3.7				
		R_L = 3.5 k (All Outputs)					3.9 −4.6			3.9 −4.6		
GBW	Operational amplifier gain BW product						5			5		MHz
SR	Operational amplifier slew rate						20			20		V/μs
I_{sc}	Maximum output, Short circuit current(8)	Source	All Outputs				12			12		mA
		Sink	All Outputs				45			45		mA
I_{IN}	Input current on Pins: 4, 5, 6, 9, 10, 11, 12, 16, 17	Tested Limit(1)						10				μA
		Design Limit(2)	T_{MIN} to T_{MAX}								10	

(5) Crosstalk between the internal filter sections is measured by applying a 1 V_{RMS} 10-kHz signal to one bandpass filter section input and grounding the input of the other bandpass filter section. The crosstalk is the ratio between the output of the grounded filter section and the 1 V_{RMS} input signal of the other section.
(6) In 50:1 mode the output noise is 3 dB higher.
(7) In 50:1 mode the clock feed through is 6 dB higher.
(8) The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst case conditions.

6.6 Electrical Characteristics for V^+ = +2.5 V and V^- = −2.5 V

The following specifications apply for Mode 1, Q = 10 (R_1 = R_3 = 100 k, R_2 = 10 k), V^+ = +2.50 V and V^- = −2.50 V unless otherwise specified. All limits are T_A = T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS			LMF100CCN			LMF100CIWM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_s	Maximum supply current	f_{CLK} = 250 kHz, No Input Signal				8			8		mA
			Tested Limit(1)				12			12	
				T_{MIN} to T_{MAX}							
			Design Limit(2)			12					
f_0	Center frequency				0.1		50000	0.1		50000	Hz

(1) Tested limits are specified to Texas Instruments AOQL (Average Outgoing Quality Level).
(2) Design limits are specified to Texas Instruments AOQL (Average Outgoing Quality Level) but are not 100% tested.

Electrical Characteristics for V^+ = +2.5 V and V^- = −2.5 V (continued)

The following specifications apply for Mode 1, Q = 10 ($R_1 = R_3$ = 100 k, R_2 = 10 k), V^+ = +2.50 V and V^- = −2.50 V unless otherwise specified. All limits are $T_A = T_J$ = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS			LMF100CCN			LMF100CIWM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
f_{CLK}	Clock frequency				5		1500000	5		1500000	Hz
f_{CLK}/f_0	Clock to center frequency ratio deviation	V_{Pin12} = 5 V or 0 V, f_{CLK} = 1 MHz				±0.2%			±0.2%		
			Tested Limit(1)	T_{MIN} to T_{MAX}			±1%			±1%	
			Design Limit(2)				±1%				
$\frac{\Delta Q}{Q}$	Q Error (MAX) (3)	Q = 10, Mode 1, V_{Pin12} = 5 V or 0 V, f_{CLK} = 1 MHz				±0.5%			±0.5%		
			Tested Limit(1)				±5%				
				T_{MIN} to T_{MAX}						±8%	
			Design Limit(2)	T_{MIN} to T_{MAX}			±8%				
H_{OBP}	Bandpass gain at f_0	f_{CLK} = 1 MHz				0			0		dB
			Tested Limit(1)				±0.4				
				T_{MIN} to T_{MAX}						±0.5	
			Design Limit(2)	T_{MIN} to T_{MAX}			±0.5				
H_{OLP}	DC Lowpass gain	$R_1 = R_2$ = 10 k, f_{CLK} = 250 kHz				0			0		dB
			Tested Limit(1)				±0.2				
				T_{MIN} to T_{MAX}						±0.2	
			Design Limit(2)	T_{MIN} to T_{MAX}			±0.2				
V_{OS1}	DC Offset voltage(4)	f_{CLK} = 250 kHz				±5			±5		mV
			Tested Limit(1)				±15			±15	
				T_{MIN} to T_{MAX}							
			Design Limit(2)	T_{MIN} to T_{MAX}			±15				
V_{OS2}	DC Offset voltage(4)	f_{CLK} = 250 kHz	$S_{A/B} = V^+$			±20			±20		mV
				Tested Limit(1)			±60				
					T_{MIN} to T_{MAX}					±60	
				Design Limit(2)	T_{MIN} to T_{MAX}		±60				
			$S_{A/B} = V^-$			±10			±10		mV
				Tested Limit(1)			±50				
					T_{MIN} to T_{MAX}					±60	
				Design Limit(2)	T_{MIN} to T_{MAX}		±60				
V_{OS3}	DC Offset voltage(4)	f_{CLK} = 250 kHz				±10			±10		mV
			Tested Limit(1)				±25				
				T_{MIN} to T_{MAX}						±30	
			Design Limit(2)	T_{MIN} to T_{MAX}			±30				
	Crosstalk(5)	A Side to B Side or B Side to A Side				–65			–65		dB
	Output noise(6)	f_{CLK} = 250 kHz	N			25			25		μV
		20 kHz Bandwidth	BP			250			250		
		100:1 Mode	LP			220			220		
	Clock feedthrough(7)	f_{CLK} = 250 kHz 100:1 Mode				2			2		mV

(3) The accuracy of the Q value is a function of the center frequency (f_0). This is illustrated in the curves under the heading *Typical Characteristics*.
(4) V_{OS1}, V_{OS2}, and V_{OS3} refer to the internal offsets as discussed in the *Application Information*.
(5) Crosstalk between the internal filter sections is measured by applying a 1 V_{RMS} 10-kHz signal to one bandpass filter section input and grounding the input of the other bandpass filter section. The crosstalk is the ratio between the output of the grounded filter section and the 1 V_{RMS} input signal of the other section.
(6) In 50:1 mode the output noise is 3 dB higher.
(7) In 50:1 mode the clock feed through is 6 dB higher.

Electrical Characteristics for V^+ = +2.5 V and V^- = −2.5 V (continued)

The following specifications apply for Mode 1, Q = 10 (R_1 = R_3 = 100 k, R_2 = 10 k), V^+ = +2.50 V and V^- = −2.50 V unless otherwise specified. All limits are T_A = T_J = 25°C unless otherwise specified.

PARAMETER			TEST CONDITIONS			LMF100CCN			LMF100CIWM			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
V_{OUT}	Minimum output voltage swing		R_L = 5 k All Outputs				1.6 −2.2			1.6 −2.2		V
			R_L = 5 k (All Outputs)	Tested Limit(1)				±1.5				
					T_{MIN} to T_{MAX}						±1.4	
				Design Limit(2)	T_{MIN} to T_{MAX}			±1.4				
			R_L = 3.5 k All Outputs				1.5 −2.1			1.5 −2.1		V
GBW	Operational amplifier gain BW product						5			5		MHz
SR	Operational amplifier slew rate						18			18		V/µs
I_{sc}	Maximum output, Short circuit current(8)	Source	All Outputs				10			10		mA
		Sink	All Outputs				20			20		mA

(8) The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst case conditions.

6.7 Logic Input Characteristics

All limits apply to T_A = T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS			LMF100CCN			LMF100CIWM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
CMOS Clock Input Voltage	MIN Logical “1”	V^+ = +5 V, V^- = −5 V,	Tested Limit(1)				3				V
				T_{MIN} to T_{MAX}						3	
			Design Limit(2)	T_{MIN} to T_{MAX}			3				
	MAX Logical “0”	V_{LSh} = 0 V	Tested Limit(1)				−3				V
				T_{MIN} to T_{MAX}						–3	
			Design Limit(2)	T_{MIN} to T_{MAX}			−3				
	MIN Logical “1”	V^+ = +10 V, V^- = 0 V,	Tested Limit(1)				8				V
				T_{MIN} to T_{MAX}						8	
			Design Limit(2)	T_{MIN} to T_{MAX}			8				
	MAX Logical “0”	V_{LSh} = +5 V	Tested Limit(1)				2				V
				T_{MIN} to T_{MAX}						2	
			Design Limit(2)	T_{MIN} to T_{MAX}			2				
TTL Clock Input Voltage	MIN Logical “1”	V^+ = +5 V, V^- = −5 V,	Tested Limit(1)				2				V
				T_{MIN} to T_{MAX}						2	
			Design Limit(2)	T_{MIN} to T_{MAX}			2				
	MAX Logical “0”	V_{LSh} = 0 V	Tested Limit(1)				0.8				V
				T_{MIN} to T_{MAX}						0.8	
			Design Limit(2)	T_{MIN} to T_{MAX}			0.8				
	MIN Logical “1”	V^+ = +10 V, V^- = 0 V,	Tested Limit(1)				2				V
				T_{MIN} to T_{MAX}						2	
			Design Limit(2)	T_{MIN} to T_{MAX}			2				
	MAX Logical “0”	V_{LSh} = 0 V	Tested Limit(1)				0.8				V
				T_{MIN} to T_{MAX}						0.8	
			Design Limit(2)	T_{MIN} to T_{MAX}			0.8				

(1) Tested limits are specified to Texas Instruments AOQL (Average Outgoing Quality Level).
(2) Design limits are specified to Texas Instruments AOQL (Average Outgoing Quality Level) but are not 100% tested.

Logic Input Characteristics (continued)

All limits apply to $T_A = T_J = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS			LMF100CCN			LMF100CIWM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
CMOS Clock Input Voltage	MIN Logical “1”	$V^+ = +2.5$ V, $V^- = -2.5$ V,	Tested Limit(1)				1.5				V
				T_{MIN} to T_{MAX}						1.5	
			Design Limit(2)	T_{MIN} to T_{MAX}			1.5				
	MAX Logical “0”	$V_{LSh} = 0$ V	Tested Limit(1)				−1.5				V
				T_{MIN} to T_{MAX}						−1.5	
			Design Limit(2)	T_{MIN} to T_{MAX}			−1.5				
	MIN Logical “1”	$V^+ = +5$ V, $V^- = 0$ V,	Tested Limit(1)				4				V
				T_{MIN} to T_{MAX}						4	
			Design Limit(2)	T_{MIN} to T_{MAX}			4				
	MAX Logical “0”	$V_{LSh} = +2.5$ V	Tested Limit(1)				1				V
				T_{MIN} to T_{MAX}						1	
			Design Limit(2)	T_{MIN} to T_{MAX}			1				
TTL Clock Input Voltage	MIN Logical “1”	$V^+ = +5$ V, $V^- = 0$ V,	Tested Limit(1)				2				V
				T_{MIN} to T_{MAX}						2	
			Design Limit(2)	T_{MIN} to T_{MAX}			2				
	MAX Logical “0”	$V_{LSh} = 0$ V, $V_D^+ = 0$ V	Tested Limit(1)				0.8				V
				T_{MIN} to T_{MAX}						0.8	
			Design Limit(2)	T_{MIN} to T_{MAX}			0.8				

6.8 Typical Characteristics

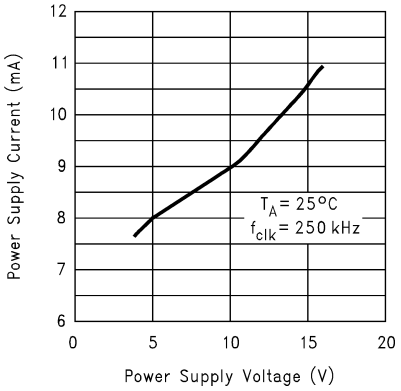


Figure 1. Power Supply Current vs Power Supply Voltage

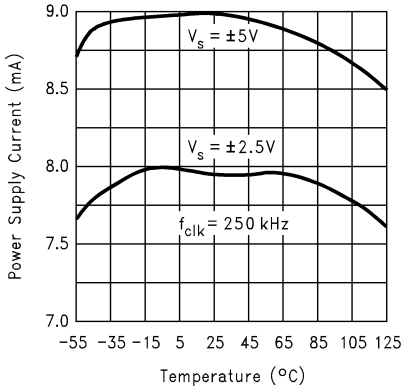


Figure 2. Power Supply Current vs Temperature

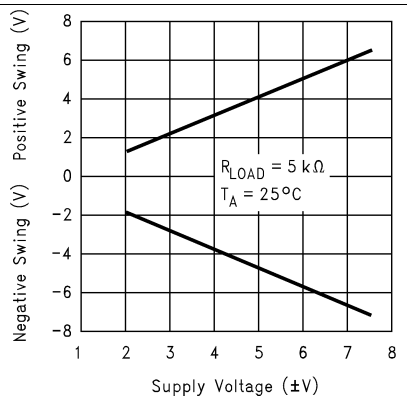


Figure 3. Output Swing vs Supply Voltage

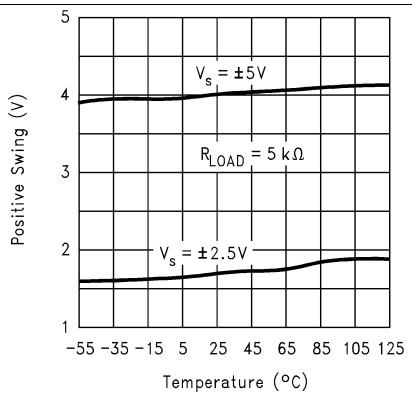


Figure 4. Positive Output Swing vs Temperature

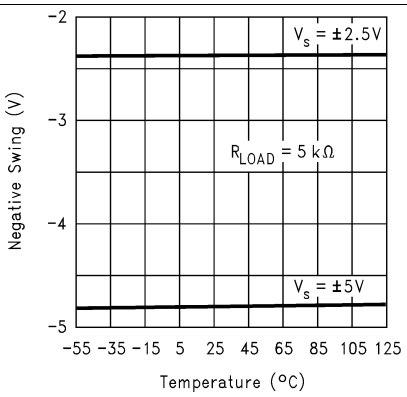


Figure 5. Negative Output Swing vs Temperature

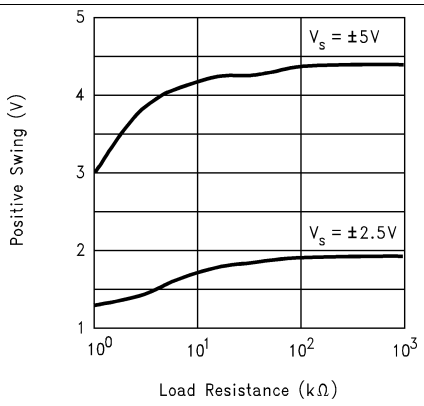


Figure 6. Positive Output Voltage Swing vs Load Resistance

Typical Characteristics (continued)

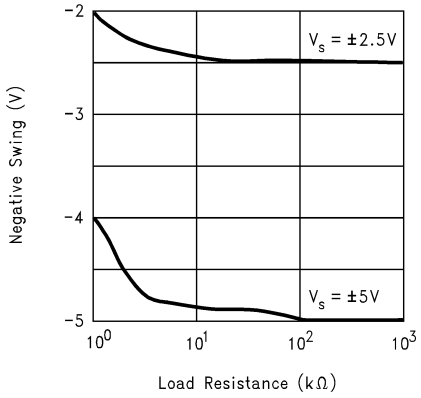


Figure 7. Negative Output Voltage Swing vs Load Resistance

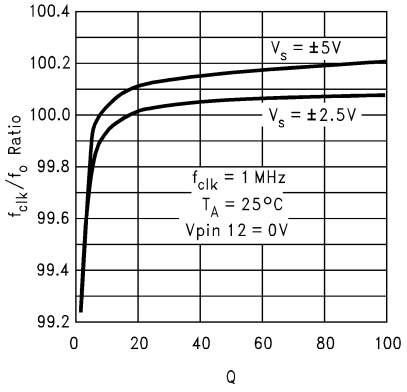


Figure 8. f_{CLK}/f_0 Ratio vs Q

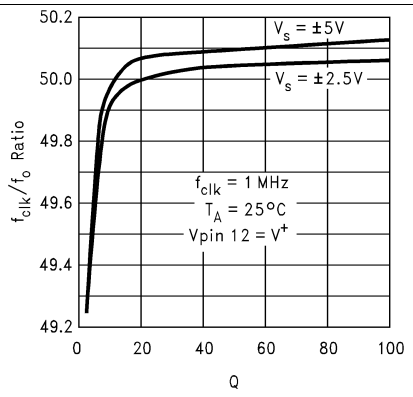


Figure 9. f_{CLK}/f_0 Ratio vs Q

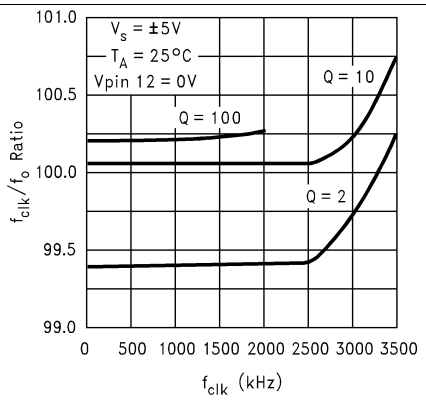


Figure 10. f_{CLK}/f_0 Ratio vs f_{CLK}

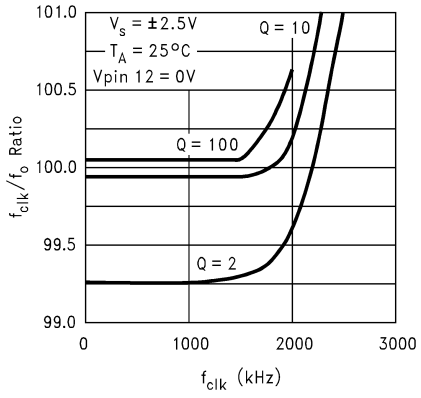


Figure 11. f_{CLK}/f_0 Ratio vs f_{CLK}

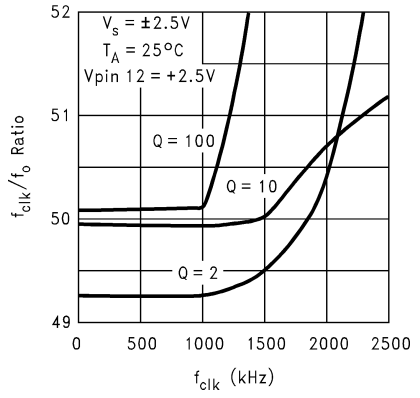


Figure 12. f_{CLK}/f_0 Ratio vs f_{CLK}

Typical Characteristics (continued)

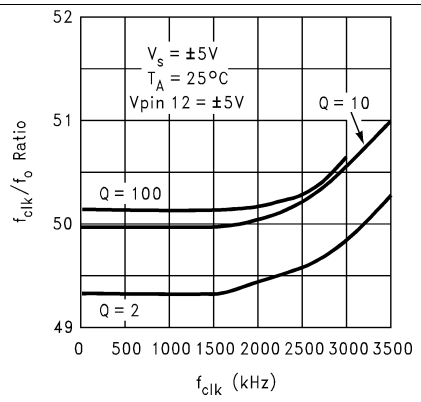


Figure 13. f_{CLK}/f_0 Ratio vs f_{CLK}

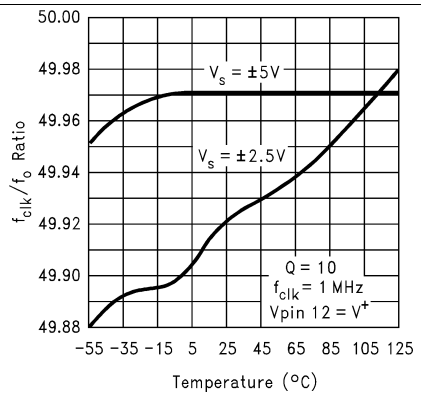


Figure 14. f_{CLK}/f_0 Ratio vs Temperature

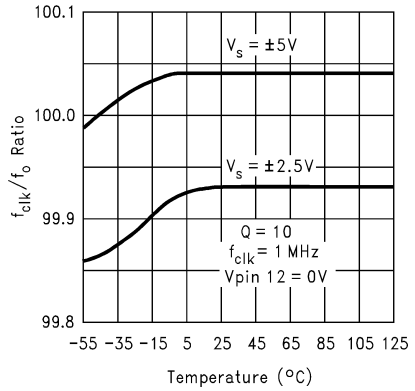


Figure 15. f_{CLK}/f_0 Ratio vs Temperature

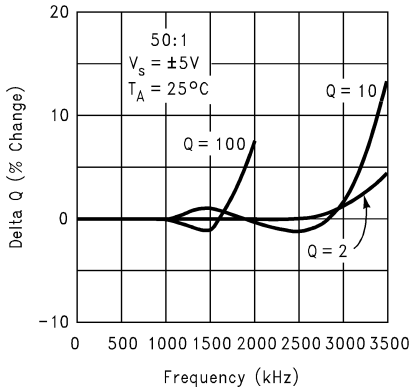


Figure 16. Q Deviation vs Clock Frequency

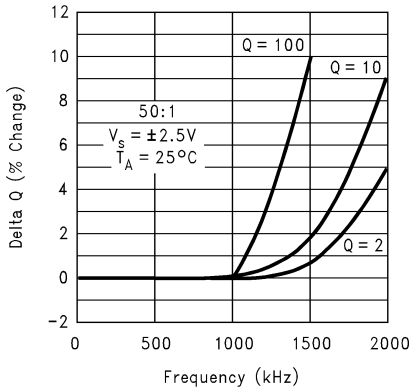


Figure 17. Q Deviation vs Clock Frequency

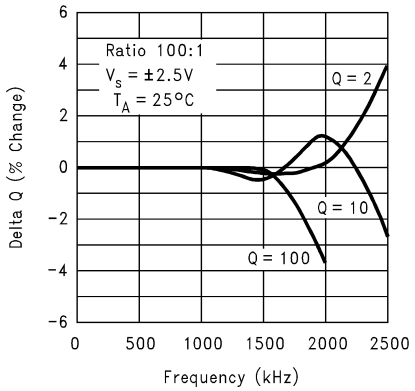


Figure 18. Q Deviation vs Clock Frequency

Typical Characteristics (continued)

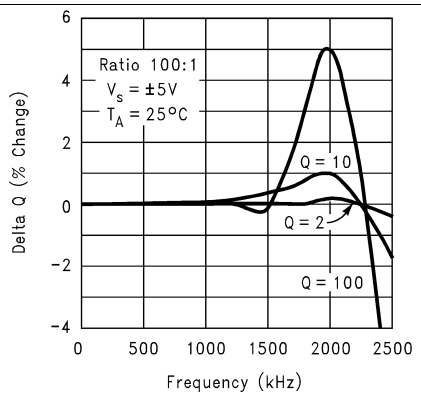


Figure 19. Q Deviation vs Clock Frequency

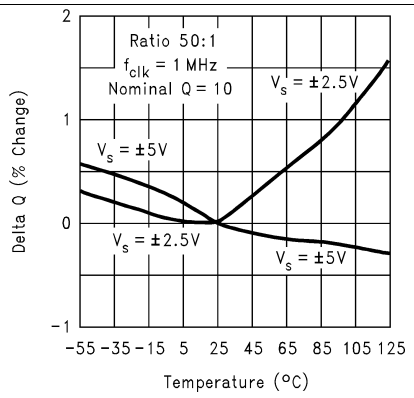


Figure 20. Q Deviation vs Temperature

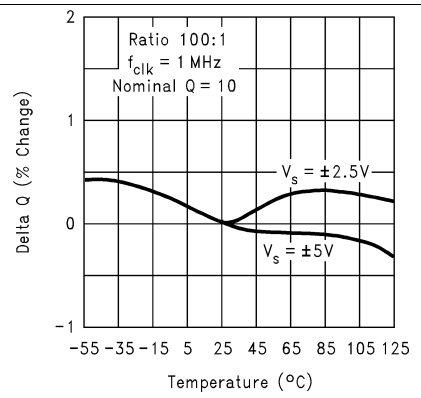


Figure 21. Q Deviation vs Temperature

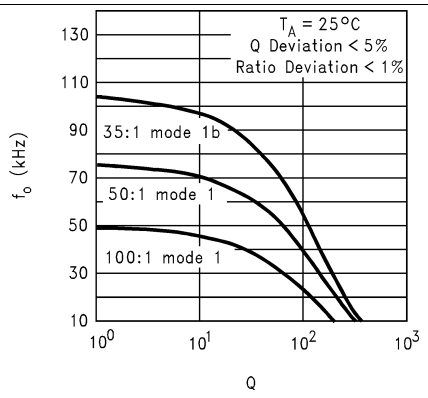


Figure 22. Maximum f_0 vs Q at V_S = ±7.5 V

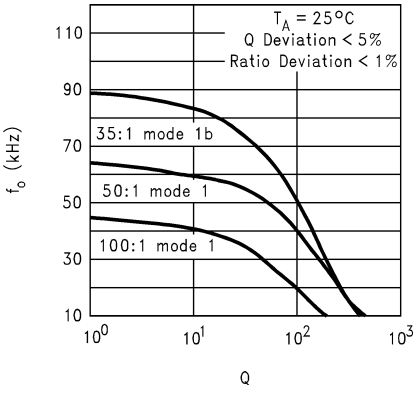


Figure 23. Maximum f_0 vs Q at V_S = ±5 V

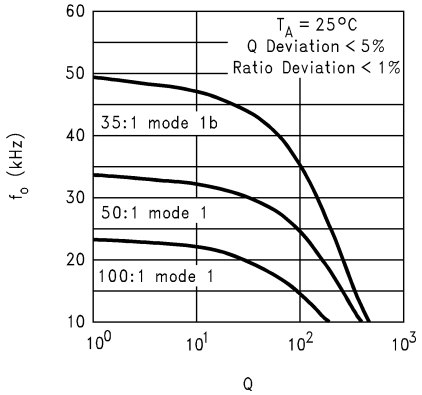


Figure 24. Maximum f_0 vs Q at V_S = ±2.5 V

7 Parameter Measurement Information

7.1 Definition of Terms Graphics

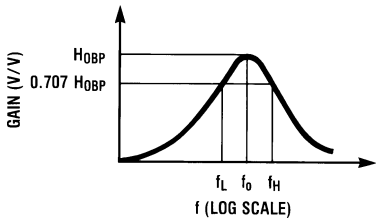


Figure 25. Second-Order Bandpass Response Gain

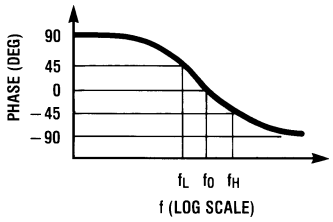


Figure 26. Second-Order Bandpass Response Phase

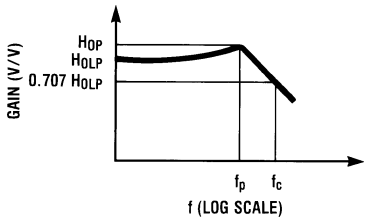


Figure 27. Second-Order Lowpass Response Gain

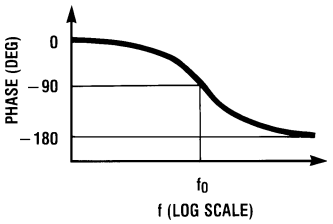


Figure 28. Second-Order Lowpass Response Phase

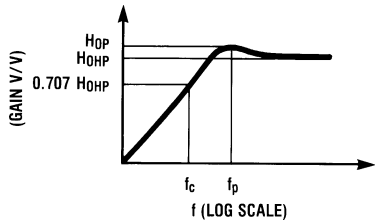


Figure 29. Second-Order Highpass Response Gain

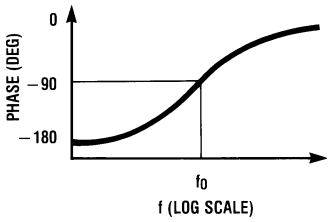


Figure 30. Second-Order Highpass Response Phase

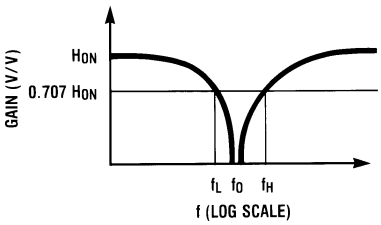


Figure 31. Second-Order Notch Response Gain

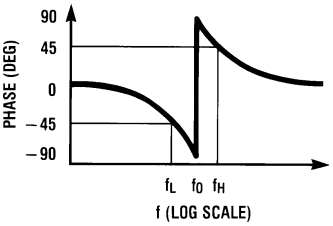


Figure 32. Second-Order Notch Response Phase

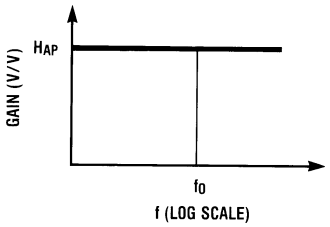


Figure 33. Second-Order Allpass Response Gain

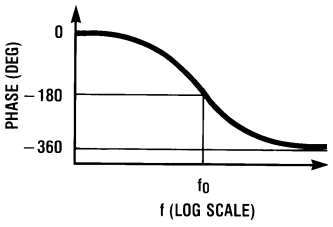


Figure 34. Second-Order Allpass Response Phase

Definition of Terms Graphics (continued)

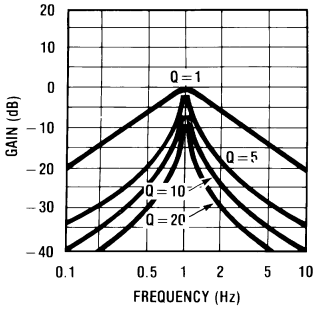


Figure 35. Bandpass Response of Various Second-Order Filters as a Function of Q. Gains and Center Frequencies are Normalized to Unity Gain

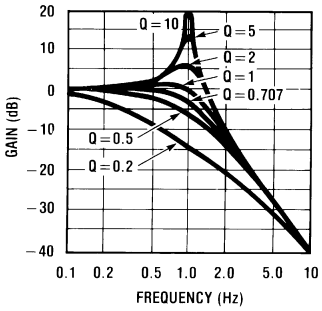


Figure 36. Lowpass Response of Various Second-Order Filters as a Function of Q. Gains and Center Frequencies are Normalized to Unity Phase

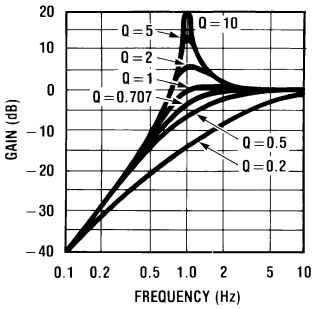


Figure 37. Highpass Response of Various Second-Order Filters as a Function of Q. Gains and Center Frequencies are Normalized to Unity Gain

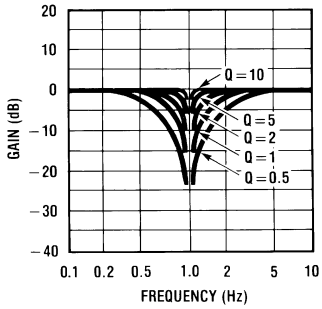


Figure 38. Notch Response of Various Second-Order Filters as a Function of Q. Gains and Center Frequencies are Normalized to Unity Gain

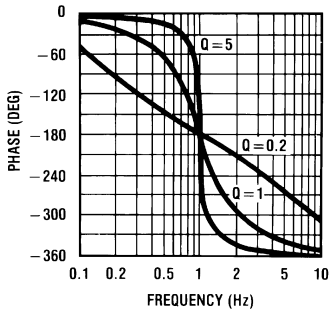


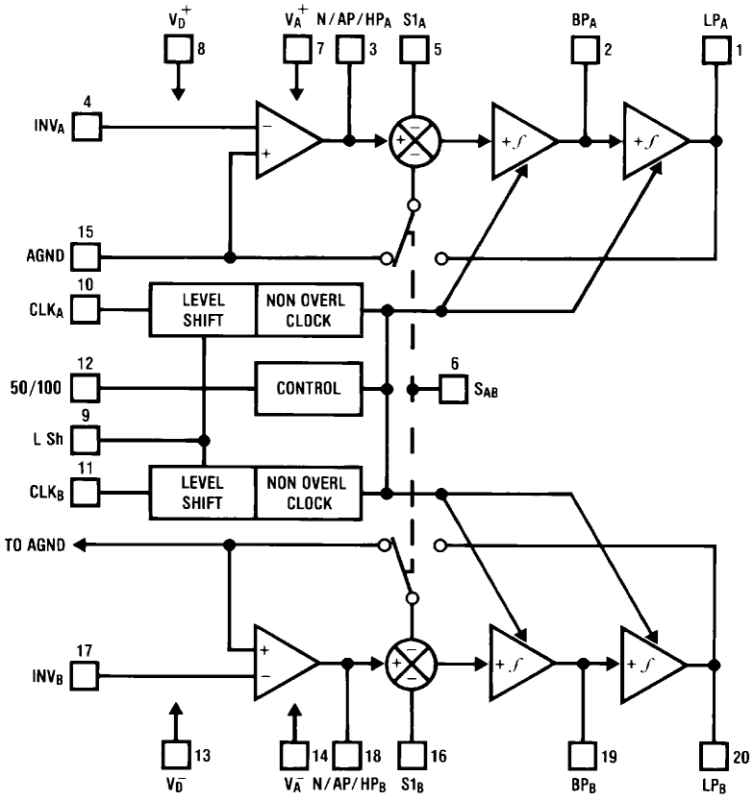
Figure 39. Allpass Response of Various Second-Order Filters as a Function of Q. Gains and Center Frequencies are Normalized to Unity Gain

8 Detailed Description

8.1 Overview

The LMF100 device contains two general-purpose, very high-performance switched capacitor filters that are cost-effective and space-saving. It enables designers to implement all the classical filters up to fourth-order biquad with one chip. This switched capacitor filters can be used in a broad range of industrial and consumer application such as audio, communication, instrumentation, medical, telemetry, etc. It can be directly cascaded to implement higher order filters,

8.2 Functional Block Diagram



8.3 Feature Description

The LMF100 is an all CMOS switched capacitor filter device that consists of two filters capable of wide supply range from 4 V to 15 V. It features much higher performance than the pin-compatible MF10 device with operation frequency to 100 kHz, which is 3X broader, and fo x Q range to 1.8 MHz which is 9X higher. Furthermore, it has pins that also function to configure filter modes of operation, level shifting, clock to filter center frequency setting, and power rail selections enabling flexibility and ease of programming.

8.4 Device Functional Modes

8.4.1 Modes of Operation

The LMF100 is a switched capacitor (sampled data) filter. To fully describe its transfer functions, a time domain analysis is appropriate. Because this is cumbersome, and because the LMF100 closely approximates continuous filters, the following discussion is based on the well-known frequency domain. Each LMF100 can produce two full second-order functions. See Table 1 for a summary of the characteristics of the various modes.

Device Functional Modes (continued)

8.4.1.1 MODE 1: Notch 1, Bandpass, Lowpass Outputs:

$f_{notch} = f_0$ (See Figure 40)

$$f_0 = \text{center frequency of the complex pole pair} = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50} \quad (1)$$

$$f_{notch} = \text{center frequency of the imaginary zero pair} = f_0 \quad (2)$$

$$H_{OLP} = \text{Lowpass gain (as } f \to 0) = -\frac{R2}{R1} \quad (3)$$

$$H_{OBP} = \text{Bandpass gain (at } f \to 0) = -\frac{R3}{R1} \quad (4)$$

$$H_{ON} = \text{Notch output gain as } \left.\begin{matrix} f \to 0 \\ f \to f_{CLK}/2 \end{matrix}\right\} = \frac{-R_2}{R_1} \quad (5)$$

$$Q = \frac{f_0}{BW} = \frac{R3}{R2} = \text{quality factor of the complex pole pair} \quad (6)$$

$$BW = \text{the } -3 \text{ dB bandwidth of the bandpass output.} \quad (7)$$

$$\text{Circuit dynamics}: H_{OBP_1} = Q \quad (8)$$

$$H_{OLP} = \frac{H_{OBP}}{Q} \text{ or } H_{OBP} = H_{OLP} \times Q = H_{ON} \times Q \quad (9)$$

$$H_{OLP(peak)} \cong Q \times H_{OLP} \text{ (for high Q's)} \quad (10)$$

8.4.1.2 MODE 1a: Noninverting BP, LP (See Figure 41)

$$f_0 = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50} \quad (11)$$

$$Q = \frac{R3}{R2} \quad (12)$$

$$H_{OLP} = -1; H_{OLP(peak)} \cong Q \times H_{OLP} \text{ (for high Q's)} \quad (13)$$

$$H_{OBP_1} = -\frac{R3}{R2} \quad (14)$$

$$H_{OBP_2} = 1 \text{ (noninverting)} \quad (15)$$

$$\text{Circuit dynamics}: H_{OBP_1} = Q \quad (16)$$

Note: VIN should be driven from a low-impedance (<1 kΩ) source.

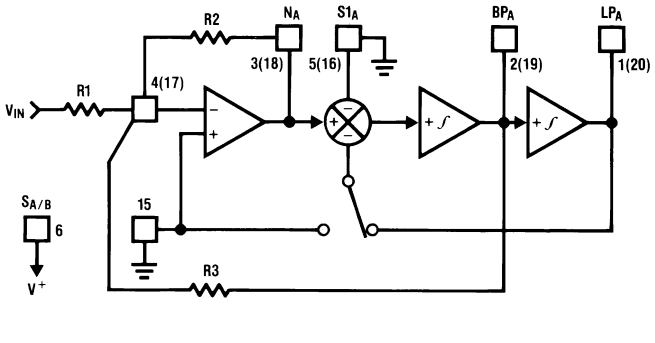


Figure 40. MODE 1

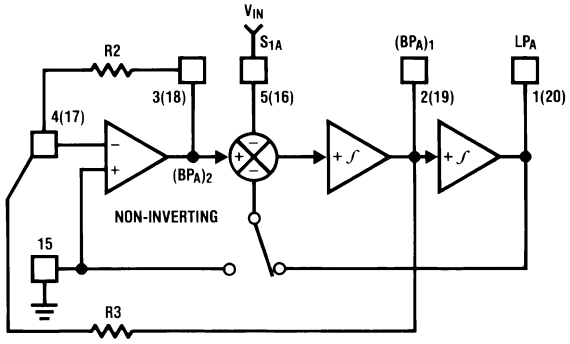


Figure 41. MODE 1a

Device Functional Modes (continued)

8.4.1.3 MODE 1b: Notch 1, Bandpass, Lowpass Outputs:

$f_{notch} = f_0$ (See Figure 42)

$$f_0 = \text{center frequency of the complex pole pair} = \frac{f_{CLK}}{100} \times \sqrt{2} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{2} \quad (17)$$

$$f_{notch} = \text{center frequency of the imaginary zero pair} = f_0 \quad (18)$$

$$H_{OLP} = \text{Lowpass gain (as } f \to 0) = -\frac{R2}{R1} \quad (19)$$

$$H_{OBP} = \text{Bandpass gain (at } f \to 0) = -\frac{R3}{R1} \quad (20)$$

$$H_{ON} = \text{Notch output gain as } \left.\begin{matrix} f \to 0 \\ f \to f_{CLK}/2 \end{matrix}\right\} = \frac{-R_2}{R_1} \quad (21)$$

$$Q = \frac{f_0}{BW} = \frac{R3}{R2} = \text{quality factor of the complex pole pair} \quad (22)$$

$$BW = \text{the } -3 \text{ dB bandwidth of the bandpass output.} \quad (23)$$

Circuit dynamics:

$$H_{OLP} = \frac{H_{OBP}}{\sqrt{2Q}} \text{ or } H_{OBP} = H_{OLP} \times Q = \sqrt{2} \quad (24)$$

$$H_{OBP} = \frac{H_{ON} \times Q}{\sqrt{2}} \quad (25)$$

$$H_{OLP(peak)} \cong Q \times H_{OLP} \text{ (for high Q's)} \quad (26)$$

8.4.1.4 MODE 2: Notch 2, Bandpass, Lowpass: $f_{notch} < f_0$ (See Figure 43)

$$f_0 = \text{center frequency} = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4} + 1} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4} + 1} \quad (27)$$

$$f_{notch} = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50} \quad (28)$$

$$Q = \text{quality factor of the complex pole pair} = \frac{\sqrt{R2/R4 + 1}}{R2/R3} \quad (29)$$

$$H_{OLP} = \text{Lowpass output gain (as } f \to 0) = -\frac{R2/R1}{R2/R4 + 1} \quad (30)$$

$$H_{OBP} = \text{Bandpass gain (at } f \to f_0) = -R3/R1 \quad (31)$$

$$H_{ON_1} = \text{Notch output gain (as } f \to 0) = -\frac{R2/R1}{R2/R4 + 1} \quad (32)$$

$$H_{ON_1} = \text{Notch output gain} \left(\text{as } f \to \frac{f_{CLK}}{2} \right) = -R2/R1 \quad (33)$$

$$\text{Filter dynamics}: H_{OBP} = Q\sqrt{H_{OLP}\, H_{ON_2}} = \sqrt{H_{OLP_1}\, H_{ON_2}} \quad (34)$$

Device Functional Modes (continued)

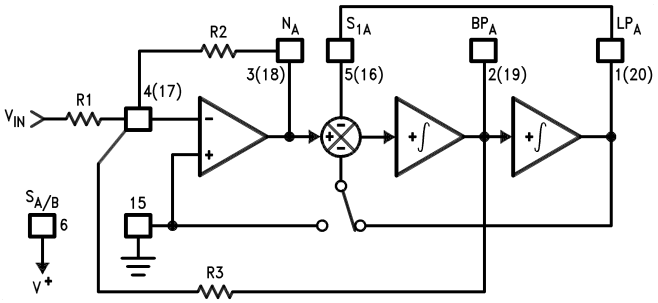


Figure 42. MODE 1b

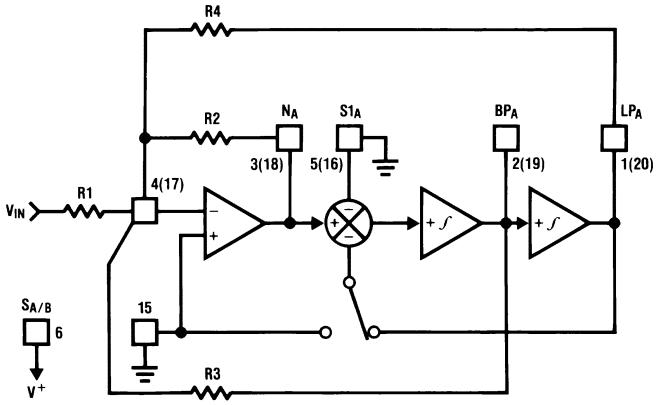


Figure 43. MODE 2

8.4.1.5 MODE 3: Highpass, Bandpass, Lowpass Outputs (See Figure 44)

$$f_0 = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4} + 1} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}} \tag{35}$$

$$Q = \text{quality factor of the complex pole pair} = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2} \tag{36}$$

$$H_{OLP} = \text{Highpass gain at} \left(f \rightarrow \frac{f_{CLK}}{2} \right) = -\frac{R2}{R1} \tag{37}$$

$$H_{OBP} = \text{Bandpass gain as} \left(f \rightarrow f_0 \right) = -\frac{R3}{R1} \tag{38}$$

$$H_{OLP} = \text{Lowpass gain (as } f \rightarrow 0) = -\frac{R4}{R1} \tag{39}$$

$$\text{Circuit dynamics}: \frac{R2}{R4} = \frac{H_{OHP}}{H_{OLP}}; H_{OBP} = \sqrt{H_{OHP} \times H_{OLP}} \times Q \tag{40}$$

$$H_{OLP(peak)} \cong Q \times H_{OLP} \text{ (for high Q's)} \tag{41}$$

$$H_{OHP(peak)} \cong Q \times H_{OHP} \text{ (for high Q's)} \tag{42}$$

8.4.1.6 MODE 3a: HP, BP, LP and Notch With External Op Amp (See Figure 45)

$$f_0 = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}} \tag{43}$$

$$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2} \tag{44}$$

$$H_{OHP} = -\frac{R2}{R1} \tag{45}$$

$$H_{OBP} = -\frac{R3}{R1} \tag{46}$$

$$H_{OLP} = -\frac{R4}{R1} \tag{47}$$

$$f_n = \text{notch frequency} = \frac{f_{CLK}}{100} \sqrt{\frac{R_h}{R_l}} \text{ or } \frac{f_{CLK}}{50} \sqrt{\frac{R_h}{R_l}} \tag{48}$$

Device Functional Modes (continued)

$$H_{ON} = \text{gain of notch at } f = f_0 = \left\| Q\left(\frac{R_g}{R_I}H_{OLP} - \frac{R_g}{R_h}H_{OHP}\right)\right\| \quad (49)$$

$$H_{n1} = \text{gain of notch } (\text{as } f \to 0) = \frac{R_g}{R_I} \times H_{OLP} \quad (50)$$

$$H_{n2} = \text{gain of notch } \left(\text{as } f \to \frac{f_{CLK}}{2}\right) = \frac{R_g}{R_h} \times H_{OHP} \quad (51)$$

*In Mode 3, the feedback loop is closed around the input summing amplifier; the finite GBW product of this op amp causes a slight Q enhancement. If this is a problem, connect a small capacitor (10 pF−100 pF) across R4 to provide some phase lead.

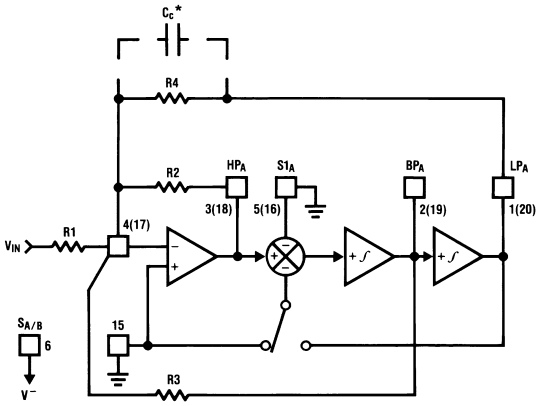


Figure 44. MODE 3

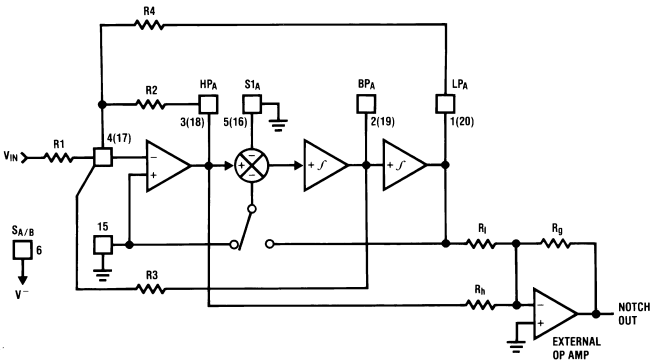


Figure 45. MODE 3a

8.4.1.7 MODE 4: Allpass, Bandpass, Lowpass Outputs (See Figure 46)

$$f_0 = \text{center frequency} = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}; f_z^* = \text{center frequency of the complex zero} \approx f_0 \quad (52)$$

$$Q = \frac{f_0}{BW} \times \frac{R3}{R2}; Qz = \text{quality factor of the complex zero pair} - \frac{R3}{R1} \quad (53)$$

For AP output make R1 = R2 (54)

$$H_{OAP}^* = \text{Allpass gain } \left(\text{at } 0 - f = \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1} = -1 \quad (55)$$

$$H_{OLP} = \text{Lowpass gain } (\text{as } f \to 0) = -\left(\frac{R2}{R1} + 1\right) = -2 \quad (56)$$

$$H_{OBP} = \text{Bandpass gain } (\text{at } f \to f_0) = -\frac{R3}{R2}\left(1 + \frac{R2}{R1}\right) = -2\left(\frac{R3}{R2}\right) \quad (57)$$

$$\text{Circuit dynamics}: H_{OBP} = H_{OLP} \times Q = (H_{OAP} + 1)Q \quad (58)$$

*Due to the sampled data nature f the filter, as light mismatch for f_z and f_0 occurs, causing a 0.4-dB peaking around f_0 of the allpass filter amplitude response (which theorectically should be a straight line). If this is unacceptable, TI recommends Mode 5.

8.4.1.8 MODE 5: Numerator Complex Zeros, BP, LP (See Figure 47)

$$f_0 = \sqrt{1 + \frac{R2}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1 + \frac{R2}{R4}} \times \frac{f_{CLK}}{50} \quad (59)$$

$$f_z = \sqrt{1 - \frac{R1}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1 - \frac{R1}{R4}} \times \frac{f_{CLK}}{50} \quad (60)$$

Device Functional Modes (continued)

$$Q = \sqrt{1 + R2/R4} \times \frac{R3}{R2} \tag{61}$$

$$Q_z = \sqrt{1 - R1/R4} \times \frac{R3}{R1} \tag{62}$$

$$H_{0z1} = \text{gain at C.Z. output } (\text{as } f \to 0 \text{ Hz}) \frac{-R2(R4 - R1)}{R1(R2 + R4)} \tag{63}$$

$$H2 = \text{gain at C.Z. output } \left(\text{as } f \to \frac{f_{CLK}}{2}\right) \frac{-R2}{R1} \tag{64}$$

$$H_{OBP} = -\left(\frac{R2}{R1} + 1\right) \times \frac{R3}{R2} \tag{65}$$

$$H_{OLP} = -\left(\frac{R2 + R1}{R2 + R4}\right) \times \frac{R4}{R1} \tag{66}$$

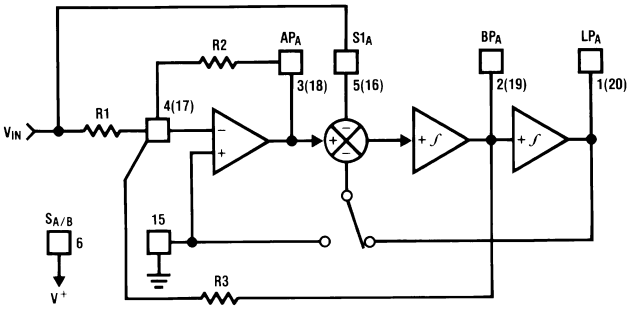


Figure 46. MODE 4

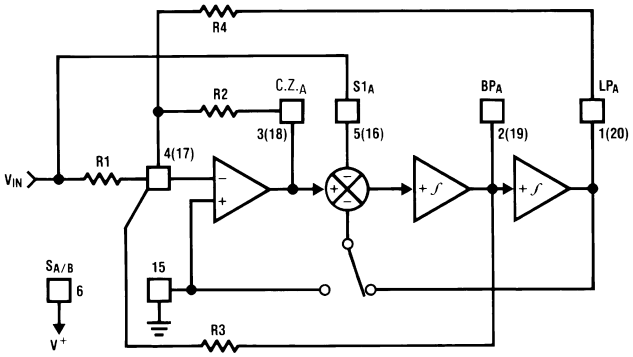


Figure 47. MODE 5

8.4.1.9 MODE 6a: Single-Pole, HP, LP Filter (See Figure 48)

$$f_0 = \text{cutoff frequency of LP or HP output} = \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50} \tag{67}$$

$$H_{OLP} = -\frac{R3}{R1} \tag{68}$$

$$H_{OHP} = -\frac{R2}{R1} \tag{69}$$

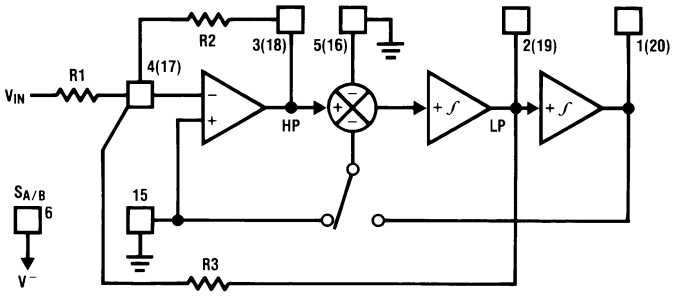


Figure 48. MODE 6a

8.4.1.10 MODE 6b: Single-Pole LP Filter (Inverting and Noninverting) (See Figure 49)

$$f_c = \text{cutoff frequency of LP outputs} = \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50} \tag{70}$$

Device Functional Modes (continued)

$$H_{OLP_1} = 1\,(\text{noninverting}) \tag{71}$$

$$H_{OHP_2} = \frac{R3}{R2} \tag{72}$$

8.4.1.11 MODE 6c: Single-Pole, AP, LP Filter (See Figure 50)

$$f_c = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50} \tag{73}$$

$$H_{OAP} = 1\,(\text{as } f \to 0) \tag{74}$$

$$H_{OAP} = -1\,(\text{as } f \to f_{CLK}/2) \tag{75}$$

$$H_{OLP} = -2 \tag{76}$$

$$R_1 = R_2 = R_3 \tag{77}$$

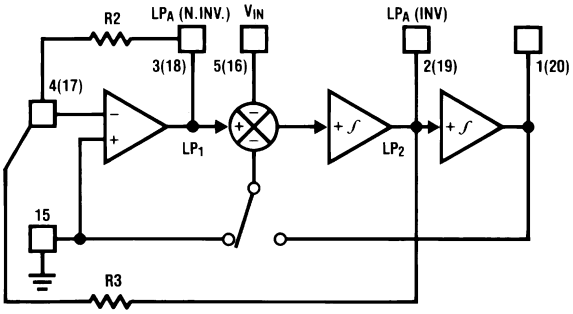


Figure 49. MODE 6b

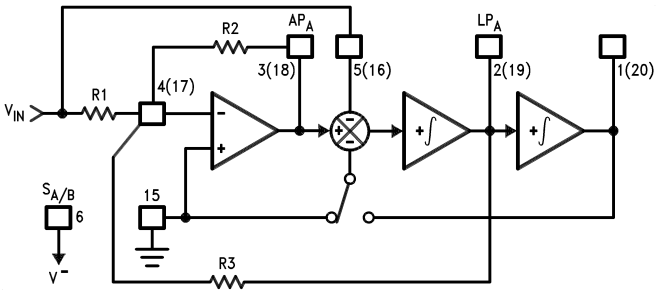


Figure 50. MODE 6c

8.4.1.12 Summing Integrator (See Figure 52)

$$\tau = \text{integrator time constant} \cong \frac{16}{f_{CLK}} \text{ or } \frac{8}{f_{CLK}}$$

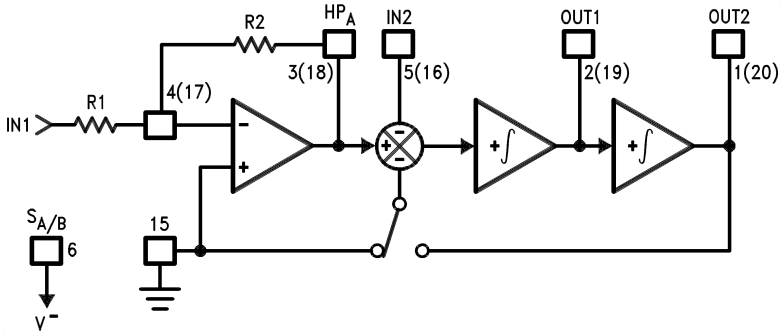


Figure 51. Equivalent Circuit

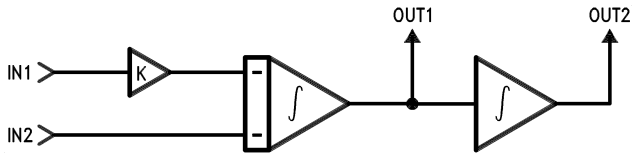


Figure 52. MODE 7

Device Functional Modes (continued)

Table 1. Summary of Modes(1)

MODE	BP	LP	HP	N	AP	NUMBER OF RESISTORS	ADJUSTABLE f_{CLK}/f_0	NOTES
1	*	*		*		3	No	
1a	$H_{OBP1} = -Q$ $H_{OBP2} = +1$	$H_{OLP} = +1$				2	No	May need input buffer. Poor dynamics for high Q.
1b	*	*		*		3	No	Useful for high-frequency applications.
2	*	*		*		3	Yes (above $f_{CLK}/50$ or $f_{CLK}/100$)	
3	*	*	*			4	Yes	Universal State-Variable Filter. Best general-purpose mode.
3a	*	*	*	*		7	Yes	As above, but also includes resistor-tuneable notch.
4	*	*			*	3	No	Gives Allpass response with $H_{OAP} = -1$ and $H_{OLP} = -2$.
5	*	*			*	4	Yes	Gives flatter allpass response than above if $R_1 = R_2 = 0.02R_4$.
6a		*	*			3	Yes	Single pole.
6b		$H_{OLP1} = +1$ $H_{OLP2} = \frac{-R3}{R2}$				2	Yes	Single pole.
6c		*			*	3	No	Single pole.
7						2	Yes	Summing integrator with adjustable time constant.

(1) Realizable filter types (that is, lowpass) denoted by asterisks (*). Unless otherwise noted, gains of various filter outputs are inverting and adjustable by resistor ratios.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMF100 is a general purpose dual second-order state variable filter whose center frequency is proportional to the frequency of the square wave applied to the clock input (f_{CLK}). The various clocking options are summarized in Table 2.

Table 2. Clocking Options

POWER SUPPLY	CLOCK LEVELS	LSh	V_D^+
−5 V and +5 V	TTL (0 V to 5 V)	0 V	+5 V
−5 V and +5 V	CMOS (−5 V to +5 V)	0 V	+5 V
0 V and 10 V	TTL (0 V to 5 V)	0 V	+10 V
0 V and 10 V	CMOS (0 V to 10 V)	+5 V	+10 V
−2.5 V and +2.5 V	CMOS	0 V	+2.5 V
0 V and 5 V	(−2.5 V to +2.5 V) TTL (0 V to 5 V)	0 V	0 V
0 V and 5 V	CMOS (0 V to 5 V)	+2.5 V	+5 V

By connecting pin 12 to the appropriate DC voltage, the filter center frequency, f_0, can be made equal to either $f_{CLK}/100$ or $f_{CLK}/50$. f_0 can be very accurately set (within ±0.6%) by using a crystal clock oscillator, or can be easily varied over a wide frequency range by adjusting the clock frequency. If desired, the fC_{LK}/f_0 ratio can be altered by external resistors as in Figure 43 through Figure 49. This is useful when high-order filters (greater than two) are to be realized by cascading the second-order sections. This allows each stage to be stagger tuned while using only one clock. The filter Q and gain are set by external resistor ratios.

All of the five second-order filter types can be built using either section of the LMF100. These are illustrated in Figure 25 through Figure 33 along with their transfer functions and some related equations. Figure 35 shows the effect of Q on the shapes of these curves.

9.2 Typical Application

When designing a LP filter that has similar pass band characteristic as a Butterworth topology but requiring a much steeper roll off then a fourth-order Chebyshev topology can implement the need with one LMF100.

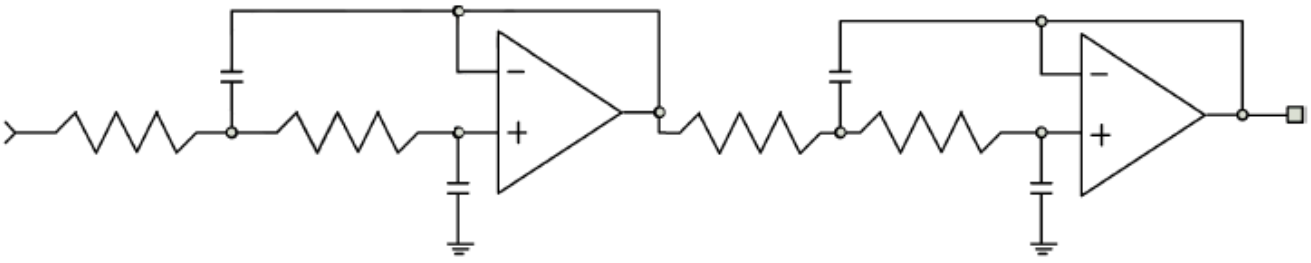


Figure 53. Implement a Fourth-Order Chebyshev LP Filter Having a 1-kHz Cutoff Frequency and 1-dB PB Ripple With an LMF100

Typical Application (continued)

9.2.1 Design Requirements

In order to design a filter using the LMF100, we must define the necessary values of three parameters for each second-order section: f_0, the filter section's center frequency; H_0, the passband gain; and the filter's Q. These are determined by the characteristics required of the filter being designed.

As an example, assume that a system requires a fourth-order Chebyshev lowpass filter with 1-dB ripple, unity gain at DC, and 1000 Hz cutoff frequency. As the system order is four, it is realizable using both second-order sections of an LMF100. Many filter design texts (and TI Switched Capacitor Filter Handbook) include tables that list the characteristics (f_0 and Q) of each of the second-order filter sections needed to synthesize a given higher-order filter. For the Chebyshev filter defined above, such a table yields the following characteristics:

f_{0A} = 529 Hz Q_A = 0.785

f_{0B} = 993 Hz Q_B = 3.559

For unity gain at DC, we also specify:

H_{0A} = 1

H_{0B} = 1

The desired clock-to-cutoff-frequency ratio for the overall filter of this example is 100, and a 100-kHz clock signal is available. The required center frequencies for the two second-order sections will not be obtainable with clock-to-center-frequency ratios of 50 or 100. It will be necessary to adjust $\frac{f_{CLK}}{f_0}$ externally. From Table 1, we see that Mode 3 can be used to produce a lowpass filter with resistor-adjustable center frequency.

In most filter designs involving multiple second-order stages, it is best to place the stages with lower Q values ahead of stages with higher Q, especially when the higher Q is greater than 0.707. This is due to the higher relative gain at the center frequency of a higher-Q stage. Placing a stage with lower Q ahead of a higher-Q stage will provide some attenuation at the center frequency and thus help avoid clipping of signals near this frequency. For this example, stage A has the lower Q (0.785) so it will be placed ahead of the other stage.

For the first section, we begin the design by choosing a convenient value for the input resistance: R_{1A} = 20 k. The absolute value of the passband gain H_{OLPA} is made equal to 1 by choosing R_{4A} such that: $R_{4A} = -H_{OLPA}R_{1A} = R_{1A}$ = 20 k. If the 50/100/CL pin is connected to mid-supply for nominal 100:1 clock-to-center-frequency ratio, we find R_{2A} by:

$$R_{2A} = R_{4A}\frac{{f_{0A}}^2}{\left(f_{CLK}/100\right)^2} = 2\times10^4 \times \frac{(529)^2}{(1000)^2} = 5.6\text{k and}$$

$$R_{3A} = Q_A\sqrt{R_{2A}R_{4A}} = 0.785\sqrt{5.6\times10^3\times2\times10^4} = 8.3\text{k}$$

The resistors for the second section are found in a similar fashion:

$$R_{1B} = 20\text{k}$$

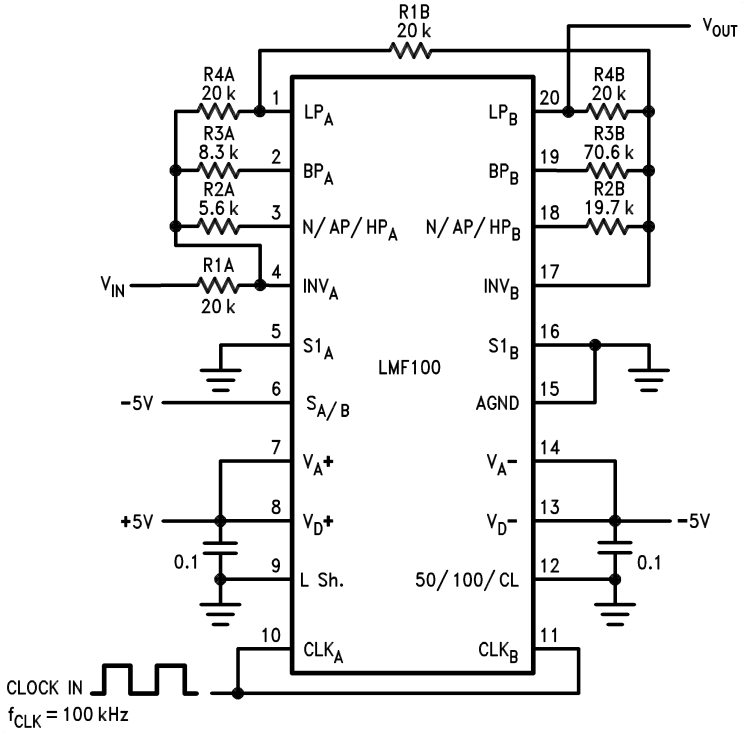
$$R_{4B} = R_{1B} = 20\text{k}$$

$$R_{2B} = R_{4B}\frac{{f_{0B}}^2}{\left(f_{CLK}/100\right)^2} = 20\text{k}\frac{(993)^2}{(1000)^2} = 19.7\text{k}$$

$$R_{3B} = Q_B\sqrt{R_{2B}R_{4B}} = 3.559\sqrt{1.97\times10^4\times2\times10^4} = 70.6\text{k}$$

Typical Application (continued)

The complete circuit is shown in Figure 54 for split ±5-V power supplies. TI highly recommends Supply bypass capacitors.



±5-V power supply. 0-V to 5-V TTL or ±5-V CMOS logic levels.

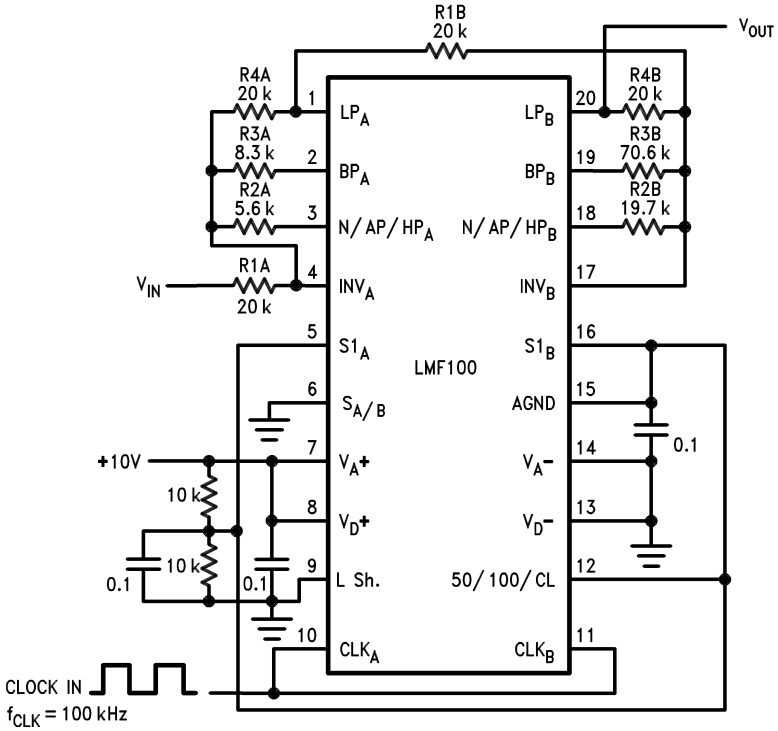
Figure 54. Fourth-Order Chebyshev Lowpass Filter from Example in 3.1.

9.2.2 Detailed Design Procedure

9.2.2.1 Single-Supply Operation

The LMF100 can also operate with a single-ended power supply. Figure 55 shows the example filter with a single-ended power supply. V_A^+ and V_D^+ are again connected to the positive power supply (4 to 15 volts), and V_A^- and V_D^- are connected to ground. The AGND pin must be tied to $V^+/2$ for single-supply operation. This half-supply point should be very “clean”, as any noise appearing on it will be treated as an input to the filter. It can be derived from the supply voltage with a pair of resistors and a bypass capacitor (Figure 56), or a low-impedance half-supply voltage can be made using a three-terminal voltage regulator or an operational amplifier (Figure 57 and Figure 58). The passive resistor divider with a bypass capacitor is sufficient for many applications, provided that the time constant is long enough to reject any power supply noise. It is also important that the half-supply reference present a low impedance to the clock frequency, so at very low clock frequencies the regulator or operational amplifier approaches may be preferable because they will require smaller capacitors to filter the clock frequency. The main power supply voltage should be clean (preferably regulated) and bypassed with 0.1 µF

Typical Application (continued)



Single 10-V power supply. 0-V to 5-V TTL logic levels. Input signals should be referred to half-supply or applied through a coupling capacitor.

Figure 55. Fourth-Order Chebyshev Lowpass Filter from Example in 3.1.

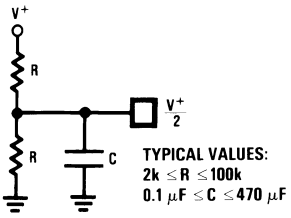


Figure 56. Three Ways of Generating $V^+/2$ for Single-Supply Operation Option A

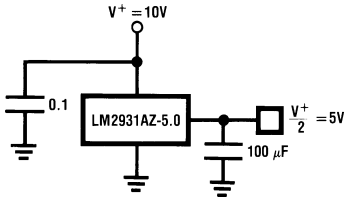


Figure 57. Three Ways of Generating $V^+/2$ for Single-Supply Operation Option B

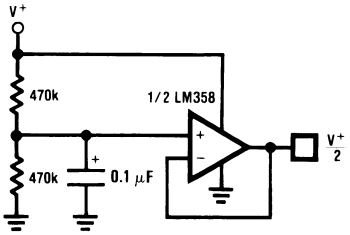


Figure 58. Three Ways of Generating $V^+/2$ for Single-Supply Operation Option C

9.2.2.2 Dynamic Considerations

The maximum signal handling capability of the LMF100, like that of any active filter, is limited by the power supply voltages used. The amplifiers in the LMF100 can swing to within about 1 volt of the supplies, so the input signals must be kept small enough that none of the outputs will exceed these limits. If the LMF100 is operating on ±5 volts, for example, the outputs will clip at about 8 V_{p-p}. The maximum input voltage multiplied by the filter gain should therefore be less than 8 V_{p-p}.

Typical Application (continued)

If the filter Q is high, the gain at the lowpass or highpass outputs will be much greater than the nominal filter gain (Figure 35). As an example, a lowpass filter with a Q of 10 will have a 20-dB peak in its amplitude response at f_0. If the nominal gain of the filter (H_{OLP}) is equal to 1, the gain at f_0 will be 10. The maximum input signal at f_0 must therefore be less than 800 mV_{p-p} when the circuit is operated on ±5 volt supplies.

Also, one output can have a reasonable small voltage on it while another is saturated. This is most likely for a circuit such as the notch in Mode 1 (Figure 40). The notch output will be very small at f_0, so it might appear safe to apply a large signal to the input. However, the bandpass will have its maximum gain at f_0 and can clip if overdriven. If one output clips, the performance at the other outputs will be degraded, so avoid overdriving any filter section, even ones whose outputs are not being directly used. Accompanying Figure 40 through Figure 50 are equations labeled *circuit dynamics*, which relate the Q and the gains at the various outputs. These should be consulted to determine peak circuit gains and maximum allowable signals for a given application.

9.2.2.3 Offset Voltage

The switched capacitor integrators of the LMF100 have a slightly higher input offset voltage than found in a typical continuous time active filter integrator. Because of TI's new LMCMOS process and new design techniques the internal offsets have been minimized, compared to the industry standard MF10. Figure 59 shows an equivalent circuit of the LMF100 from which the output DC offsets can be calculated. Typical values for these offsets with $S_{A/B}$ tied to V^+ are:

V_{OS1} = opamp offset = ±5 mV
V_{OS2} = ±30 mV at 50:1 or 100:1
V_{OS3} = ±15 mV at 50:1 or 100:1

When $S_{A/B}$ is tied to V^-, V_{OS2} will approximately halve. The DC offset at the BP output is equal to the input offset of the lowpass integrator (V_{OS3}). The offsets at the other outputs depend on the mode of operation and the resistor ratios, as described in the following expressions.

Mode 1 and Mode 4

$$V_{OS(N)} = V_{OS1}\left(\frac{1}{Q} + 1 + \|H_{OLP}\|\right) - \frac{V_{OS3}}{Q}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 1a

$$V_{OS}(\text{N.INV.BP}) = \left(1 + \frac{1}{Q}\right)V_{OS1} - \frac{V_{OS3}}{Q}$$

$$V_{OS}(\text{INV.BP}) = V_{OS3}$$

$$V_{OS}(\text{LP}) = V_{OS}(\text{N.INV.BP}) - V_{OS2}$$

Mode 1b

$$V_{OS(N)} = V_{OS1}\left(1 + \frac{R2}{R3} + \frac{R2}{R1}\right) - \frac{R2}{R3}V_{OS3}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = \frac{V_{OS(N)}}{2} - \frac{V_{OS2}}{2}$$

Mode 2 and Mode 5

$$V_{OS(N)} = \left(\frac{R2}{Rp} + 1\right)V_{OS3} \times \frac{1}{1 + R2/R4} + V_{OS2}\frac{1}{1 + R4/R2} - \frac{V_{OS3}}{Q\sqrt{1 + R2/R4}} : R_p = R1 \| R3 \| R4$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Typical Application (continued)

Mode 3

$$V_{OS(HP)} = V_{OS2}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS1}\left[1+\frac{R4}{R_p}\right] - V_{OS2}\left(\frac{R4}{R2}\right) - V_{OS3}\left(\frac{R4}{R3}\right)$$

$$R_p = R1 \,||\, R2 \,||\, R3$$

Mode 6a and 6c

$$V_{OS(HP)} = V_{OS2}$$

$$V_{OS(LP)} = V_{OS1}\left(1+\frac{R_3}{R_2}+\frac{R_3}{R_1}\right) - \frac{R_3}{R_2}V_{OS2}$$

Mode 6b

$$V_{OS(LP(N.INV))} = V_{OS2}$$

$$V_{OS(LP(INV))} = V_{OS1}\left(1+\frac{R_3}{R_2}\right) - \frac{R_3}{R_2}V_{OS2}$$

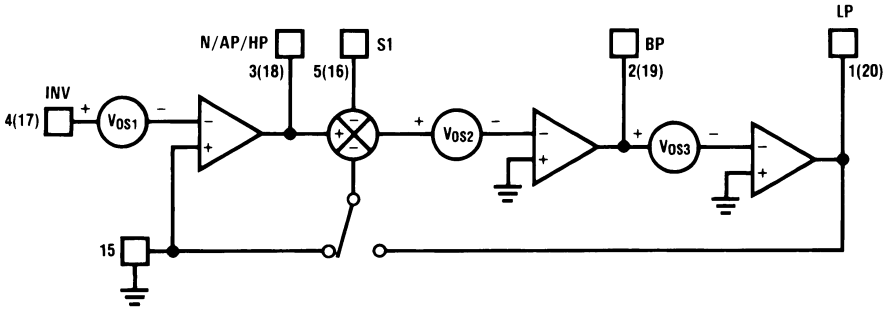
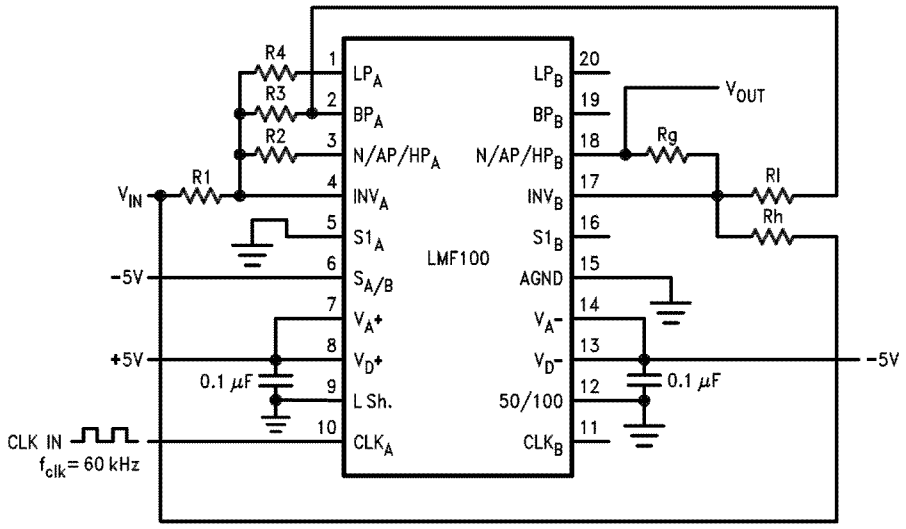


Figure 59. Offset Voltage Sources

In many applications, the outputs are AC-coupled and DC offsets are not bothersome unless large signals are applied to the filter input. However, larger offset voltages will cause clipping to occur at lower AC signal levels, and clipping at any of the outputs will cause gain nonlinearities and will change f_0 and Q. When operating in Mode 3, offsets can become excessively large if R_2 and R_4 are used to make f_{CLK}/f_0 significantly higher than the nominal value, especially if Q is also high.

For example, Figure 60 shows a second-order 60-Hz notch filter. This circuit yields a notch with about 40 dB of attenuation at 60 Hz. A notch is formed by subtracting the bandpass output of a mode 3 configuration from the input using the unused side B operational amplifier. The Q is 10 and the gain is 1 V/V in the passband. However, f_{CLK}/f_0 = 1000 to allow for a wide input spectrum. This means that for pin 12 tied to ground (100:1 mode), R4/R2 = 100. The offset voltage at the lowpass output (LP) will be about 3 V. However, this is an extreme case and the resistor ratio is usually much smaller. Where necessary, the offset voltage can be adjusted by using the circuit of Figure 61. This allows adjustment of V_{OS1}, which will have varying effects on the different outputs as described in the above equations. Some outputs cannot be adjusted this way in some modes, however ($V_{OS(BP)}$ in modes 1a and 3, for example).

Typical Application (continued)



R1 = 100 kΩ
R2 = 1 kΩ
R3 = 100 kΩ
R4 = 100 kΩ
Rg = 10 kΩ
RI = 10 kΩ
Rh = 10 kΩ

Figure 60. Second-Order Notch Filter

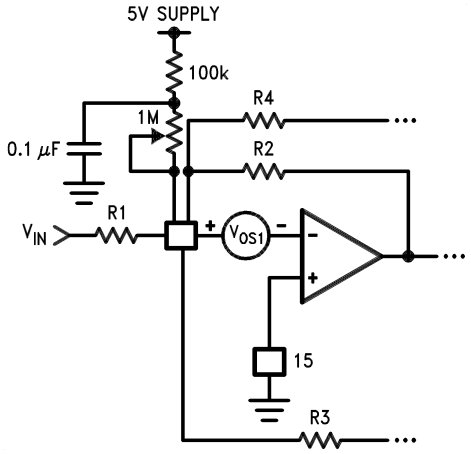


Figure 61. Method for Trimming V_{OS}

9.2.2.4 Sampled Data System Considerations

The LMF100 is a sampled data filter, and as such, differs in many ways from conventional continuous-time filters. An important characteristic of sampled-data systems is their effect on signals at frequencies greater than one-half the sampling frequency. (The sampling frequency of the LMF100 is the same as its clock frequency.) If a signal with a frequency greater than one-half the sampling frequency is applied to the input of a sampled data system, it will be *reflected* to a frequency less than one-half the sampling frequency. Thus, an input signal whose

Typical Application (continued)

frequency is $f_s/2$ + 100 Hz will cause the system to respond as though the input frequency was $f_s/2$ − 100 Hz. This phenomenon is known as *aliasing*, and can be reduced or eliminated by limiting the input signal spectrum to less than $f_s/2$. This may in some cases require the use of a bandwidth-limiting filter ahead of the LMF100 to limit the input spectrum. However, because the clock frequency is much higher than the center frequency, this will often not be necessary.

Another characteristic of sampled-data circuits is that the output signal changes amplitude once every sampling period, resulting in “steps” in the output voltage which occur at the clock rate (Figure 62). If necessary, these can be “smoothed” with a simple R-C lowpass filter at the LMF100 output.

The ratio of f_{CLK} to f_c (normally either 50:1 or 100:1) will also affect performance. A ratio of 100:1 will reduce any aliasing problems and is usually recommended for wideband input signals. In noise-sensitive applications, a ratio of 100:1 will result in 3 dB lower output noise for the same filter configuration.

The accuracy of the f_{CLK}/f_0 ratio is dependent on the value of Q. This is shown in the curves under the heading Figure 54. As Q is changed, the true value of the ratio changes as well. Unless the Q is low, the error in f_{CLK}/f_0 will be small. If the error is too large for a specific application, use a mode that allows adjustment of the ratio with external resistors.

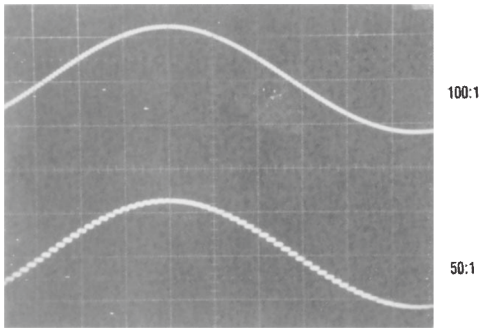


Figure 62. The Sampled-Data Output Waveform

9.2.3 Application Curve

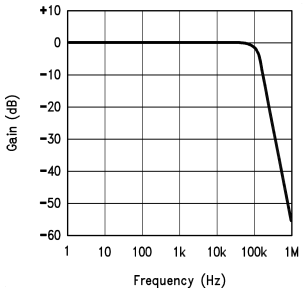


Figure 63. The Wide BW of a Fourth-Order Butterworth LP Implemented With One LMF100

10 Power Supply Recommendations

The LMF100 can operate with a single-ended power supply as well as bipolar supplies. Refer to Figure 56 through Figure 58 for methods of generating V+/2 for single-supply operation. In this circumstance, pins VA+ and VD+ are connected to the positive power supply (4 to 15 V), and VA− and VD− are connected to ground. The AGND pin must be tied to V+/2. Furthermore, the half-supply node should be very “clean”, as any noise appearing on it will be treated as an input to the filter. Ensure liberal bypassing is employed to reject any supply noise and present a low impedance to the clock frequency. Bypass caps should always be located as close to the supply pins a practical. Moreover, the regulator or op-amp approaches of generating V+/e is preferred for very low clock frequency applications. The main power supply voltage should also be clean (preferably regulated) and bypassed with 0.1-µF nonpolar ceramic capacitor. If there is no bulk cap nearby, a 10-uF electrolytic tantalum in parallel with the 0.1-µF supply bypass cap should achieve cleaner and optimal transient response. Select capacitors with low ESR and ESL rating and test them to ensure no ringing occurs. The power source is preferably a linear supply or regulator. If a switching supply is used ensure it is a clean switcher and deploy proper bypassing or post regulate with an LDO as necessary.

11 Layout

11.1 Layout Guidelines

The most critical part to the success of a switched capacitor filter design is a properly layout PCB. Because of the mixed signal circuitry involved, take extra care in the board design for noise abatement, star-grounding, and shielding techniques. A ground plane must separate digital and analog ground planes if possible, or have separate paths and join together only at the common return node at the supply source. All component leads and PCB tracks are kept as short as possible. The filter clock input should be a shielded cable.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

12.1.1.1 Definitions of Terms

f_{CLK}: the frequency of the external clock signal applied to pin 10 or 11.

f_0: center frequency of the second order function complex pole pair. f_0 is measured at the bandpass outputs of the LMF100, and is the frequency of maximum bandpass gain. (Figure 25).

f_{notch}: the frequency of minimum (ideally zero) gain at the notch outputs.

f_z: the center frequency of the second order complex zero pair, if any. If f_z is different from f_0 and if Q_z is high, it can be observed as the frequency of a notch at the allpass output. (Figure 46).

Q: "quality factor" of the 2nd order filter. Q is measured at the bandpass outputs of the LMF100 and is equal to f_0 divided by the −3 dB bandwidth of the 2nd order bandpass filter (Figure 25). The value of Q determines the shape of the 2nd order filter responses as shown in Figure 35.

Q_Z: the quality factor of the second order complex zero pair, if any. Q_Z is related to the allpass characteristic, which is written:

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_o + \omega_o^2}{Q_z}\right)}{s^2 - \frac{s\omega_o}{Q} + \omega_o^2}$$

where $Q_Z = Q$ for an allpass response.

H_{OLP}: the gain (in V/V) of the lowpass output as f → 0 Hz (Figure 27).

H_{OHP}: the gain (in V/V) of the highpass output as f → $f_{CLK}/2$ (Figure 29).

H_{ON}: the gain (in V/V) of the notch output as f → 0 Hz and as f → $f_{CLK}/2$, when the notch filter has equal gain above and below the center frequency (Figure 31). When the low-frequency gain differs from the high-frequency gain, as in modes 2 and 3a (Figure 43 and Figure 45), the two quantities below are used in place of H_{ON}.

H_{ON1}: the gain (in V/V) of the notch output as f → 0 Hz.

H_{ON2}: the gain (in V/V) of the notch output as f → $f_{CLK}/2$.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

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12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMF100CIWM	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	LMF100 CIWM	
LMF100CIWM/NOPB	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	LMF100 CIWM	
LMF100CIWMX	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	LMF100 CIWM	
LMF100CIWMX/NOPB	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	LMF100 CIWM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

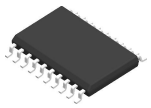
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

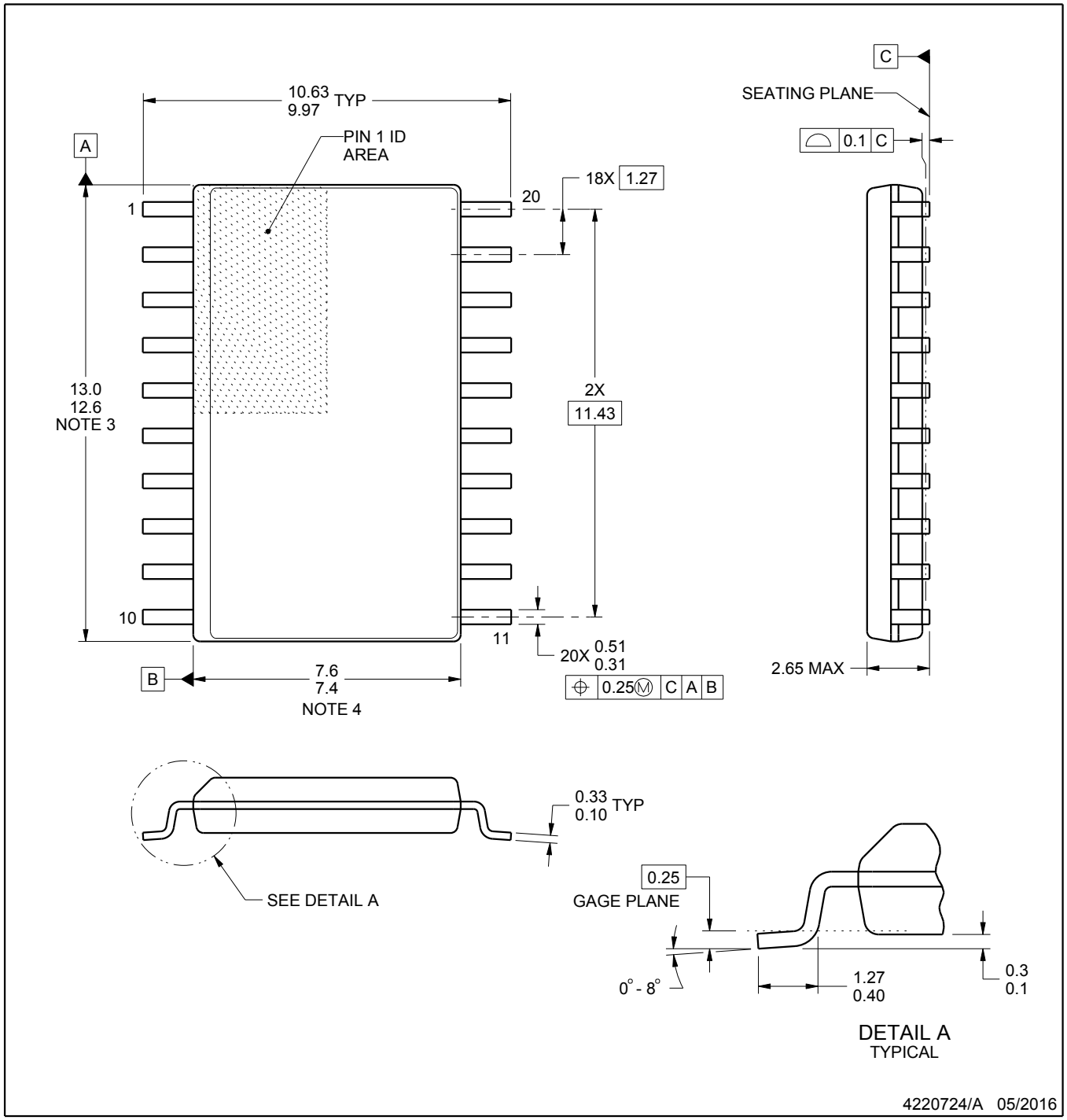


PACKAGE OUTLINE

DW0020A

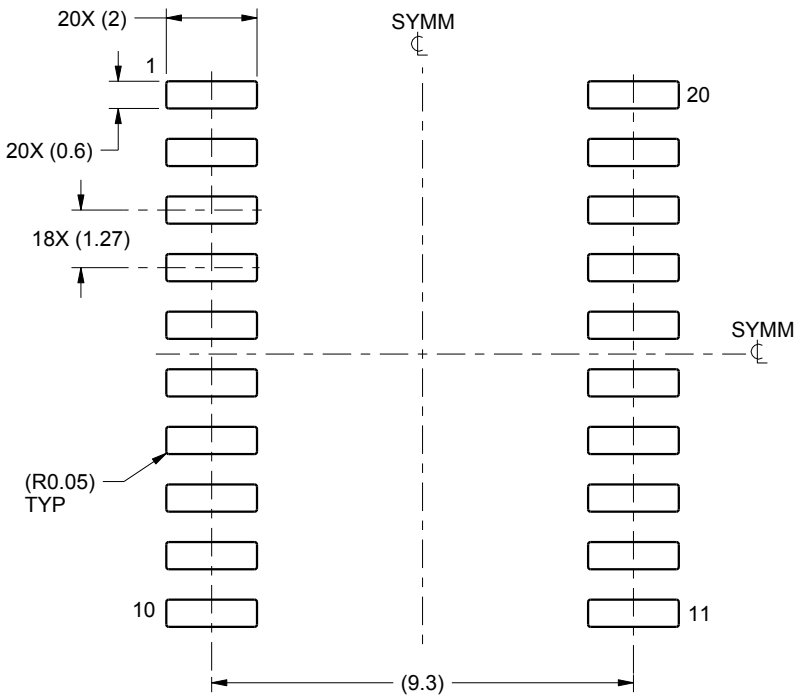
SOIC - 2.65 mm max height

SOIC

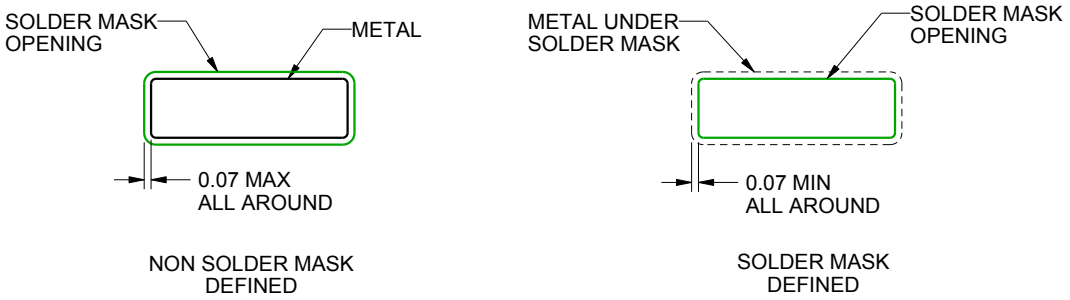


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

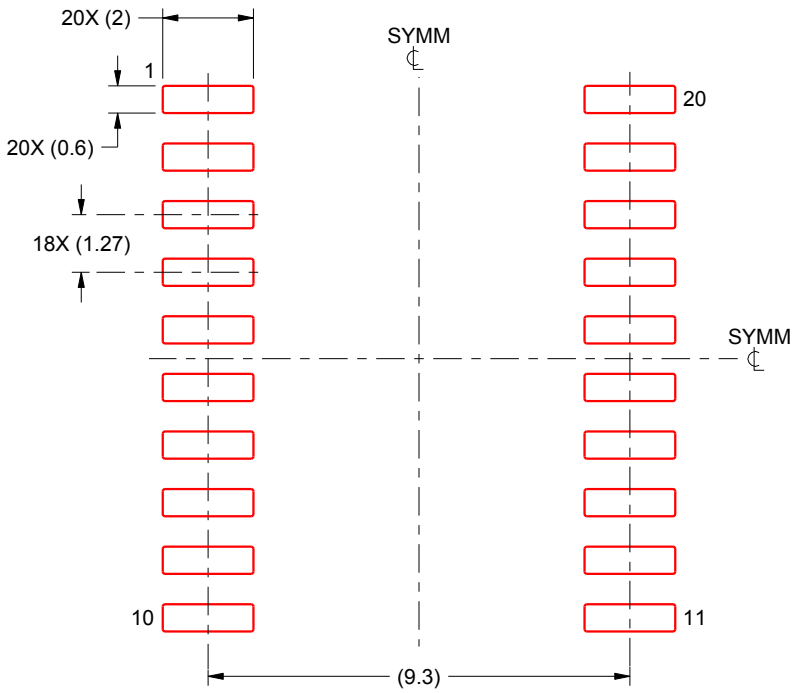


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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