

OPA124

Low Noise Precision *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- **LOW NOISE:** $6\text{nV}/\sqrt{\text{Hz}}$ (10kHz)
- **LOW BIAS CURRENT:** 1pA max
- **LOW OFFSET:** 250 μV max
- **LOW DRIFT:** 2 $\mu\text{V}/^\circ\text{C}$ max
- **HIGH OPEN-LOOP GAIN:** 120dB min
- **HIGH COMMON-MODE REJECTION:** 100dB min
- **AVAILABLE IN 8-PIN PLASTIC DIP AND 8-PIN SOIC PACKAGES**

DESCRIPTION

The OPA124 is a precision monolithic FET operational amplifier using a *Difet* (dielectrical isolation) manufacturing process. Outstanding DC and AC performance characteristics allow its use in the most critical instrumentation applications.

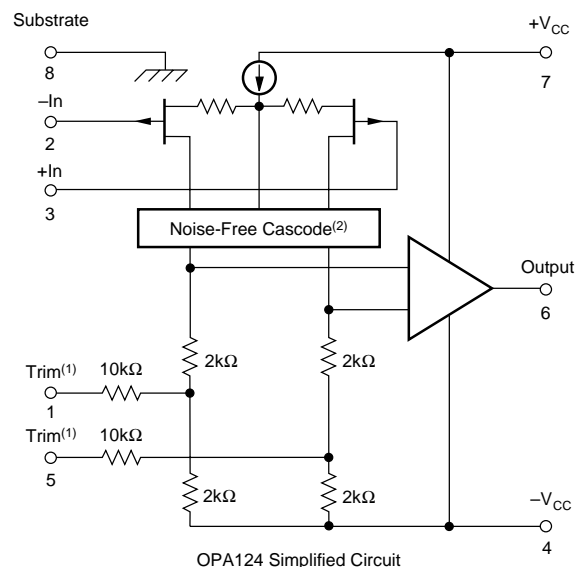
Bias current, noise, voltage offset, drift, open-loop gain, common-mode rejection and power supply rejection are superior to BIFET and CMOS amplifiers. *Difet* fabrication achieves extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry. This cascode design also allows high precision input specifications and reduced susceptibility to flicker noise. Laser trimming of thin-film resistors gives very low offset and drift.

Compared to the popular OPA111, the OPA124 gives comparable performance and is available in an 8-pin PDIP and 8-pin SOIC package.

BIFET[®] National Semiconductor Corp.,
Difet[®] Burr-Brown Corp.

APPLICATIONS

- **PRECISION PHOTODIODE PREAMP**
- **MEDICAL EQUIPMENT**
- **OPTOELECTRONICS**
- **DATA ACQUISITION**
- **TEST EQUIPMENT**



NOTES: (1) Omitted on SOIC. (2) Patented.

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Internet: <http://www.burr-brown.com/> • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

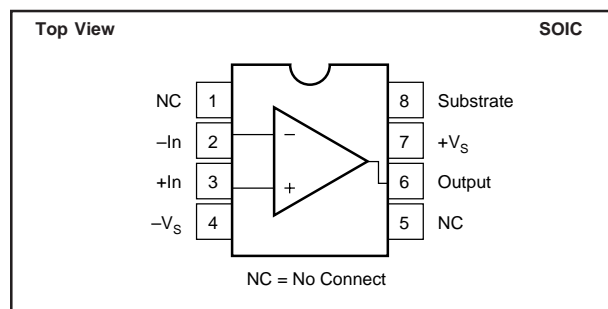
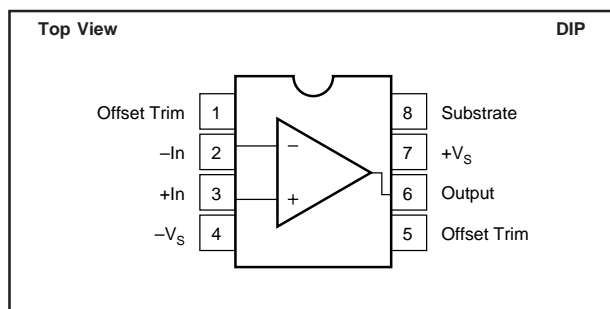
At $V_{CC} = \pm 15\text{VDC}$ and $T_A = +25^\circ\text{C}$, unless otherwise noted.

PARAMETER	CONDITION	OPA124U, P			OPA124UA, PA			OPA124PB			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
INPUT NOISE Voltage, $f_o = 10\text{Hz}^{(4)}$ $f_o = 100\text{Hz}^{(4)}$ $f_o = 1\text{kHz}^{(4)}$ $f_o = 10\text{kHz}^{(5)}$ $f_B = 10\text{Hz to } 10\text{kHz}^{(5)}$ $f_B = 0.1\text{Hz to } 10\text{Hz}$ Current, $f_B = 0.1\text{Hz to } 10\text{Hz}$ $f_o = 0.1\text{Hz thru } 20\text{kHz}$			40	80		*	*		*	*	$\text{nV}/\sqrt{\text{Hz}}$	
				15	40		*	*		*	*	$\text{nV}/\sqrt{\text{Hz}}$
				8	15		*	*		*	*	$\text{nV}/\sqrt{\text{Hz}}$
				6	8		*	*		*	*	$\text{nV}/\sqrt{\text{Hz}}$
				0.7	1.2		*	*		*	*	μVrms
				1.6	3.3		*	*		*	*	$\mu\text{Vp-p}$
			9.5	15		*	*		*	*	fAp-p	
			0.5	0.8		*	*		*	*	$\text{fA}/\sqrt{\text{Hz}}$	
OFFSET VOLTAGE ⁽¹⁾ Input Offset Voltage vs Temperature Supply Rejection vs Temperature	$V_{CM} = 0\text{VDC}$ $T_A = T_{MIN}$ to T_{MAX} $V_{CC} = \pm 10\text{V}$ to $\pm 18\text{V}$ $T_A = T_{MIN}$ to T_{MAX}		± 200	± 800		± 150	± 500		± 100	± 250	μV	
				± 4	± 7.5		± 2	± 4		± 1	± 2	$\mu\text{V}/^\circ\text{C}$
		88	110		90	*		100	*			dB
		84	100		86	*		90	*		dB	
BIAS CURRENT ⁽¹⁾ Input Bias Current	$V_{CM} = 0\text{VDC}$		± 1	± 5		± 0.5	± 2		± 0.35	± 1	pA	
OFFSET CURRENT ⁽¹⁾ Input Offset Current	$V_{CM} = 0\text{VDC}$		± 1	± 5		± 0.5	± 1		± 0.25	± 0.5	pA	
IMPEDANCE Differential Common-Mode			$10^{13} \parallel 1$			*			*		$\Omega \parallel \text{pF}$	
			$10^{14} \parallel 3$			*			*		$\Omega \parallel \text{pF}$	
VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection vs Temperature	$V_{IN} = \pm 10\text{VDC}$ $T_A = T_{MIN}$ to T_{MAX}	± 10	± 11		*	*		*	*		V	
		92	110		94	*		100	*		dB	
		86	100		*	*		90	*		dB	
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	106	125		*	*		120	*		dB	
FREQUENCY RESPONSE Unity Gain, Small Signal Full Power Response Slew Rate THD Settling Time, 0.1% 0.01% Overload Recovery, 50% Overdrive ⁽²⁾	20Vp-p , $R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$ Gain = -1 , $R_L = 2\text{k}\Omega$ 10V Step Gain = -1		1.5			*			*		MHz	
		16	32		*	*		*	*		kHz	
		1	1.6		*	*		*	*		$\text{V}/\mu\text{s}$	
			0.0003		*	*		*	*		%	
			6		*	*		*	*		μs	
			10		*	*		*	*		μs	
			5		*	*		*	*		μs	
RATED OUTPUT Voltage Output Current Output Output Resistance Load Capacitance Stability Short Circuit Current	$R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{VDC}$ DC, Open Loop Gain = $+1$	± 11	± 12		*	*		*	*		V	
		± 5.5	± 10		*	*		*	*		mA	
			100			*				*		Ω
			1000			*				*		pF
		10	40		*	*		*	*			mA
POWER SUPPLY Rated Voltage Voltage Range, Derated Current, Quiescent	$I_O = 0\text{mADC}$		± 15		*	*		*	*		VDC	
		± 5		± 18	*	*	*	*	*	*	VDC	
			2.5	3.5	*	*	*	*	*	*	mA	
TEMPERATURE RANGE Specification Storage θ Junction-Ambient: PDIP SOIC	T_{MIN} and T_{MAX}	-25		+85	*	*		*	*		$^\circ\text{C}$	
		-65		+125	*	*		*	*		$^\circ\text{C}$	
			90			*			*		$^\circ\text{C}/\text{W}$	
			100			*			*		$^\circ\text{C}/\text{W}$	

* Specification same as OPA124U, P

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up. For performance at other temperatures see Typical Performance Curves. (2) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (3) For performance at other temperatures see Typical Performance Curves. (4) Sample tested, 98% confidence. (5) Guaranteed by design.

CONNECTION DIAGRAMS



PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE	BIAS CURRENT pA, max	OFFSET DRIFT $\mu\text{V}/^\circ\text{C}$, max
OPA124U	8-Lead SOIC	182	-25°C to +85°C	5	7.5
OPA124P	8-Pin Plastic DIP	006	-25°C to +85°C	5	7.5
OPA124UA	8-Lead SOIC	182	-25°C to +85°C	2	4
OPA124PA	8-Pin Plastic DIP	006	-25°C to +85°C	2	4
OPA124PB	8-Pin Plastic DIP	006	-25°C to +85°C	1	2

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply	$\pm 18\text{VDC}$
Internal Power Dissipation ⁽²⁾	750mW
Differential Input Voltage ⁽³⁾	$\pm 36\text{VDC}$
Input Voltage Range ⁽³⁾	$\pm 18\text{VDC}$
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit Duration ⁽⁴⁾	Continuous
Junction Temperature	+175°C

NOTES: (1) Stresses above these ratings may cause permanent damage.
 (2) Packages must be derated based on $\theta_{JA} = 90^\circ\text{C}/\text{W}$ for PDIP and $100^\circ\text{C}/\text{W}$ for SOIC. (3) For supply voltages less than $\pm 18\text{VDC}$, the absolute maximum input voltage is equal to $+18\text{V} > V_{IN} > -V_{CC} - 6\text{V}$. See Figure 2. (4) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J .



ELECTROSTATIC DISCHARGE SENSITIVITY

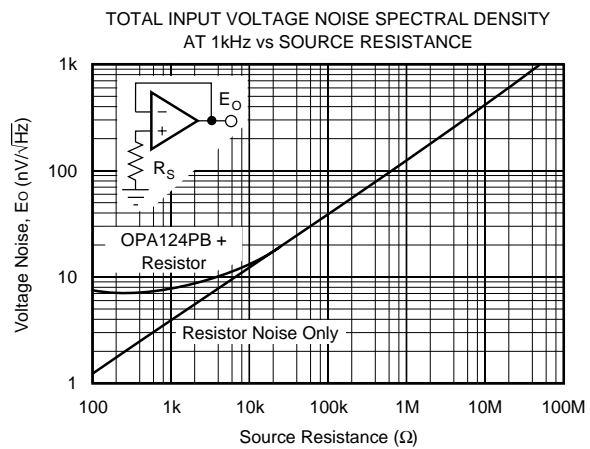
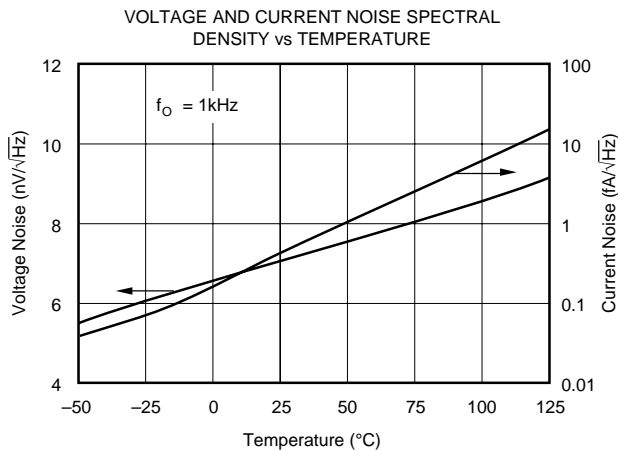
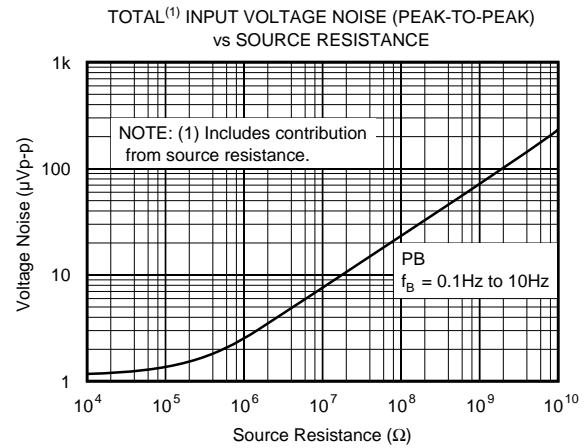
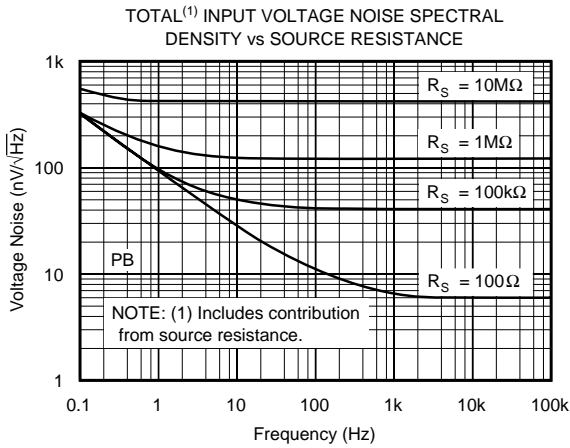
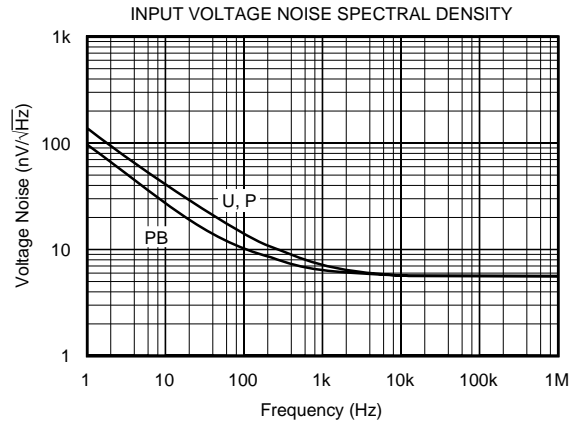
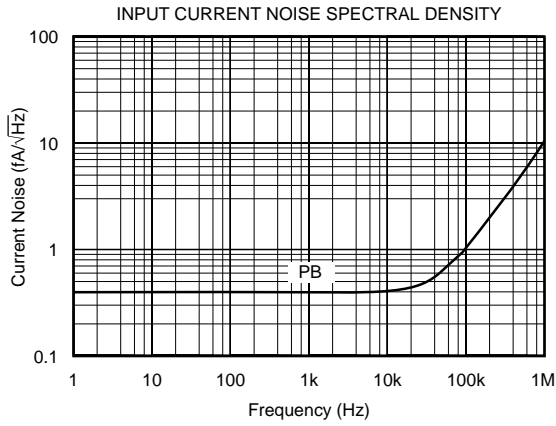
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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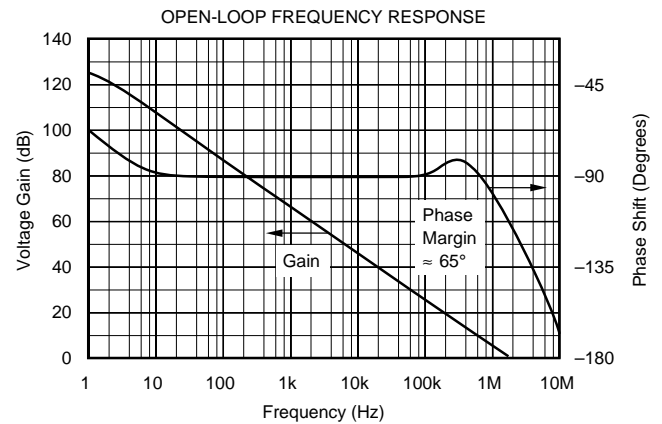
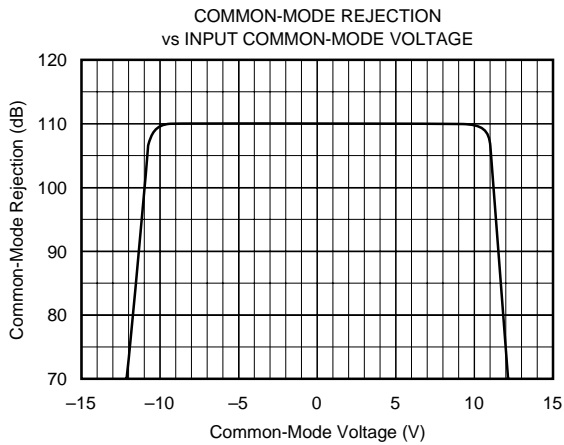
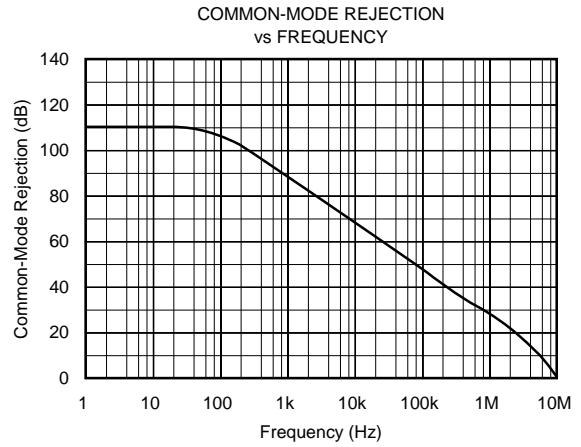
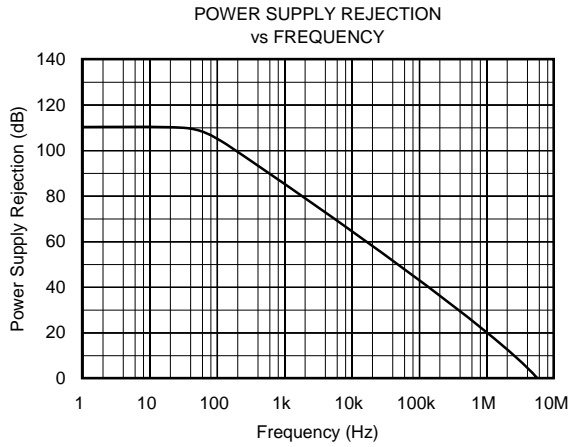
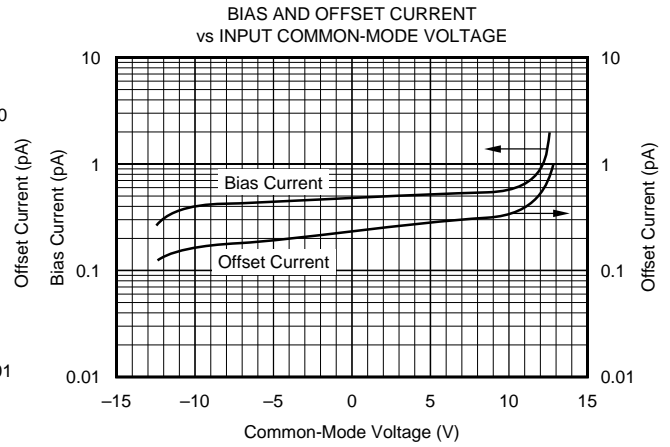
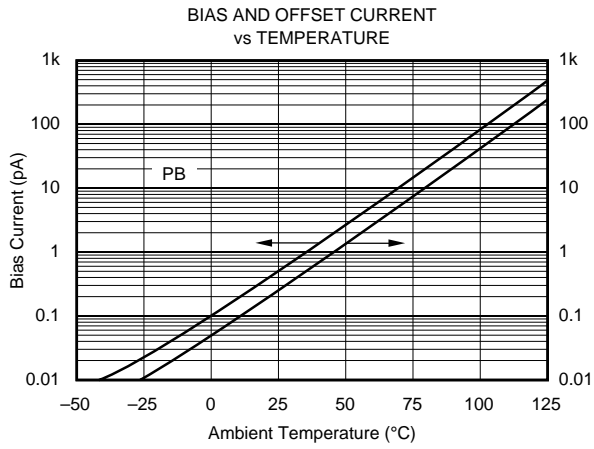
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, and $V_{CC} = \pm 15\text{VDC}$, unless otherwise noted.



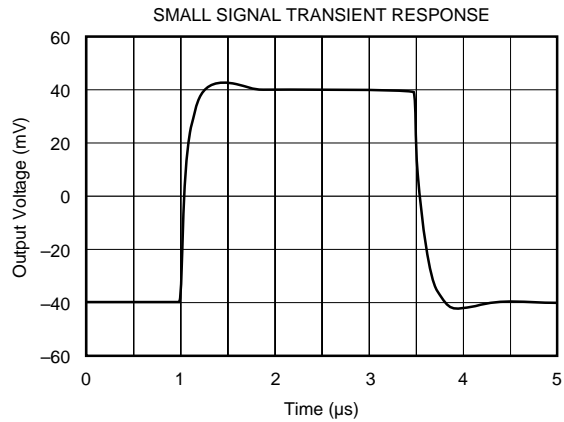
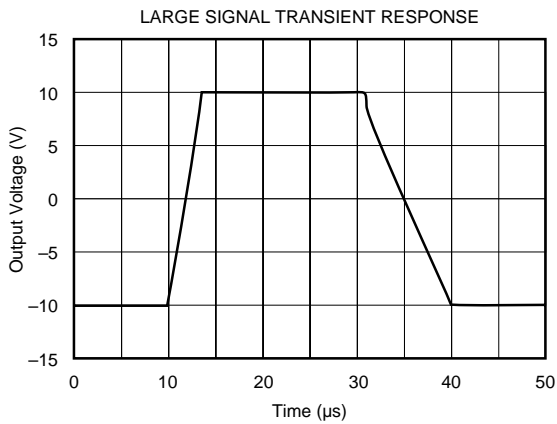
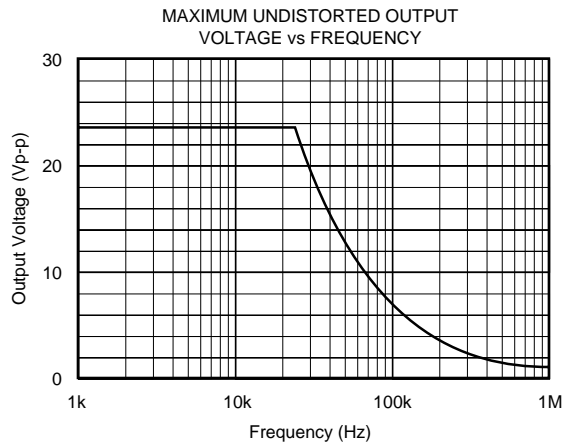
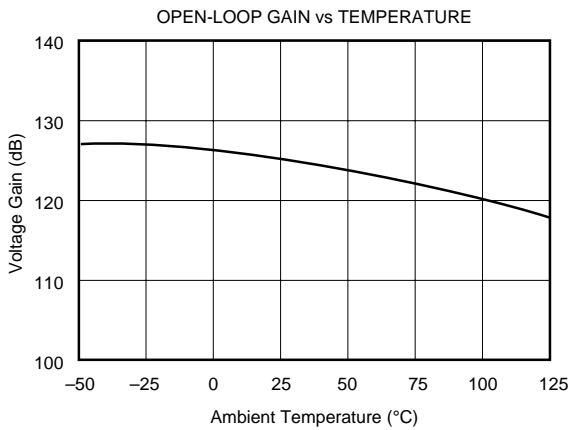
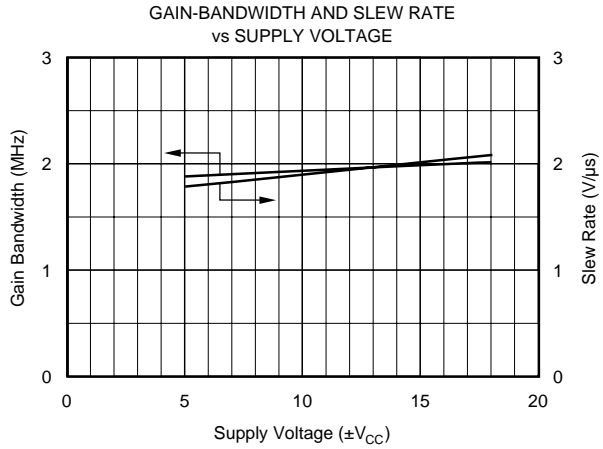
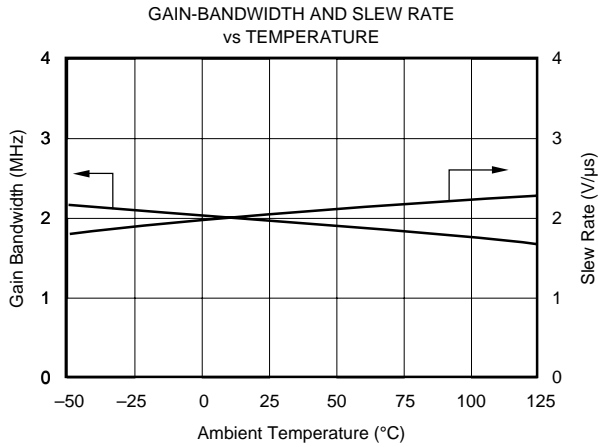
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, and $V_{CC} = \pm 15\text{VDC}$, unless otherwise noted.



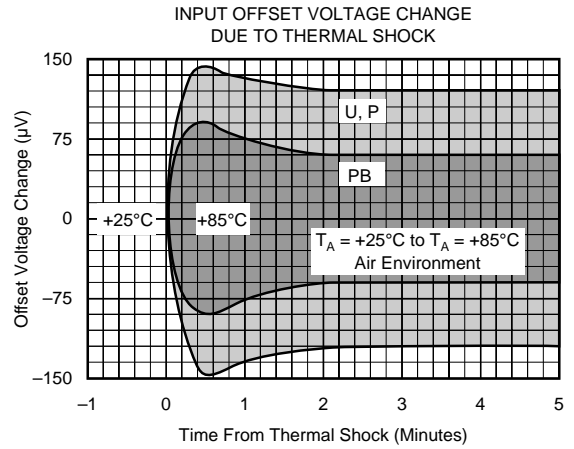
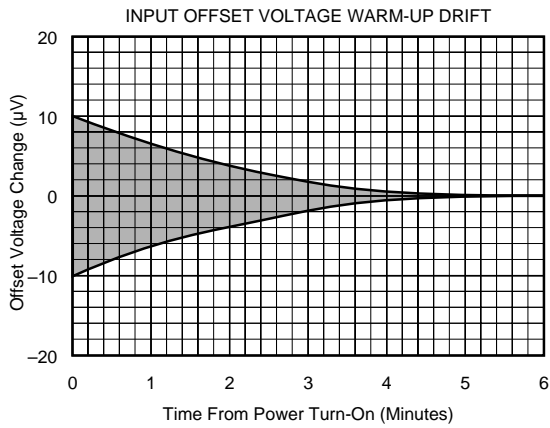
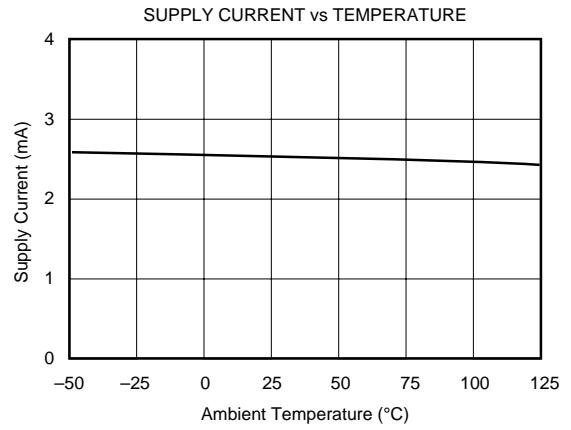
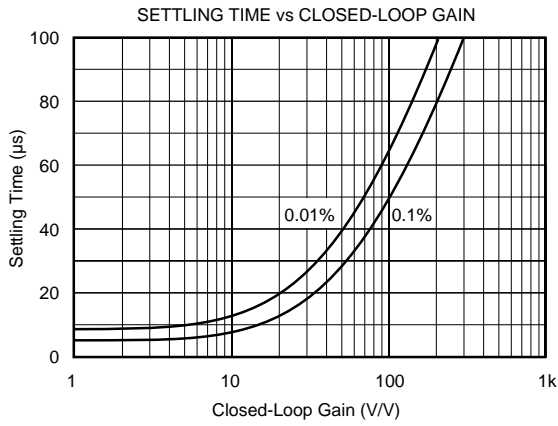
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, and $V_{CC} = \pm 15\text{VDC}$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, and $V_{CC} = \pm 15\text{VDC}$, unless otherwise noted.



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA124 offset voltage is laser-trimmed and will require no further trim for most applications. In order to reduce layout leakage errors, the offset adjust capability has been removed from the SOIC versions (OPA124UA and OPA124U). The PDIP versions (OPA124PB, OPA124PA, and OPA124P) do have pins available for offset adjustment. As with most amplifiers, externally trimming the remaining offset can change drift performance by about $0.3\mu\text{V}/^\circ\text{C}$ for each $100\mu\text{V}$ of adjusted offset. The correct circuit configuration for offset adjust for the PDIP packages is shown in Figure 1.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

Unlike BIFET amplifiers, the *Difet* OPA124 requires input current limiting resistors only if its input voltage is greater than 6V more negative than $-V_{CC}$. A $10\text{k}\Omega$ series resistor will limit input current to a safe level with up to $\pm 15\text{V}$ input levels, even if both supply voltages are lost (Figure 2).

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift. Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce “hum” pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA124. To avoid leakage problems, the OPA124 should be soldered directly into a printed circuit board. Utmost care must be used in planning the board layout. A “guard” pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier substrate should be connected to any input shield or guard via pin 8 minimizing both leakage and noise pickup (see Figure 3).

If guarding is not required, pin 8 should be connected to ground.

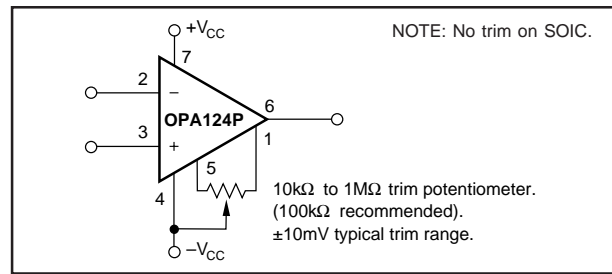


FIGURE 1. Offset Voltage Trim for PDIP packages.

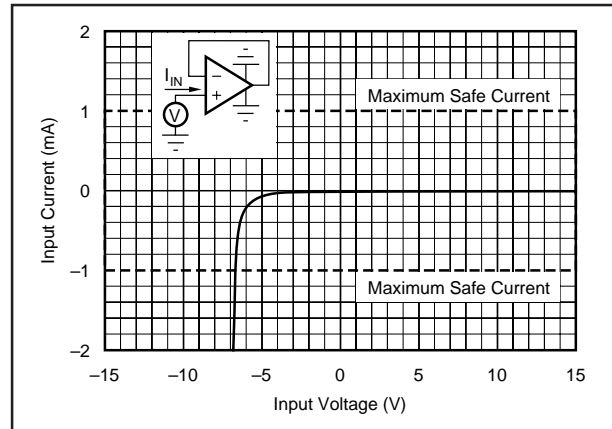


FIGURE 2. Input Current vs Input Voltage with $\pm V_{CC}$ Pins Grounded.

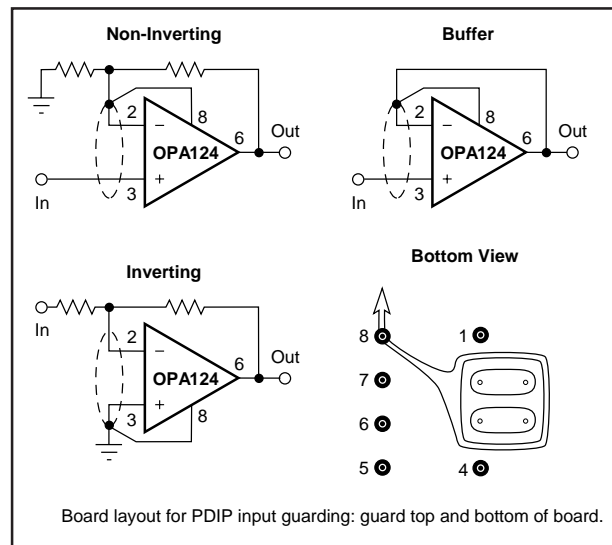


FIGURE 3. Connection of Input Guard.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
OPA124P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA124PA	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA124PA2	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA124PB	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA124U	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA124U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA124U/2K5E4	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA124U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA124UA	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA124UA/2K5	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA124UA/2K5E4	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA124UAE4	ACTIVE	SOIC	D	8	100	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA124UAG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA124UE4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA124UG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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