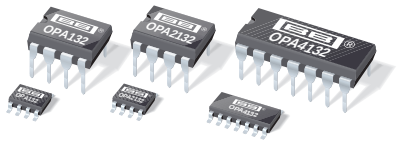
Burr-Brown Products
from Texas Instruments



OPA132
OPA2132
OPA4132

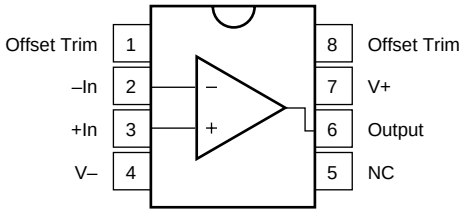
SBOS054A – JANUARY 1995 – REVISED JUNE 2004

High-Speed
FET-INPUT OPERATIONAL AMPLIFIERS

FEATURES

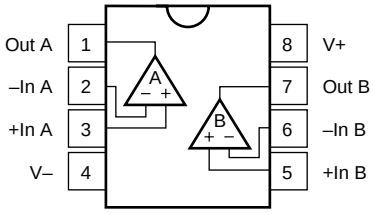
- **FET INPUT: I_B = 50pA max**
- **WIDE BANDWIDTH: 8MHz**
- **HIGH SLEW RATE: 20V/μs**
- **LOW NOISE: 8nV/√Hz (1kHz)**
- **LOW DISTORTION: 0.00008%**
- **HIGH OPEN-LOOP GAIN: 130dB (600Ω load)**
- **WIDE SUPPLY RANGE: ±2.5 to ±18V**
- **LOW OFFSET VOLTAGE: 500μV max**
- **SINGLE, DUAL, AND QUAD VERSIONS**

OPA132



8-Pin DIP, SO-8

OPA2132



8-Pin DIP, SO-8

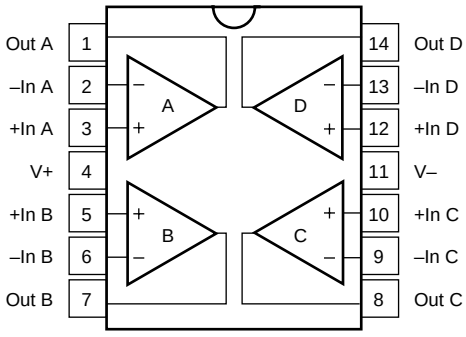
DESCRIPTION

The OPA132 series of FET-input op amps provides high-speed and excellent dc performance. The combination of high slew rate and wide bandwidth provide fast settling time. Single, dual, and quad versions have identical specifications for maximum design flexibility. High performance grades are available in the single and dual versions. All are ideal for general-purpose, audio, data acquisition and communications applications, especially where high source impedance is encountered.

OPA132 op amps are easy to use and free from phase inversion and overload problems often found in common FET-input op amps. Input cascode circuitry provides excellent common-mode rejection and maintains low input bias current over its wide input voltage range. OPA132 series op amps are stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions, including high load capacitance. Dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

Single and dual versions are available in 8-pin DIP and SO-8 surface-mount packages. Quad is available in 14-pin DIP and SO-14 surface-mount packages. All are specified for –40°C to +85°C operation.

OPA4132



14-Pin DIP
SO-14

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to V–	36V
Input Voltage	(V–) –0.7V to (V+) +0.7V
Output Short-Circuit[1]	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

NOTE: (1) Short-circuit to ground, one amplifier per package.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SPECIFICATIONS

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

PARAMETER	CONDITION	OPA132P, U OPA2132P, U			OPA132PA, UA OPA2132PA, UA OPA4132PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE								
Input Offset Voltage			±0.25	±0.5		±0.5	±2	mV
vs Temperature[1]	Operating Temperature Range		±2	±10		*	*	µV/°C
vs Power Supply	V_S = ±2.5V to ±18V		5	15		*	30	µV/V
Channel Separation (dual and quad)	R_L = 2kΩ		0.2			*		µV/V
INPUT BIAS CURRENT								
Input Bias Current[2]	V_{CM} = 0V		+5	±50		*	*	pA
vs Temperature			See Typical Curve			*		
Input Offset Current[2]	V_{CM} = 0V		±2	±50		*	*	pA
NOISE								
Input Voltage Noise								
Noise Density, f = 10Hz			23			*		nV/√Hz
f = 100Hz			10			*		nV/√Hz
f = 1kHz			8			*		nV/√Hz
f = 10kHz			8			*		nV/√Hz
Current Noise Density, f = 1kHz			3			*		fA/√Hz
INPUT VOLTAGE RANGE								
Common-Mode Voltage Range		(V–)+2.5	±13	(V+)–2.5	*	*	*	V
Common-Mode Rejection	V_{CM} = –12.5V to +12.5V	96	100		86	94		dB
INPUT IMPEDANCE								
Differential			10^{13} || 2			*		Ω || pF
Common-Mode	V_{CM} = –12.5V to +12.5V		10^{13} || 6			*		Ω || pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	R_L = 10kΩ, V_O = –14.5V to +13.8V	110	120		104	*		dB
	R_L = 2kΩ, V_O = –13.8V to +13.5V	110	126		104	120		dB
	R_L = 600Ω, V_O = –12.8V to +12.5V	110	130		104	120		dB
FREQUENCY RESPONSE								
Gain-Bandwidth Product			8			*		MHz
Slew Rate			±20			*		V/µs
Settling Time: 0.1%	G = –1, 10V Step, C_L = 100pF		0.7			*		µs
0.01%	G = –1, 10V Step, C_L = 100pF		1			*		µs
Overload Recovery Time	G = ±1		0.5			*		µs
Total Harmonic Distortion + Noise	1kHz, G = 1, V_O = 3.5Vrms							
	R_L = 2kΩ		0.00008			*		%
	R_L = 600Ω		0.00009			*		%
OUTPUT								
Voltage Output, Positive	R_L = 10kΩ	(V+)–1.2	(V+)–0.9		*	*		V
Negative		(V–)+0.5	(V–)+0.3		*	*		V
Positive	R_L = 2kΩ	(V+)–1.5	(V+)–1.2		*	*		V
Negative		(V–)+1.2	(V–)+0.9		*	*		V
Positive	R_L = 600Ω	(V+)–2.5	(V+)–2.0		*	*		V
Negative		(V–)+2.2	(V–)+1.9		*	*		V
Short-Circuit Current			±40			*		mA
Capacitive Load Drive (Stable Operation)			See Typical Curve			*		
POWER SUPPLY								
Specified Operating Voltage			±15			*		V
Operating Voltage Range		±2.5		±18	*		*	V
Quiescent Current (per amplifier)	I_O = 0		±4	±4.8		*	*	mA
TEMPERATURE RANGE								
Operating Range		–40		+85	*		*	°C
Storage		–40		+125	*		*	°C
Thermal Resistance, θ_{JA}								
8-Pin DIP			100			*		°C/W
SO-8 Surface-Mount			150			*		°C/W
14-Pin DIP			80			*		°C/W
SO-14 Surface-Mount			110			*		°C/W

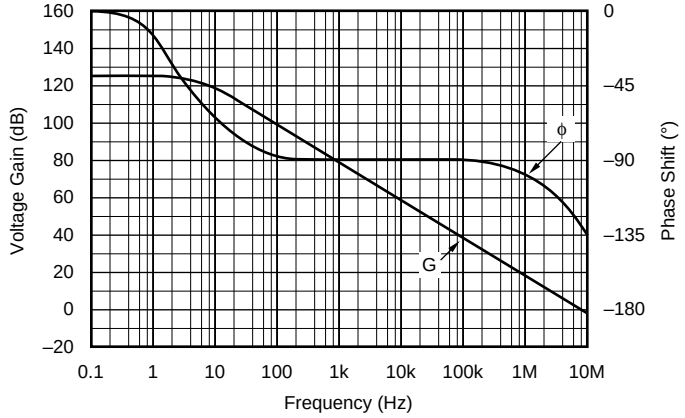
* Specifications same as OPA132P, OPA132U.

NOTES: (1) Guaranteed by wafer test. (2) High-speed test at T_J = 25°C.

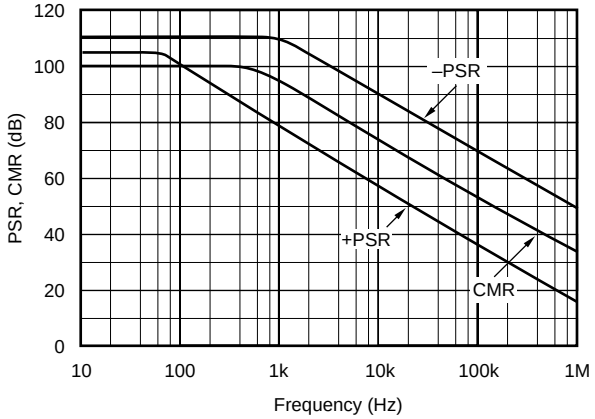
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V, R_L = 2kΩ, unless otherwise noted.

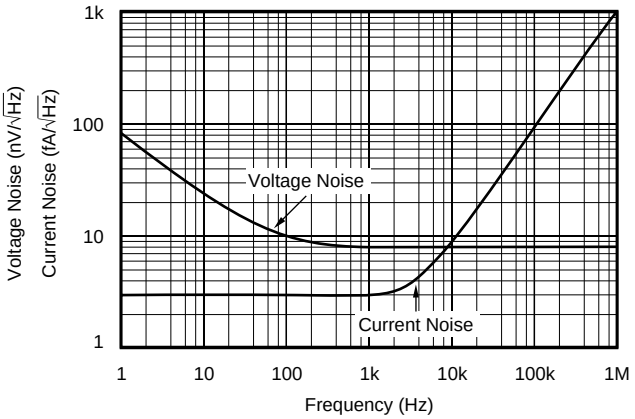
OPEN-LOOP GAIN/PHASE vs FREQUENCY



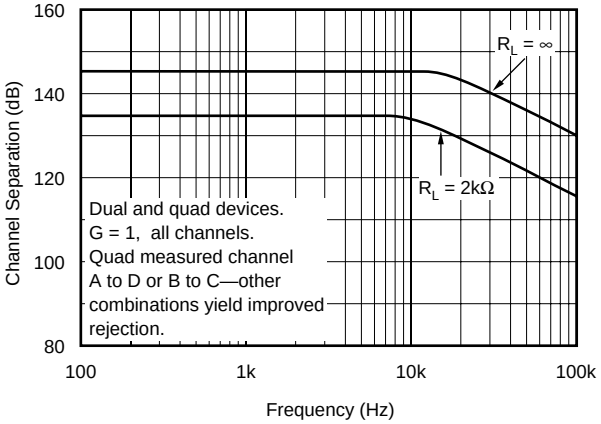
POWER SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY



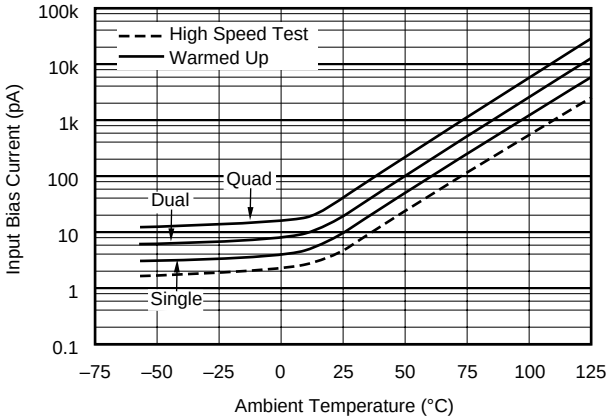
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



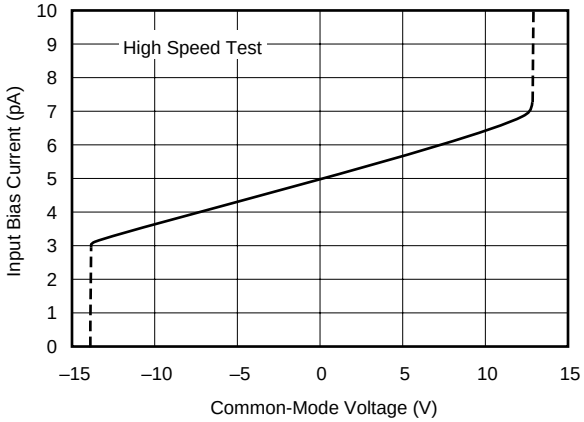
CHANNEL SEPARATION vs FREQUENCY



INPUT BIAS CURRENT vs TEMPERATURE



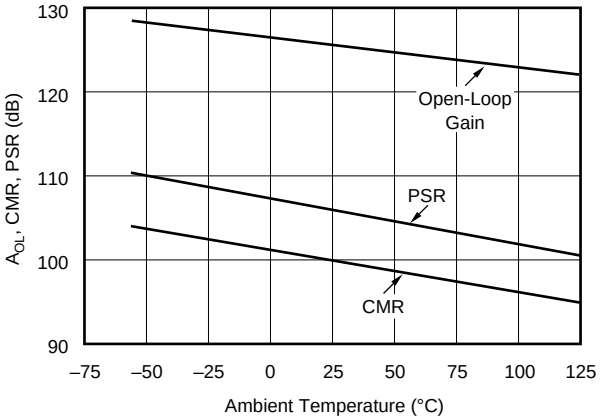
INPUT BIAS CURRENT vs INPUT COMMON-MODE VOLTAGE



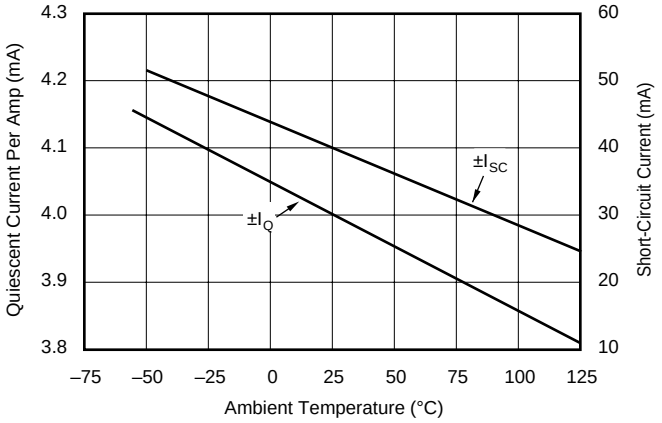
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_S = ±15V, R_L = 2kΩ, unless otherwise noted.

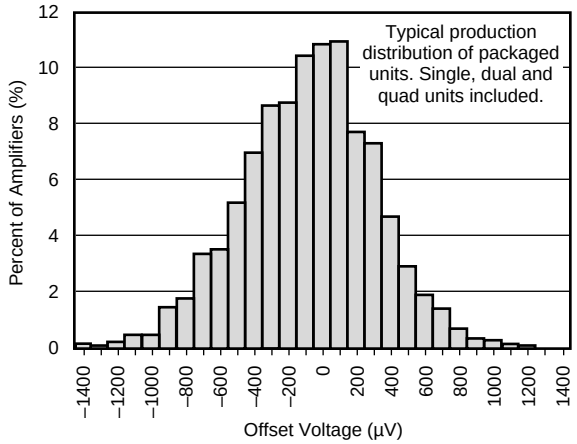
A_{OL}, CMR, PSR vs TEMPERATURE



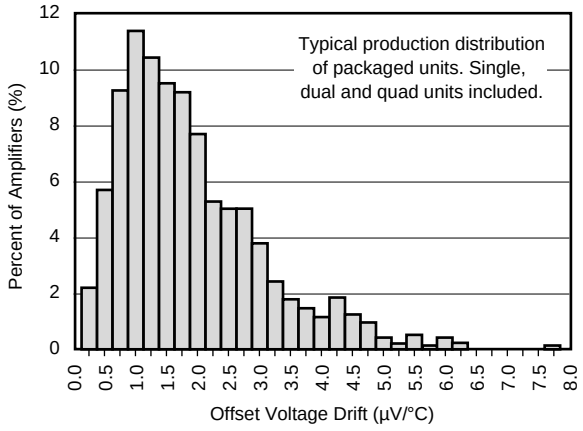
QUIESCENT CURRENT AND SHORT-CIRCUIT CURRENT vs TEMPERATURE



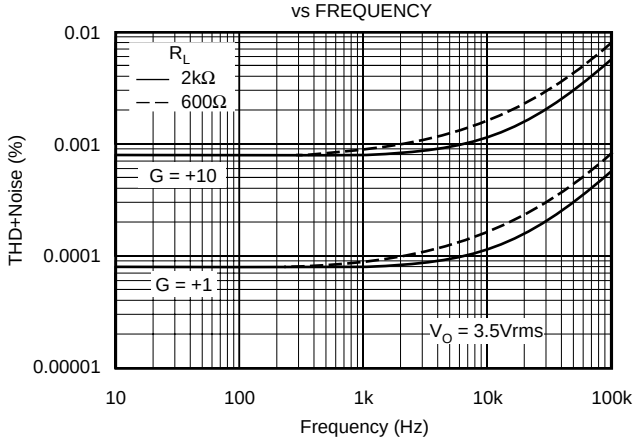
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



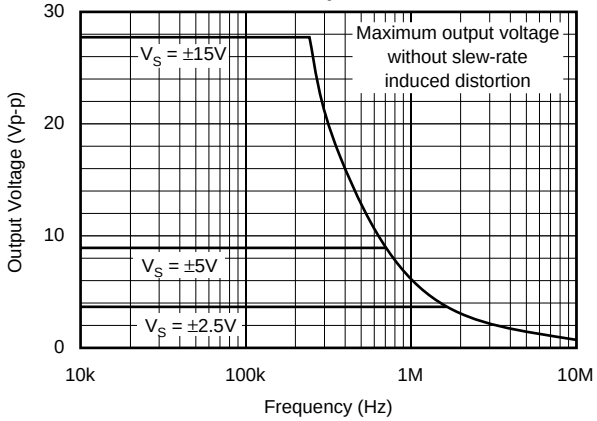
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



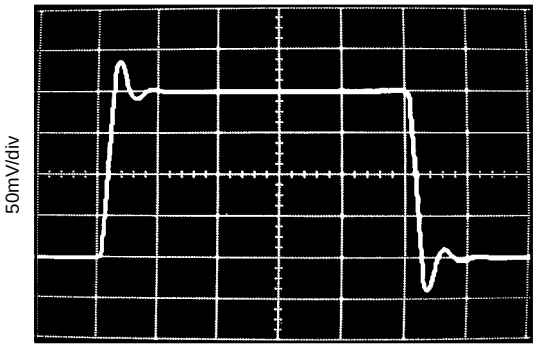
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



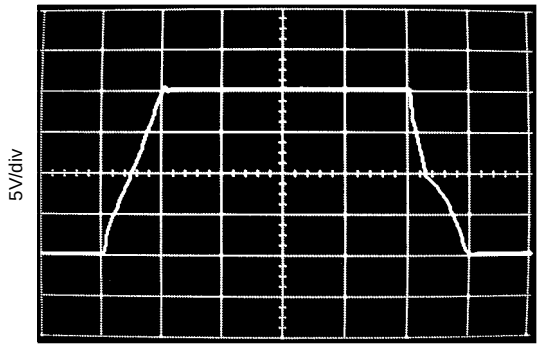
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_S = ±15V, R_L = 2kΩ, unless otherwise noted.

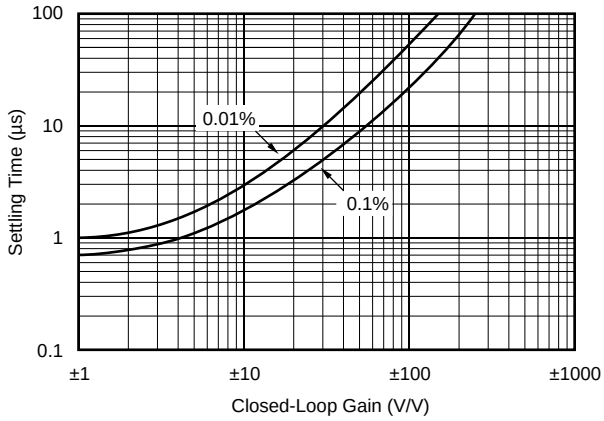
SMALL-SIGNAL STEP RESPONSE
G = 1, C_L = 100pF



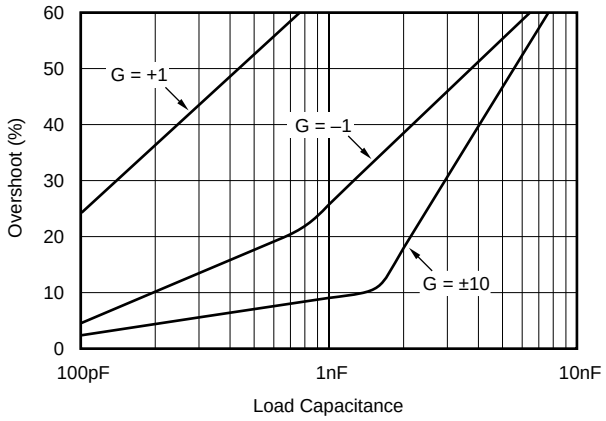
LARGE-SIGNAL STEP RESPONSE
G = 1, C_L = 100pF



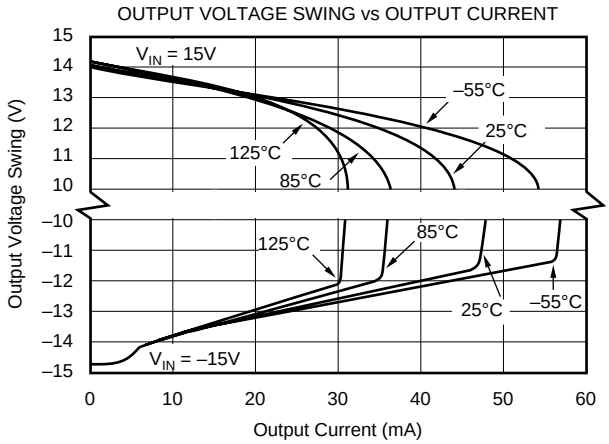
SETTLING TIME vs CLOSED-LOOP GAIN



SMALL-SIGNAL OVERSHOOT
vs LOAD CAPACITANCE



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



APPLICATIONS INFORMATION

OPA132 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power supply pins should be bypassed with 10nF ceramic capacitors or larger.

OPA132 op amps are free from unexpected output phase-reversal common with FET op amps. Many FET-input op amps exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control loop applications. OPA132 series op amps are free from this undesirable behavior. All circuitry is completely independent in dual and quad versions, assuring normal behavior when one amplifier in a package is overdriven or short-circuited.

OPERATING VOLTAGE

OPA132 series op amps operate with power supplies from ±2.5V to ±18V with excellent performance. Although specifications are production tested with ±15V supplies, most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the typical performance curves.

OFFSET VOLTAGE TRIM

Offset voltage of OPA132 series amplifiers is laser trimmed and usually requires no user adjustment. The OPA132 (single op amp version) provides offset voltage trim connections on pins 1 and 8. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset could degrade the offset voltage drift behavior of the op amp. While it is not possible to predict the exact change in drift, the effect is usually small.

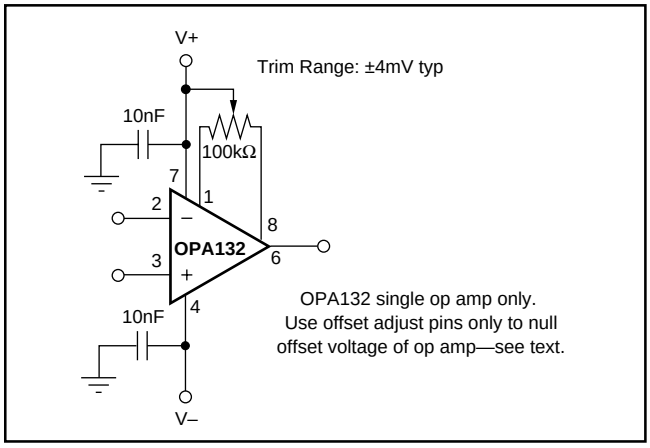


FIGURE 1. OPA132 Offset Voltage Trim Circuit.

INPUT BIAS CURRENT

The FET-inputs of the OPA132 series provide very low input bias current and cause negligible errors in most applications. For applications where low input bias current is crucial, junction temperature rise should be minimized. The input bias current of FET-input op amps increases with temperature as shown in the typical performance curve "Input Bias Current vs Temperature."

The OPA132 series may be operated at reduced power supply voltage to minimize power dissipation and temperature rise. Using ±3V supplies reduces power dissipation to one-fifth that at ±15V.

The dual and quad versions have higher total power dissipation than the single, leading to higher junction temperature. Thus, a warmed-up quad will have higher input bias current than a warmed-up single. Furthermore, an SOIC will generally have higher junction temperature than a DIP at the same ambient temperature because of a larger θ_{JA}. Refer to the specifications table.

Circuit board layout can also help minimize junction temperature rise. Temperature rise can be minimized by soldering the devices to the circuit board rather than using a socket. Wide copper traces will also help dissipate the heat by acting as an additional heat sink.

Input stage cascode circuitry assures that the input bias current remains virtually unchanged throughout the full input common-mode range of the OPA132 series. See the typical performance curve "Input Bias Current vs Common-Mode Voltage."

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA132P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
OPA132P1	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
OPA132PA	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
OPA132PA2	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
OPA132U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 132U	Samples
OPA132U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 132U	Samples
OPA132U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 132U	Samples
OPA132U1	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
OPA132UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	Samples
OPA132UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	Samples
OPA132UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	Samples
OPA132UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	Samples
OPA132UA2	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
OPA132UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	Samples
OPA132UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	Samples
OPA132UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 132U	Samples
OPA2132P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2132P	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA2132PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2132P A	Samples
OPA2132PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2132P A	Samples
OPA2132PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2132P	Samples
OPA2132U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	Samples
OPA2132U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	Samples
OPA2132U/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	Samples
OPA2132U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	Samples
OPA2132UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 125	OPA 2132U A	Samples
OPA2132UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U A	Samples
OPA2132UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U A	Samples
OPA2132UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 125	OPA 2132U A	Samples
OPA2132UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 125	OPA 2132U A	Samples
OPA2132UE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	Samples
OPA2132UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	Samples
OPA4132PA	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI			
OPA4132UA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4132UA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA4132UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4132UA	Samples
OPA4132UA/2K5E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4132UA	Samples
OPA4132UA/2K5G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4132UA	Samples
OPA4132UAE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4132UA	Samples
OPA4132UAG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4132UA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

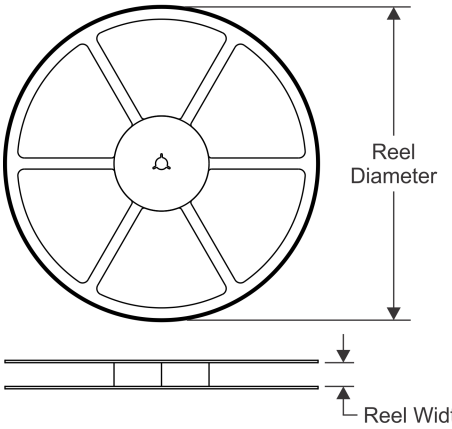
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

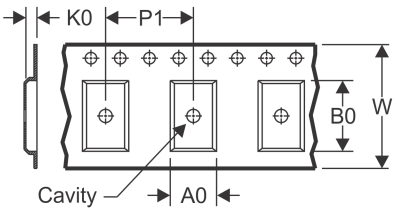
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

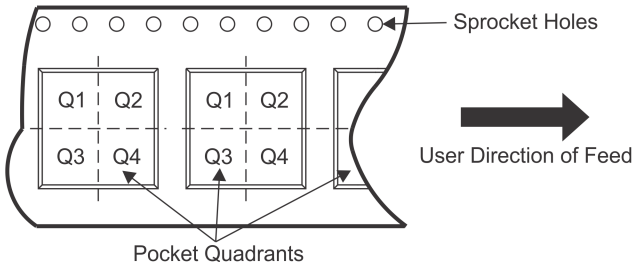


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

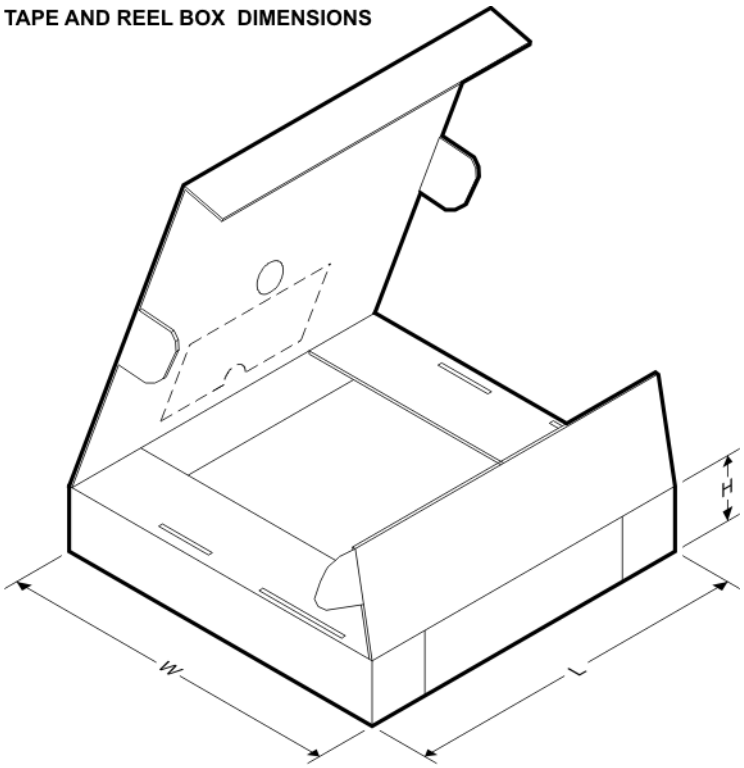
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2132UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4132UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

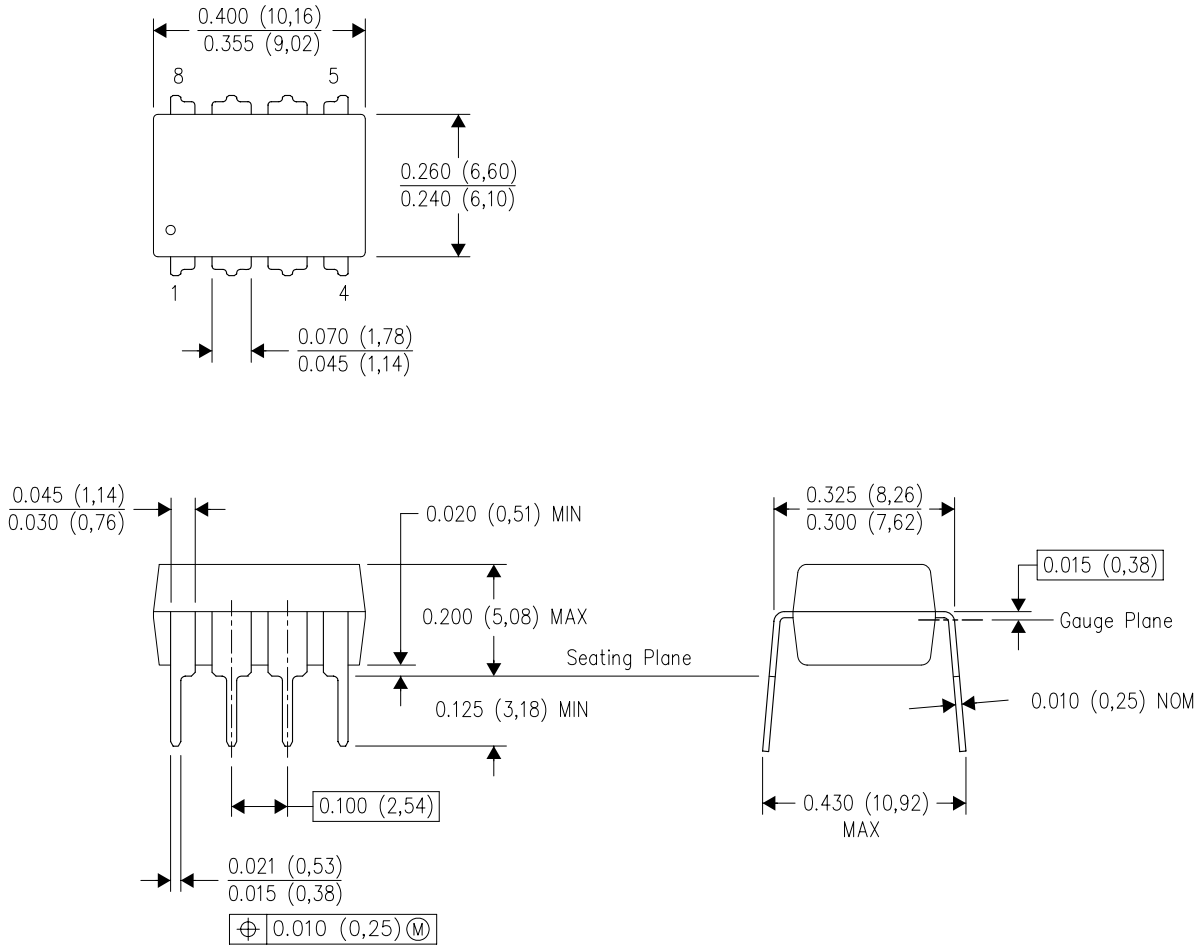
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

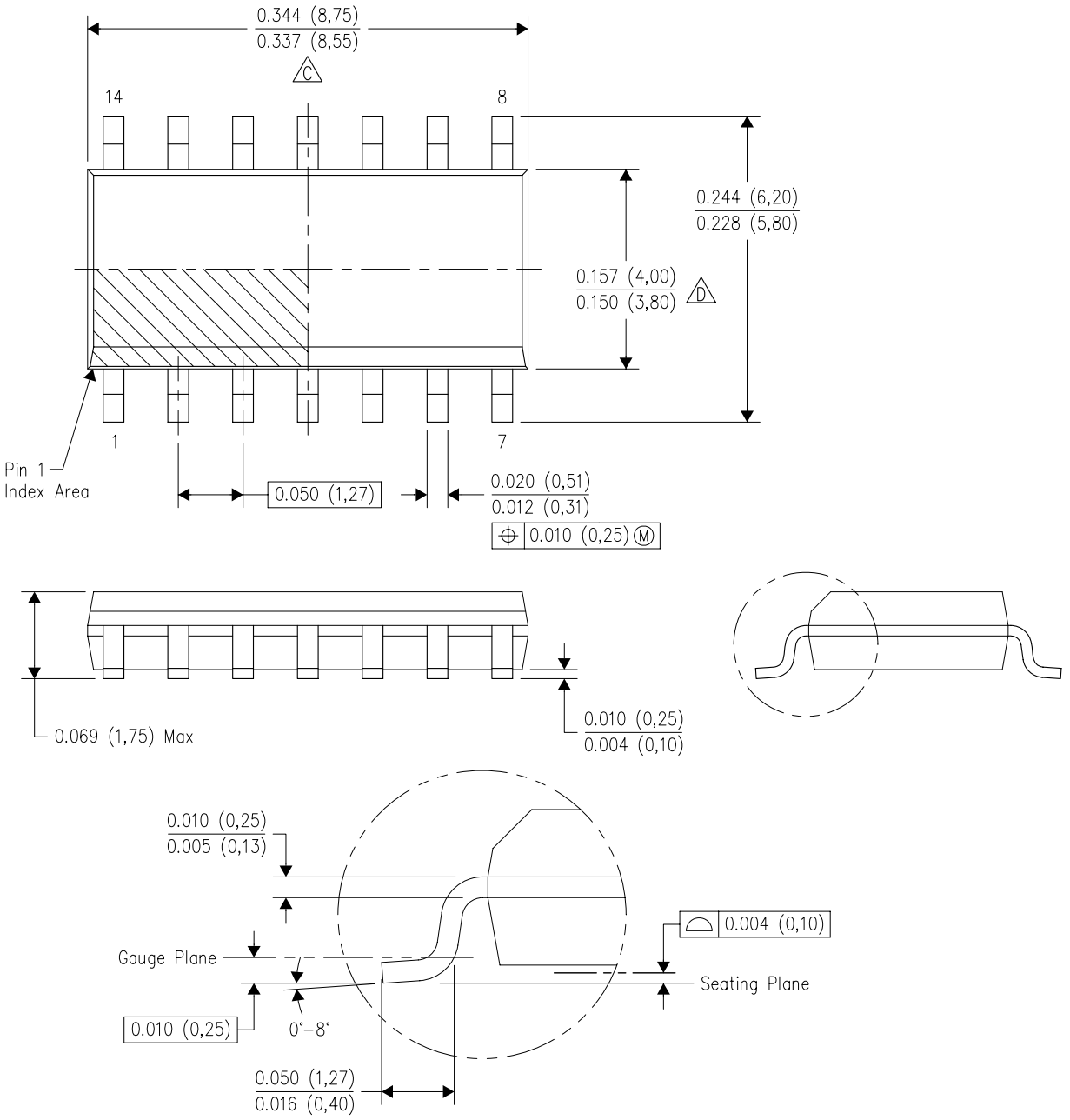
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2132UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA4132UA/2K5	SOIC	D	14	2500	367.0	367.0	38.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

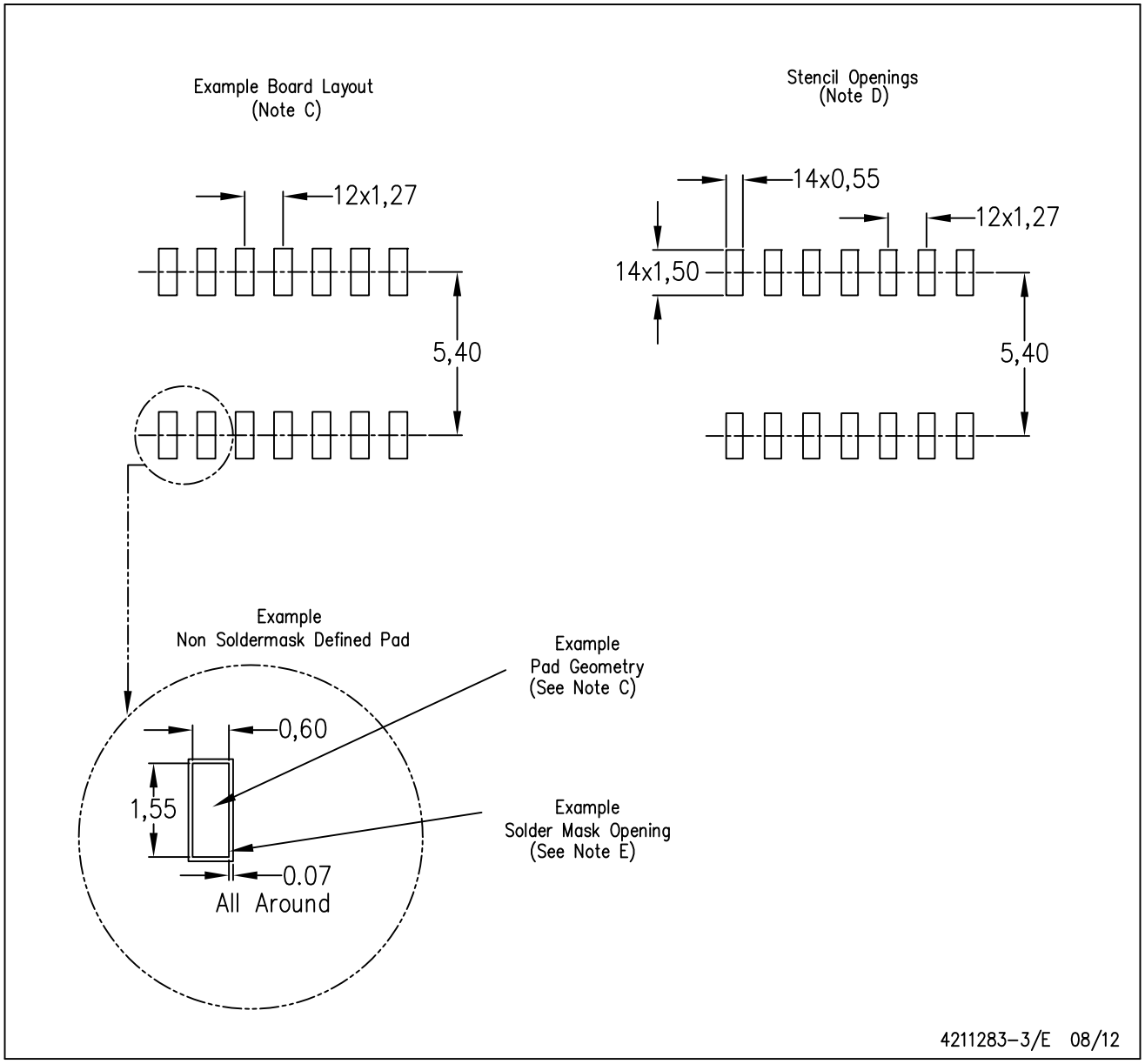
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

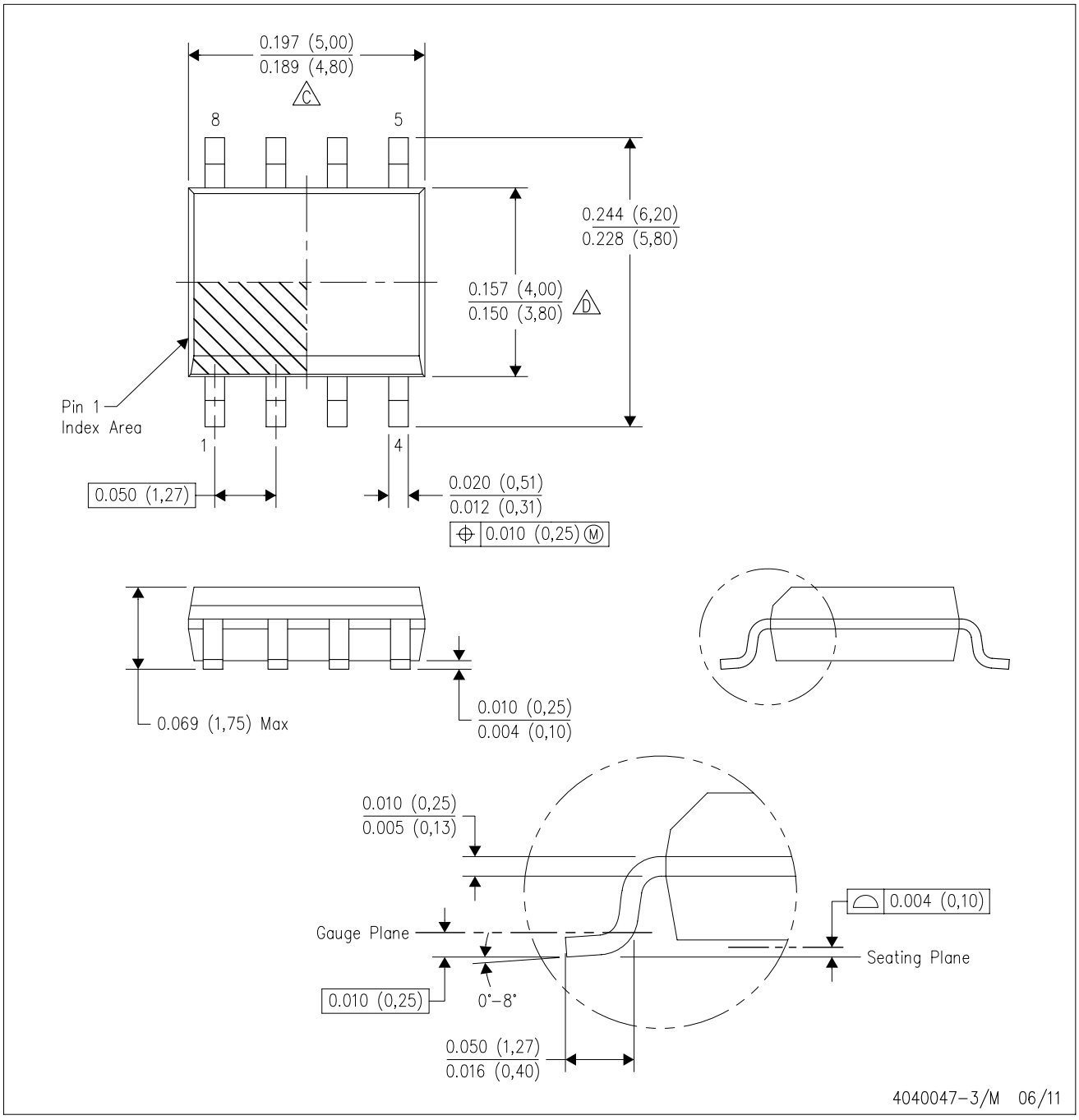
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



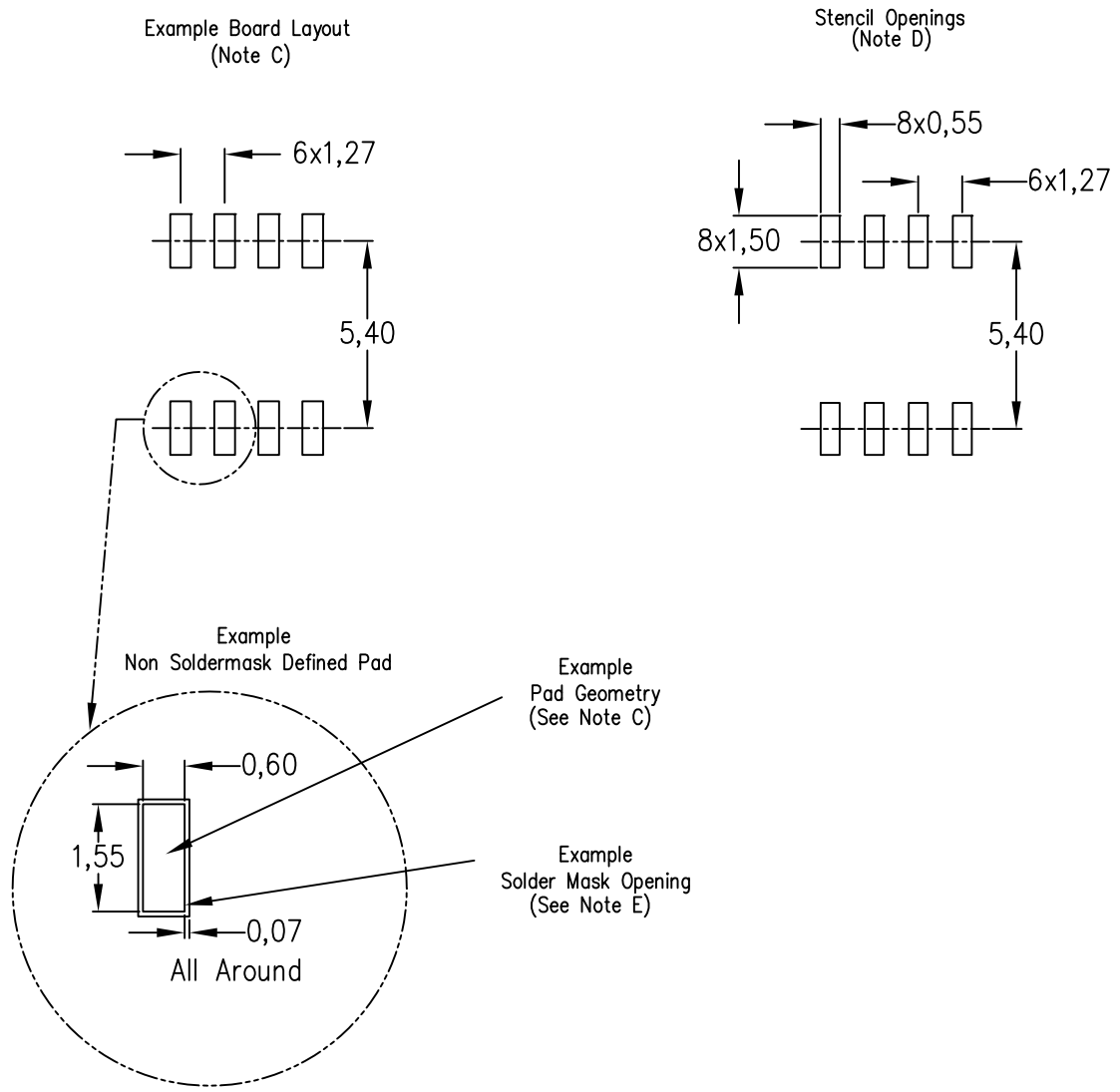
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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