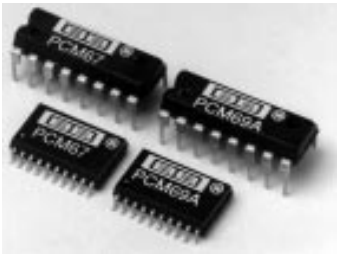
BURR - BROWN®



PCM67P/U
PCM69AP/AU

Advanced 1-Bit BiCMOS Dual 18-Bit DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **18-BIT RESOLUTION DUAL AUDIO DAC**
- **EXCELLENT THD PERFORMANCE:**
  0.0025% (–92dB) at F/S, K Grade
  1.0% (–40dB) at –60dB, K Grade
- **HIGH S/N RATIO: 110dB typ (IHF-A)**
- **DUAL, CO-PHASE**
- **SINGLE SUPPLY +5V OPERATION**
- **LOW POWER: 75mW typical**
- **CAPABLE OF 16X OVERSAMPLING**
- **AVAILABLE IN SPACE SAVING 16-PIN DIP OR 20-PIN SOIC**
- **OPERATING TEMP RANGE: –25°C to +85°C**
- **EXTREMELY LOW GLITCH ENERGY**

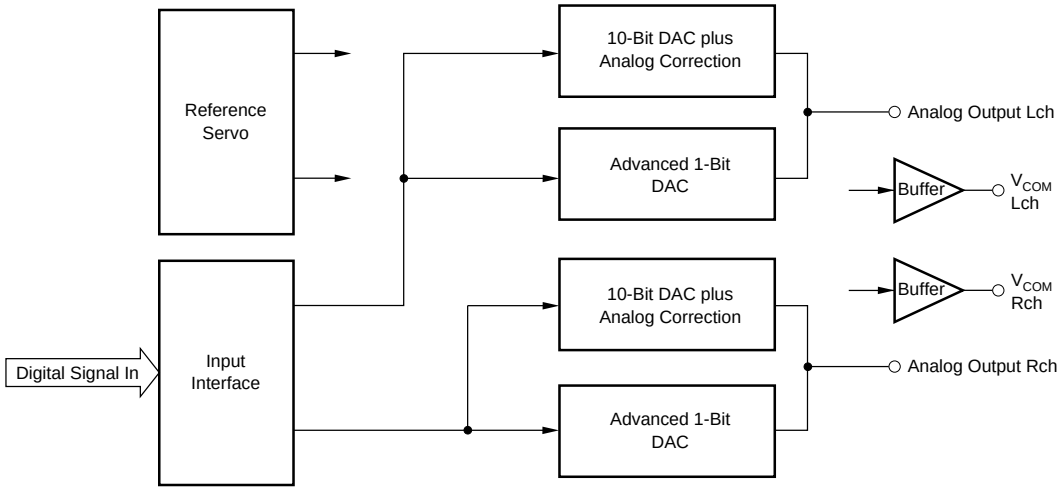
DESCRIPTION

The PCM67 and PCM69A dual 18-bit DAC are low cost, dual output 18-bit BiCMOS digital-to-analog converters utilizing a novel architecture to achieve excellent low level performance.

By combining a conventional thin-film R-2R ladder DAC, a digital offset technique with analog correction and an advanced one-bit DAC using first order noise shaping technique, the PCM67 and PCM69A achieve high resolution, minimal glitch, and low zero-crossing distortion.

PCM67 digital offset occurs at bit 9, making it ideal for high-performance CD players. PCM69A digital offset occurs at bit 4, making it an excellent choice for digital musical instruments and audio DSP.

Both PCM67 and PCM69A operate from a single +5V supply. The low power consumption and small size (16-pin PDIP or 20-pin SOIC) make these converters ideal for a variety of digital audio applications.



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PDS-1168A
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SPECIFICATIONS

ELECTRICAL

All specifications at +25°C and $+V_A$, $+V_D$ = +5V unless otherwise noted

PARAMETER	CONDITIONS	PCM67/69A MIN	PCM67/69A TYP	PCM67/69A MAX	UNITS
RESOLUTION			18		Bits
DYNAMIC RANGE, THD+N at –60dB Referred to Full Scale			106		dB
DIGITAL INPUT					
Logic Family			TTL/CMOS Compatible		
Logic Level: V_{IH}	I_{IH} = ±5µA	+2		$+V_D$	V
V_{IL}	I_{IL} = ±5µA	0		0.8	V
Data Format			Serial, MSB First, BTC[1]		
Input System Clock Frequency			16.9344		MHz
TOTAL HARMONIC DISTORTION + N[2,3,4]					
PCM67P/69AP, PCM67U/69AU					
f = 991Hz (0dB)	f_S = 352.8kHz		–86	–82	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–68		dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–40	–34	dB
PCM67P-J/69AP-J, PCM67U-J/69AU-J					
f = 991Hz (0dB)	f_S = 352.8kHz		–91	–88	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–72		dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–46	–40	dB
PCM67P-K/69AP-K, PCM67U-K/69AU-K					
f = 991Hz (0dB)	f_S = 352.8kHz		–95	–92	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–74		dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–46	–40	dB
CHANNEL SEPARATION	(f = 1kHz)		106		dB
ACCURACY					
Level Linearity	at –90dB Signal Level		±1		dB
Gain Error			±3	±10	%
Gain Mismatch, Channel-to-Channel			±1	±5	%
Gain Drift	0°C to +70°C		95		ppm/°C
Warm-up Time			1		Minute
IDLE CHANNEL SNR[5]	20Hz to 40kHz at BPZ[6]		110		dB
ANALOG OUTPUT					
Output Range (±3%)			1.2		mA
Output Impedance (±30%)			1.8		kΩ
V_{COM}		3.35	3.50	3.65	V
Glitch Energy			No Glitch Around Zero		
POWER SUPPLY REQUIREMENTS, System Clock = 16.9344MHz					
$+V_A$, $+V_D$ Supply Voltage Range	$+V_A$ = $+V_D$	+4.75	+5.00	+5.25	V
$+I_A$, $+I_D$ Combined Supply Current	$+V_A$, $+V_D$ = +5V		15	20	mA
Power Dissipation	$+V_A$, $+V_D$ = +5V		75	105	mW
TEMPERATURE RANGE					
Operating		–25		+85	°C
Storage		–55		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$)/$Signal_{RMS}$. (3) D/A converter output frequency/signal level (both left and right channels are "on"). (4) D/A converter sample frequency (8 x 44.1kHz; 8X oversampling per channel). (5) Ratio of $Noise_{RMS}$/$Signal_{RMS}$. Measured using a 40kHz 3rd-order GIC (Generalized Immittance Converter) filter and an A-weighted filter. (6) Bipolar Zero.

PIN ASSIGNMENTS

PCM67P PCM69AP	PCM67U PCM69AU	DESCRIPTION	MNEMONIC
1	1	+5V Analog Supply Voltage	$+V_A$
2	2	Left Voltage Common	LV_{COM}
	3	No Connection	NC
3	4	Left Current Output (0 to 1.2mA)	LI_{OUT}
4	5	Servo Decoupling Capacitor	SRVCAP
5	6	Reference Decoupling Capacitor	REFCAP
6	7	Right Current Output (0 to 1.2mA)	RI_{OUT}
	8	No Connection	NC
7	9	Right Voltage Common	RV_{COM}
8	10	Analog Common	ACOM
9	11	Digital Common	DCOM
	12	Mode Control 2	MC2
10	13	Right Data Input	RDATA
11	14	Bit Clock	BTCK
12	15	System Clock	SYSCK
13	16	Word Clock	WDCK
14	17	Left Data Input	LDATA
	18	Mode Control 3	MC3
15	19	Mode Control 1	MC1
16	20	+5V Digital Supply Voltage	$+V_D$

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM67P/69AP	16-Pin Plastic DIP	180
PCM67U/69AU	20-Pin SOIC	248

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

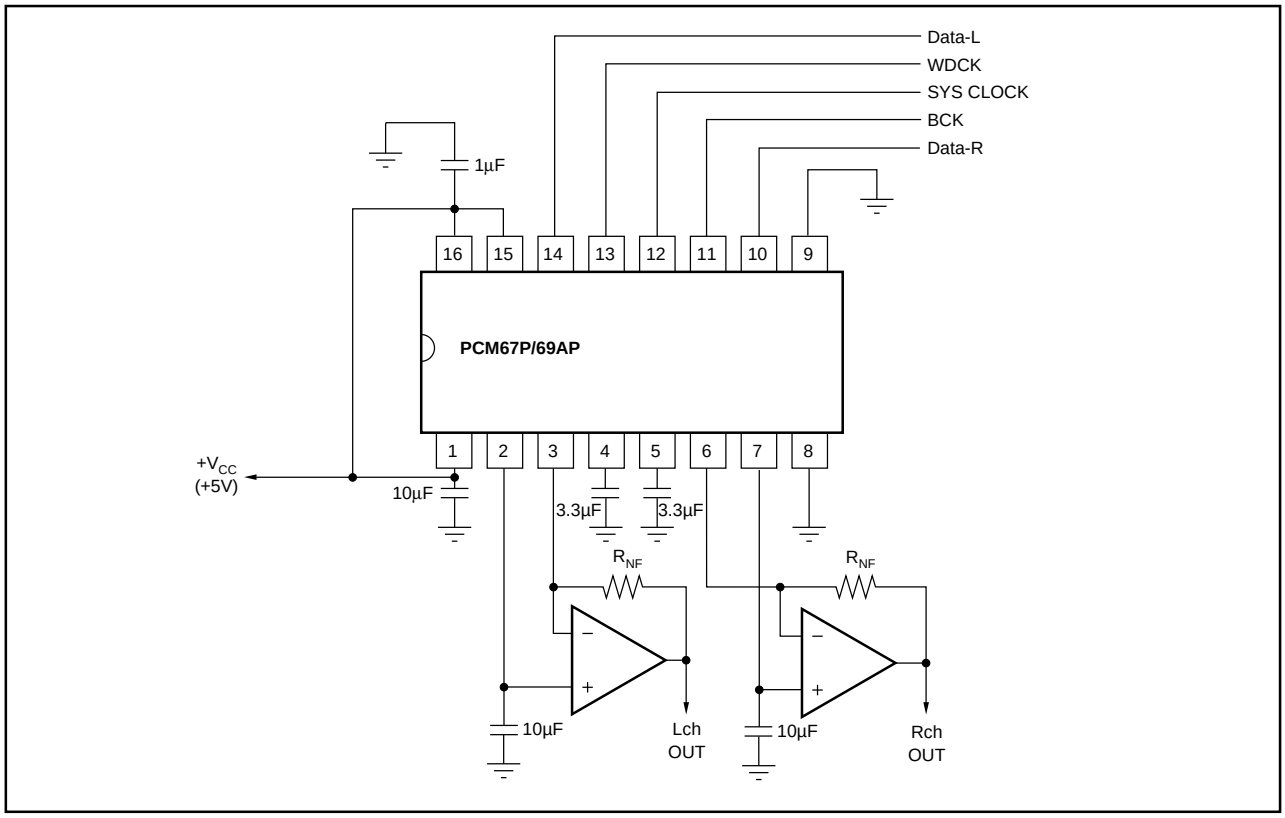
$+V_A$, $+V_D$ to ACOM, DCOM	0V to +6.5V
ACOM to DCOM	±0.5V
Digital Inputs to DCOM	–0.3V to $+V_D$ + 0.3V
Power Dissipation	300mW (U Package), 500mW (P Package)
Lead Temperature, (soldering, 10s)	+260°C
Max Junction Temperature	+165°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

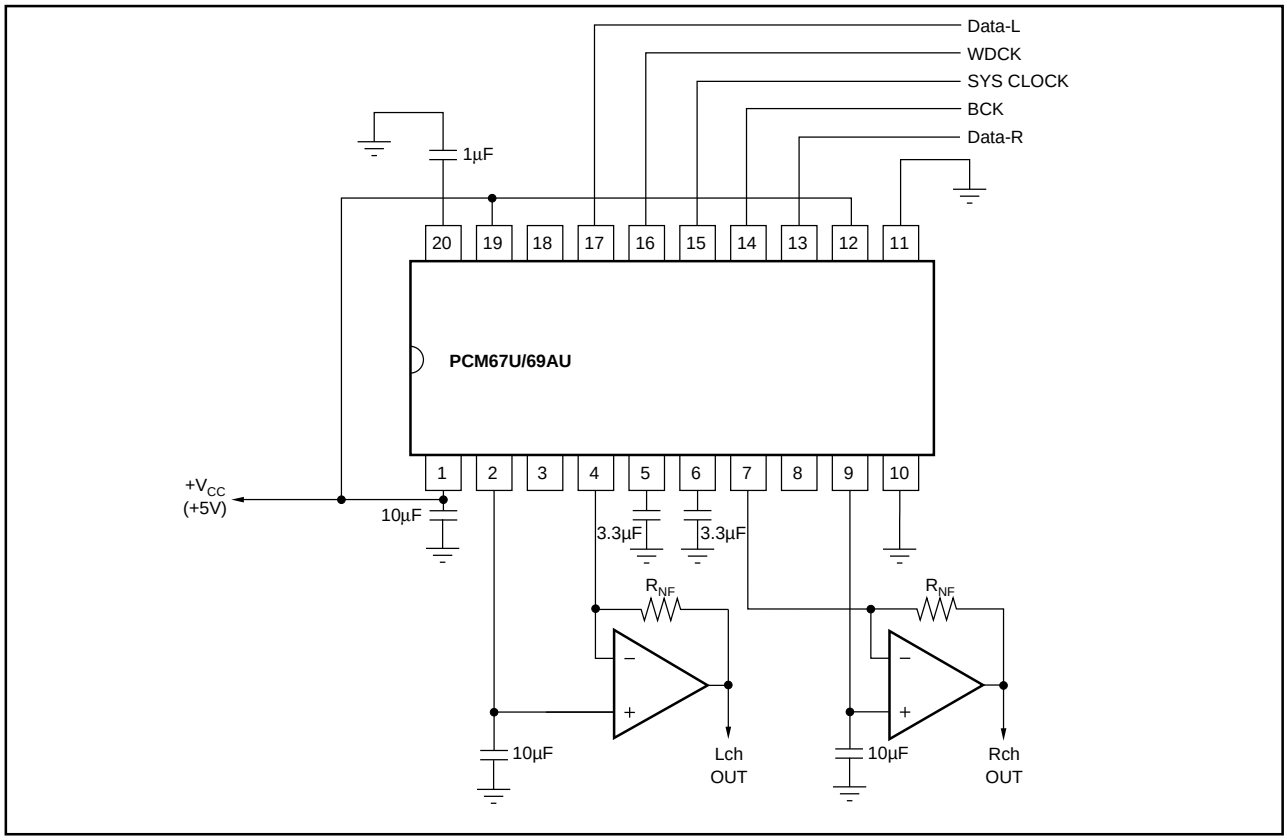
ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PIN CONFIGURATION — PCM67P/69AP (16-Pin DIP)



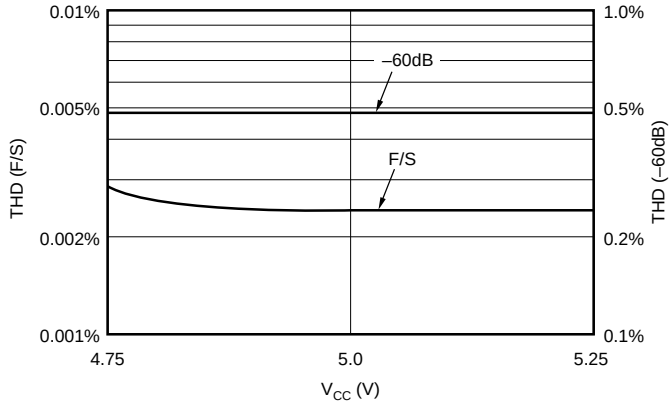
PIN CONFIGURATION — PCM67U/69AU (20-Pin SOIC)



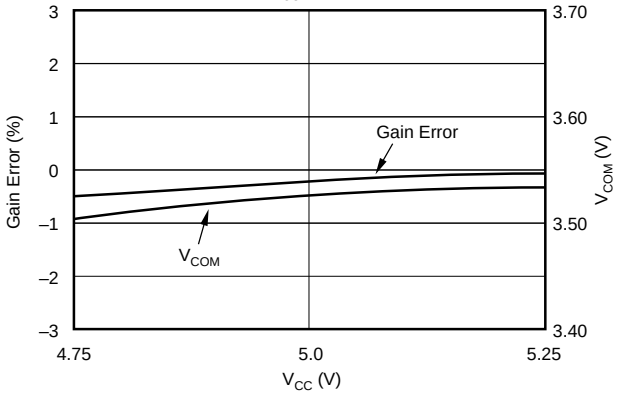
TYPICAL PERFORMANCE CURVES

All specifications at +25°C and V_{CC} = +5.0V unless otherwise noted.

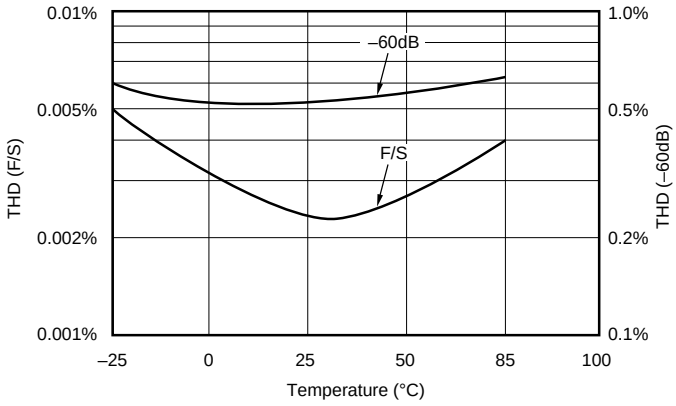
THD vs POWER SUPPLY VOLTAGE



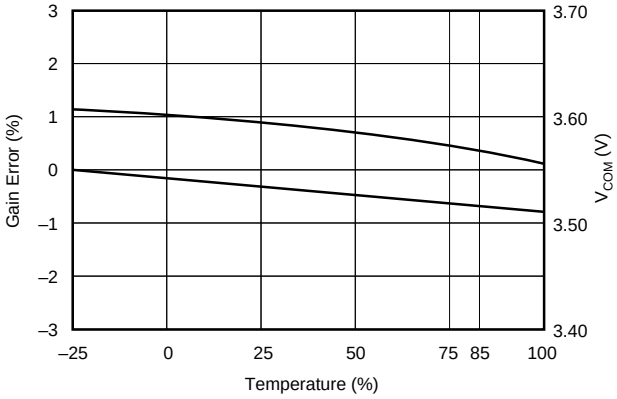
GAIN ERROR / V_{COM} vs POWER SUPPLY



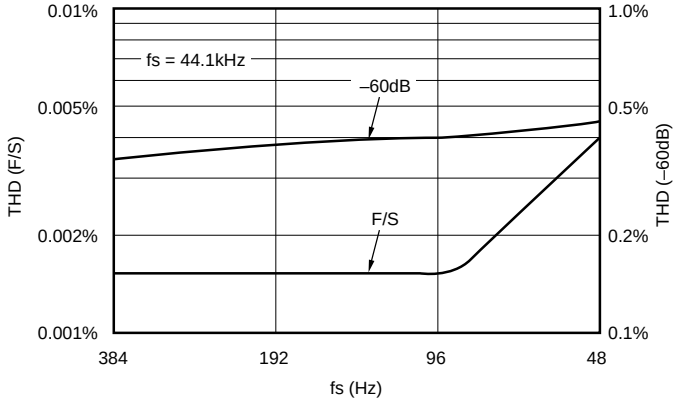
THD vs TEMPERATURE



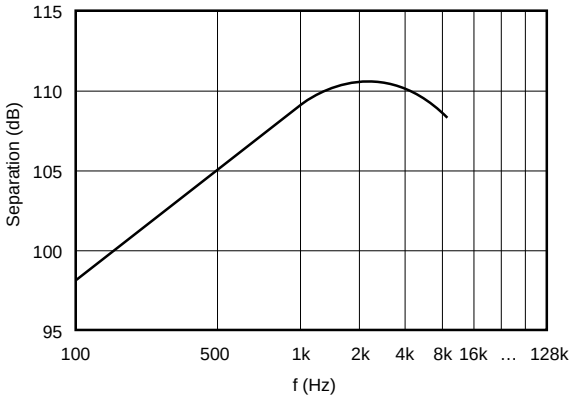
GAIN ERROR / V_{COM} vs TEMPERATURE



THD vs SYSTEM CLOCK FREQUENCY



CHANNEL SEPARATION vs SIGNAL FREQUENCY



DISCUSSION OF SPECIFICATIONS

The PCM67 and PCM69A are specified to provide critical performance criteria for a variety of applications. The accuracy of a D/A converter is described by the transfer function shown in Figure 1.

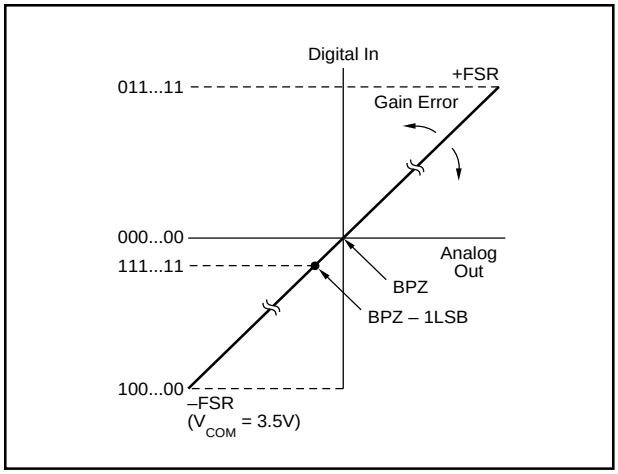


FIGURE 1. Transfer Performance.

DIGITAL INPUT CODE

The PCM67/69A accepts Binary Two's Complement (BTC) digital input code (MSB FIRST).The relationship of digital input to analog output is shown in Table 1.

DIGITAL INPUT	ANALOG OUTPUT (VOLTAGE)	ANALOG OUTPUT (CURRENT)
7FFFFF (HEX)	+FSR	–1.2mA
00003F (HEX)	BPZ	–0.6mA
FFFFFF (HEX)	BPZ – 1LSB	–0.59995mA
80003F (HEX)	–FSR	0mA

TABLE I. Digital Code and Analog Out.

GAIN ERROR AND GAIN MISMATCH, CHANNEL-TO-CHANNEL

Gain error is defined as deviation of the output current span from the ideal span of 1.2mA (FSR) on each channel. Gain error of PCM67/69A is typically ±3% of FSR.

Gain mismatch, channel-to-channel is defined as the difference in gain error between the left channel and right channel.

THE RELATIONSHIP OF V_{COM} AND I/V OUT

The output current range of PCM67 and PCM69A is 0mA to 1.2mA as shown in Table 1.

In the typical application, the non-inverting input of the external I/V op amp is connected to the V_{COM} pin of PCM67 and PCM69A. Accordingly, the output voltage level at FSR after I/V conversion is V_{COM} voltage (+3.5V) as shown in Figure 2.

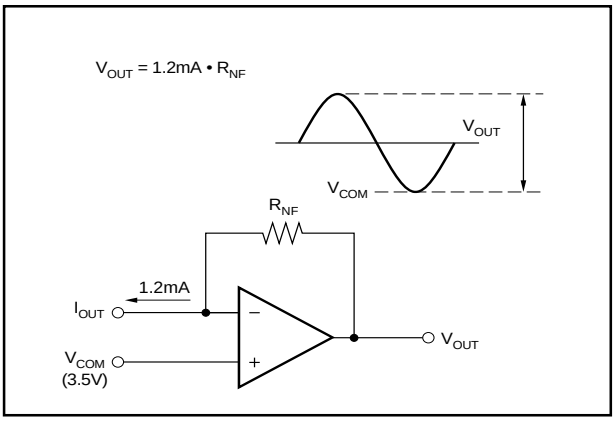


FIGURE 2. I/V Amplifier Circuit.

S/N RATIO

S/N ratio is defined as the ratio of full scale output and no input noise level at BPZ point. The PCM67/69A is specified at 110dB typical with "IHF-A" filter.

LEVEL LINEARITY ERROR

Level linearity error is defined as the deviation of actual analog output level from digital input level. PCM67/69A is specified at 1dB typical at –90dB output level. The 0.5LSB quantization error at –90dB of 16-bit conversion is equal to +1.94dB, –2.5dB.

TOTAL HARMONIC DISTORTION

THD is a key parameter in audio applications, THD is a measure of the magnitude and distribution of the linearity error, differential linearity error, and noise, as well as quantization error. To be useful, THD should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of D/A converter accuracy for audio applications.

THD is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency and is expressed in percent or dB. The rms value of the PCM67/69A error referred to the input can be shown to be

$$\varepsilon_{rms} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}\left[E_L(i) + E_Q(i)\right]^2} \qquad (1)$$

where n is the number of samples in one cycle of any given sine wave, $E_L(i)$ is the linearity error of the PCM67 or PCM69A at each sampling point. THD can then be expressed as

$$THD = \frac{\varepsilon_{rms}}{E_{rms}} = \frac{\sqrt{\frac{1}{n}\sum_{i=1}^{n}\left[E_L(i) + E_Q(i)\right]^2}}{E_{rms}} \times 100\% \qquad (2)$$

where E_{rms} is the rms signal-voltage level.

This expression indicates that, in general, there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to THD.

For PCM67 and PCM69A the test period is set at an 8X oversampling rate (352.8kHz = 44.1kHz • 8), which is the typical sample rate for CD player applications.

The test signal frequency is 991Hz and the amplitude of the signal level is F/S (0dB), and –60dB down from F/S.

All THD tests are performed without a deglitcher circuit and without a 20kHz low pass filter.

SYSTEM CLOCK REQUIREMENTS

The PCM67 and PCM69A need a system clock for the one-bit noise shaping DAC operation.

The PCM67 is capable of only a 384Fs corollary system clock frequency such as 192Fs, 96Fs (24 times word rate or integer multiple of 24).

The PCM69A is capable of any system clock up from 48Fs to 384Fs such as 384Fs, 256Fs, 100Fs with condition for timing as described in "Timing of PCM69A" in Figure 5.

The user can choose either model for their application. Table II shows the different SYSCLK options.

MODEL	BASIC SYSCLK	OTHER CAPABLE SYSCLK
PCM67	384Fs	192Fs, 96Fs
PCM69A	Any Clock (with timing condition) Examples: 384Fs, 300Fs, 256Fs, 200Fs, 90Fs	

TABLE II. System Clock Requirements.

LOGIC TIMING

The serial data bit transfers are triggered on positive bit clock (BCK) edges. The serial-to-parallel data transfer to the DAC occurs on the falling edge of Word Clock (WDCK). The change in the output of the DAC coincides with the falling edge of WDCK.

Refer to Figure 3 for graphical relationships of these signals. The setup and hold timing relationships for these signals are shown in Figure 4.

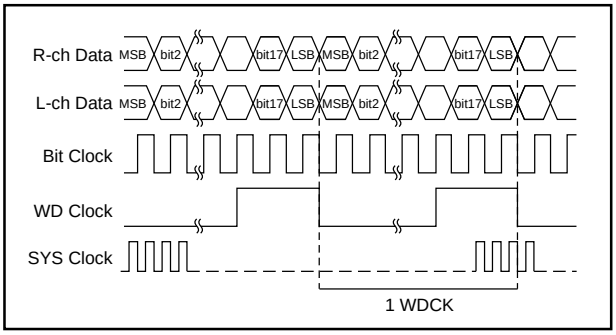


FIGURE 3. Timing Diagram.

The PCM67/69A accepts TTL compatible logic input levels. The data format of the PCM67/69A is BTC with the most significant bit (MSB) being first in the serial input bit stream.

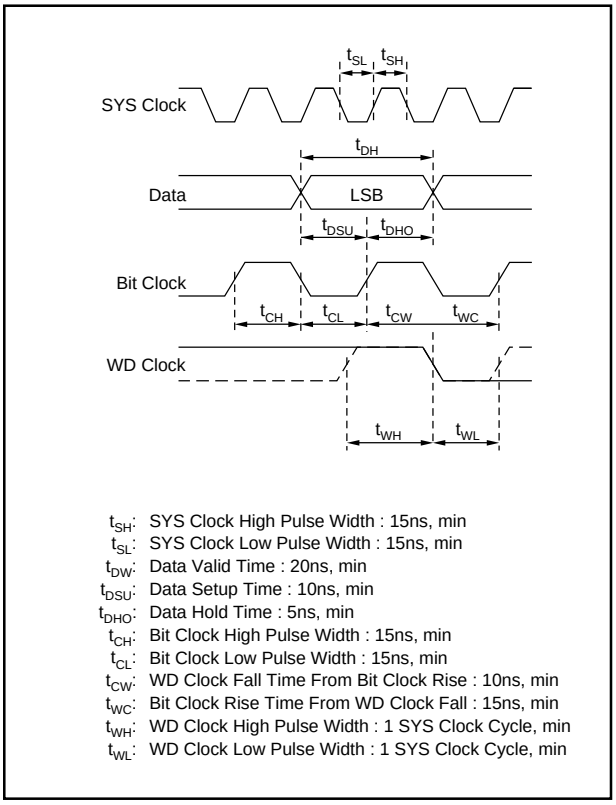


FIGURE 4. Timing Specification.

TIMING OF PCM69A

PCM69A timing is similar to PCM67 except that PCM69A is capable of operating from any system clock up to 384Fs. For synchronized operation, PCM69A system clock and WDCK timing must be as shown in Figure 5.

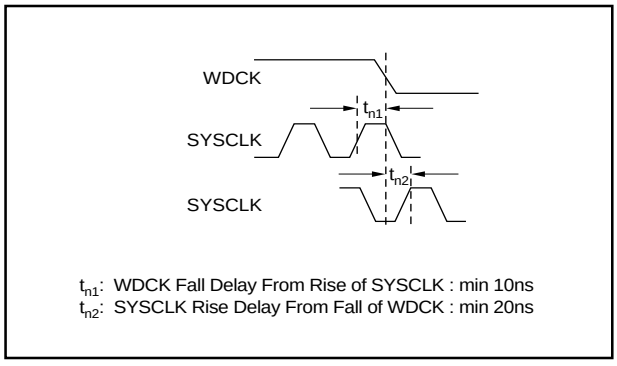


FIGURE 5. Timing of PCM69A for SYSCLK and WDCK.

INSTALLATION

POWER SUPPLIES

Refer to "Pin Configuration" diagram for proper connection of the PCM67/69A. The PCM67/69A requires only a +5V supply. Both analog and digital supplies should be tied together at a single point, as no real advantage is gained by using separate supplies. It is more important that both these supplies be as "clean" as possible to reduce coupling of supply noise to the output.

FILTER CAPACITOR REQUIREMENTS

As shown in the "Pin Configuration" diagram, various sizes of decoupling capacitors can be used with no special tolerances required. All capacitors should be as close to the appropriate pins of the PCM67/69A as possible to reduce noise pickup from surrounding circuitry.

A power supply decoupling capacitor should be used near the analog supply pin to maximize power supply rejection, as shown in Figure 6, regardless of how good the supplies are. Both commons should be connected to an analog ground plane as close to the PCM67/69A as possible.

The value of these capacitors is influenced by actual board layout design and noise from power supplies and other digital input lines.

The best suitable value for the capacitors should be determined by the user's actual application board.

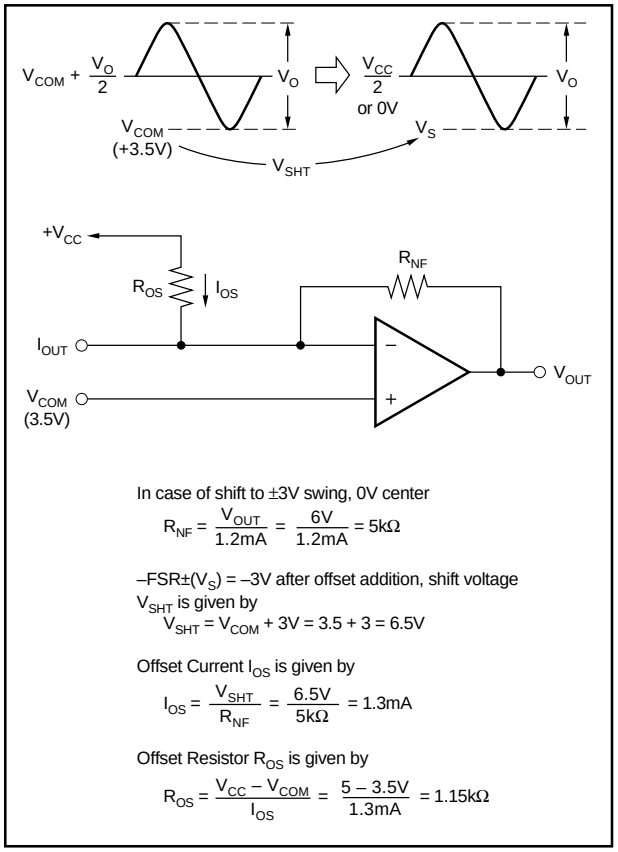


FIGURE 6. Shift of I/V Out Voltage.

SHIFT OF I/V OUT VOLTAGE

If the user requires a bipolar voltage output centered around 0V or one-half of V_{CC}, the output can be shifted by adding an offset current on the inverting point of the I/V op amp as shown in Figure 6.

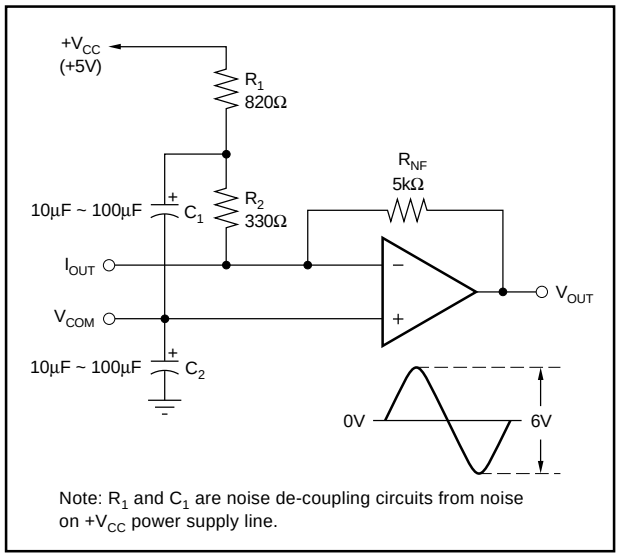


FIGURE 7. Useful Application Circuit for Shift of I/V Out Voltage.

INTERFACE CONTROL FUNCTION

Both the PCM67 and PCM69A (SOIC package type) are capable of 16-bit L/R serial input and 20-bit L/R parallel input as shown in Table 3.

MC1	MC2	MC3	DATA-R	INPUT FORMAT
0	0	1	0	16-Bit L/R Serial(1) $\overline{L}R\overline{L}R$ WDCK
0	0	1	1	16-Bit L/R Serial(1) $L\overline{R}L\overline{R}$ WDCK
0	1	1	0	18-Bit L/R Serial(1) $\overline{L}R\overline{L}R$ WDCK
0	1	1	1	18-Bit L/R Serial(1) $L\overline{R}L\overline{R}$ WDCK
1	0	1	X	20-Bit L/R Parallel
1	0	0	X	20-Bit L/R Parallel [WDCK Invert]
1	1	1	X	18-Bit L/R Parallel
1	1	0	X	18-Bit L/R Parallel [WDCK Invert]

NOTE: (1) Data input to Data-Lch (Pin 17) for L/R serial format.

TABLE III. Interface Control Function of SOIC.

PCM67P and PCM69AP (DIP package) have only 18-bit L/R serial input function as shown in Table 4.

MC1	DATA-R	INPUT FORMAT
0	0	18-Bit L/R Serial $\overline{L}R\overline{L}R$ WDCK
0	1	18-Bit L/R Serial $L\overline{R}L\overline{R}$ WDCK
1	X	18-Bit L/R Parallel

TABLE IV. Interface Control Function of DIP.

DIGITAL FILTER INTERFACE

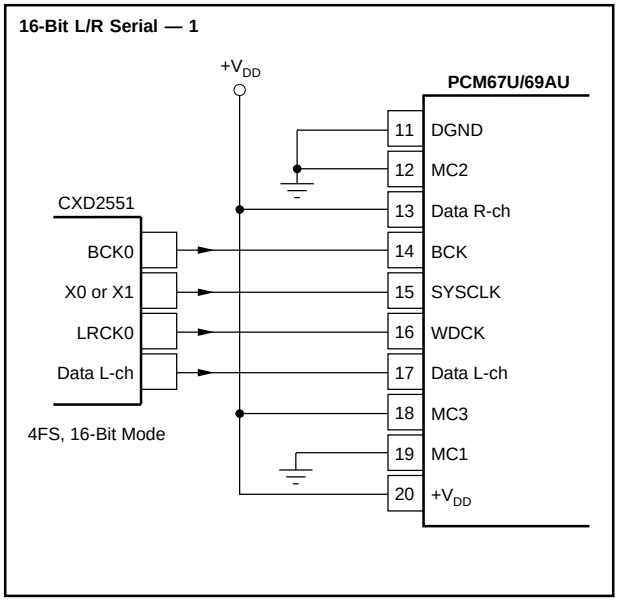


FIGURE 8. Using Sony CXD2551.

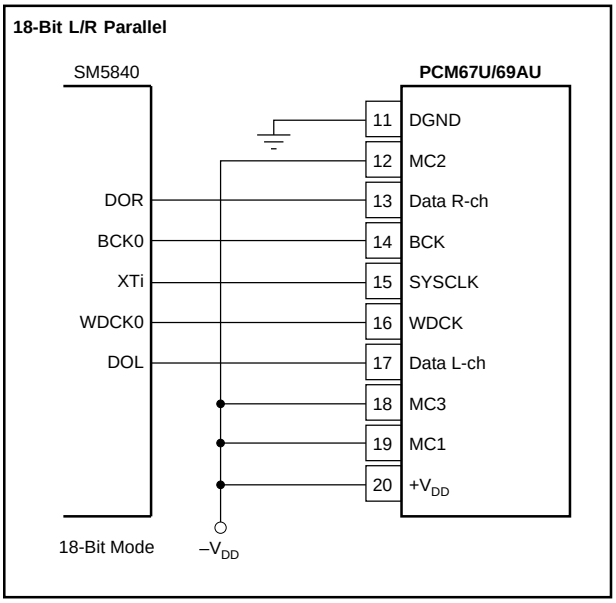


FIGURE 10. Using NPC SM5840.

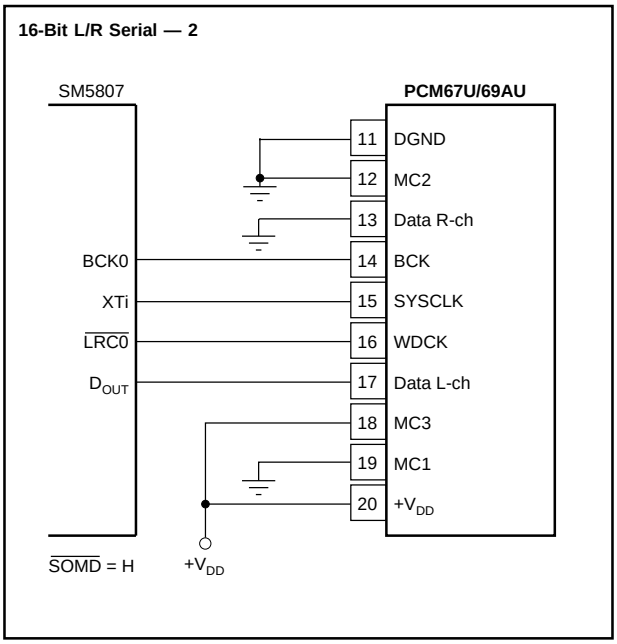


FIGURE 9. Using NPC SM5807.

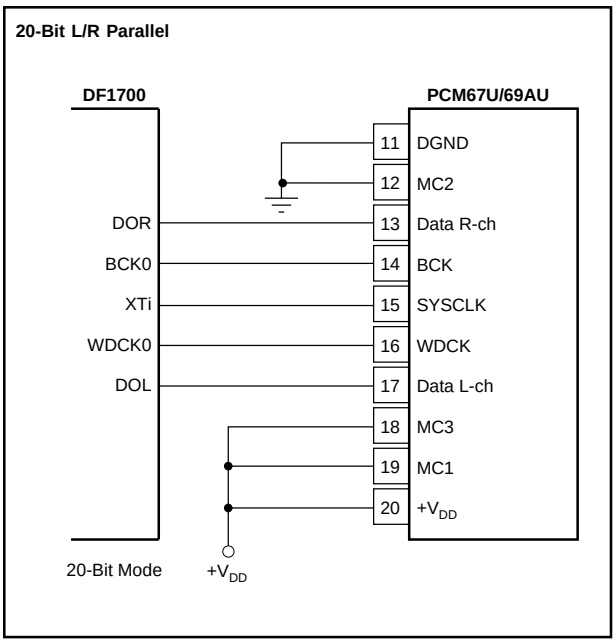


FIGURE 11. Using Burr-Brown DF1700.

THEORY OF OPERATION

Digital converters in audio systems have traditionally utilized a laser-trimmed, current-source DAC architecture. Unfortunately, this type of technology suffers from the problems inherent in switching widely varying current levels. Design improvements have helped, but DACs of this type still exhibit low-level nonlinearity due to errors at the major carry.

Recently, DACs employing a different architecture have been introduced. Most of these DACs utilize a one-bit DAC with "noise shaping" techniques and very high oversampling rate to achieve the digital-to-analog conversion. Basically, the trade-off is from very accurate but slow current sources to one rapidly sampled current source whose average output in the audio frequency range is equal to the current desired. Noise shaping insures that the "undesirable" frequencies associated with one-bit DAC output lie outside the audio range.

These "Bitstream", "MASH", or one-bit DACs overcome the low level linearity problems of conventional DACs, since there can be no major carry error. However, this architecture exhibits problems of its own: signal-to-noise performance is usually worse than a similar conventional DAC, "dither noise" may be needed in order to get rid of unwanted tones, a separate high-speed clock may be required, the part may show sensitivity to clock jitter, and a high-order low-pass filter is necessary to filter the DAC output.

The PCM67/69A is a cross between these two architectures. It includes both a conventional laser-trimmed, current-source DAC and an advanced one-bit DAC. The conventional DAC is a 10-bit DAC where each bit weight has been trimmed to 18-bit linearity. The one-bit DAC has a weight equal to bit 10 and employs a first-order noise shaper to generate the "bitstream."

This approach does not eliminate all the problems associated with the two architectures but rather minimizes them as much as possible. The conventional DAC still exhibits some major carry error which would normally reduce low-level linearity. However, to reduce this error even further, the PCM67/69A utilizes an offset technique whereby bit n is subtracted from the digital input code whenever it is positive (see Figure 1 and Table I). When this is done, an offset current equal to the weight of bit n is switched in to compensate. This offset comes from a one-bit DAC which has also been trimmed to 18-bit linearity. While this technique doesn't remove the major carry error completely, the "glitch" is only present in higher amplitude signals where it is much less audible.

As for the one-bit DAC, a number of problems with this architecture are also reduced: the DAC is designed to operate from the system clock, thus eliminating the need for a separate clock; the lower quantizing level of the DAC make it less sensitive to clock jitter; and output filtering requirements are reduced because "out-of-band noise" has smaller amplitude, is "farther-out," and increases much more slowly due to the first-order noise shaper. Still, it is important to keep in mind that the one-bit DAC imposes some design considerations. Figure 2 shows the THD + N of the converter versus "System Clock" frequency. This is the clock used to operate the one-bit DAC and noise shaper. Generally, the higher the oversampling the better. However, near full-scale, the converter is limited by other constraints and higher clock frequencies (past $96f_s$) tend to slightly worsen its performance. At low levels, performance improves almost linearly with increasing clock frequency. The one-bit DAC was designed to operate between $96f_s$ (4X oversampling) and $384f_s$ (16X oversampling). But, it can be operated at $48f_s$ (2X oversampling) with slightly reduced performance.

TOTAL HARMONIC DISTORTION + NOISE

A key specification for audio DACs is usually total harmonic distortion plus noise (THD + N). For the PCM67/69A, THD + N is tested in production as shown in Figure 12. Digital data words are read into the PCM67/69A at eight times the standard compact disk audio sampling frequency of 44.1kHz (352.8kHz) so that a sine wave output of 991Hz is realized. The output of the DAC goes to an I-to-V converter, then to a programmable gain amplifier to provide gain at lower signal output test levels, and then through a 40kHz low pass filter before being fed into an analog type distortion analyzer.

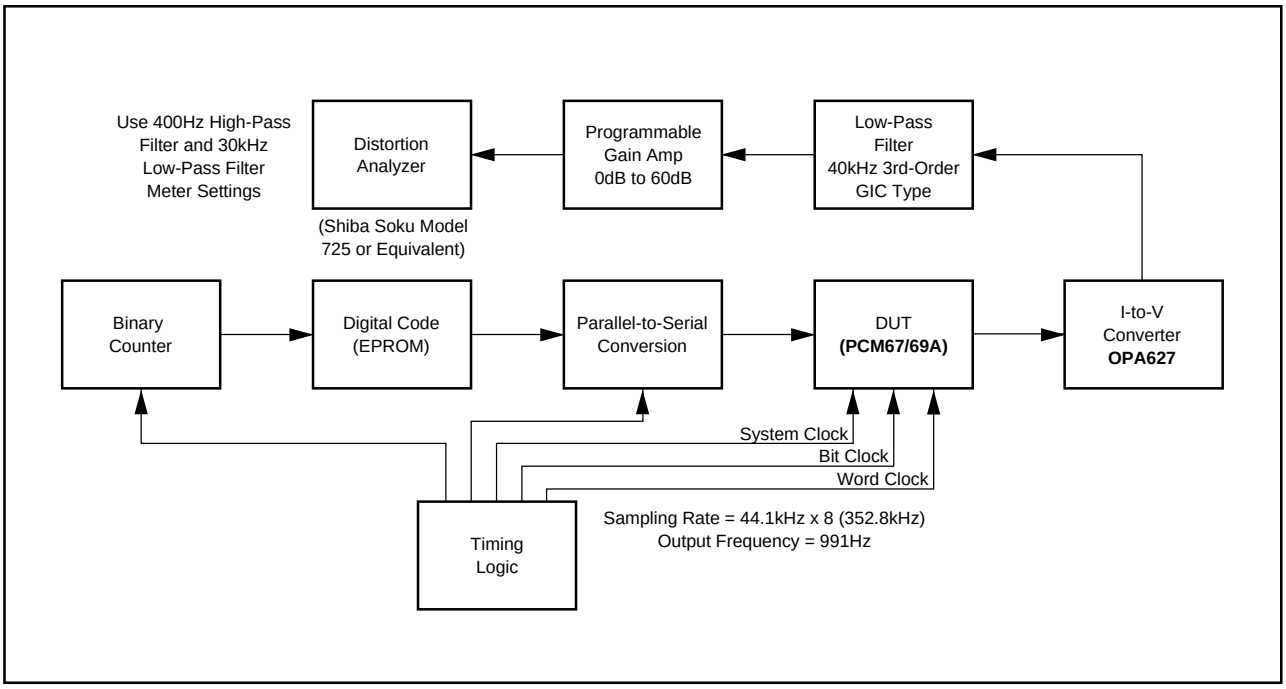


FIGURE 12. PCM67/69A THD+N Production Test.

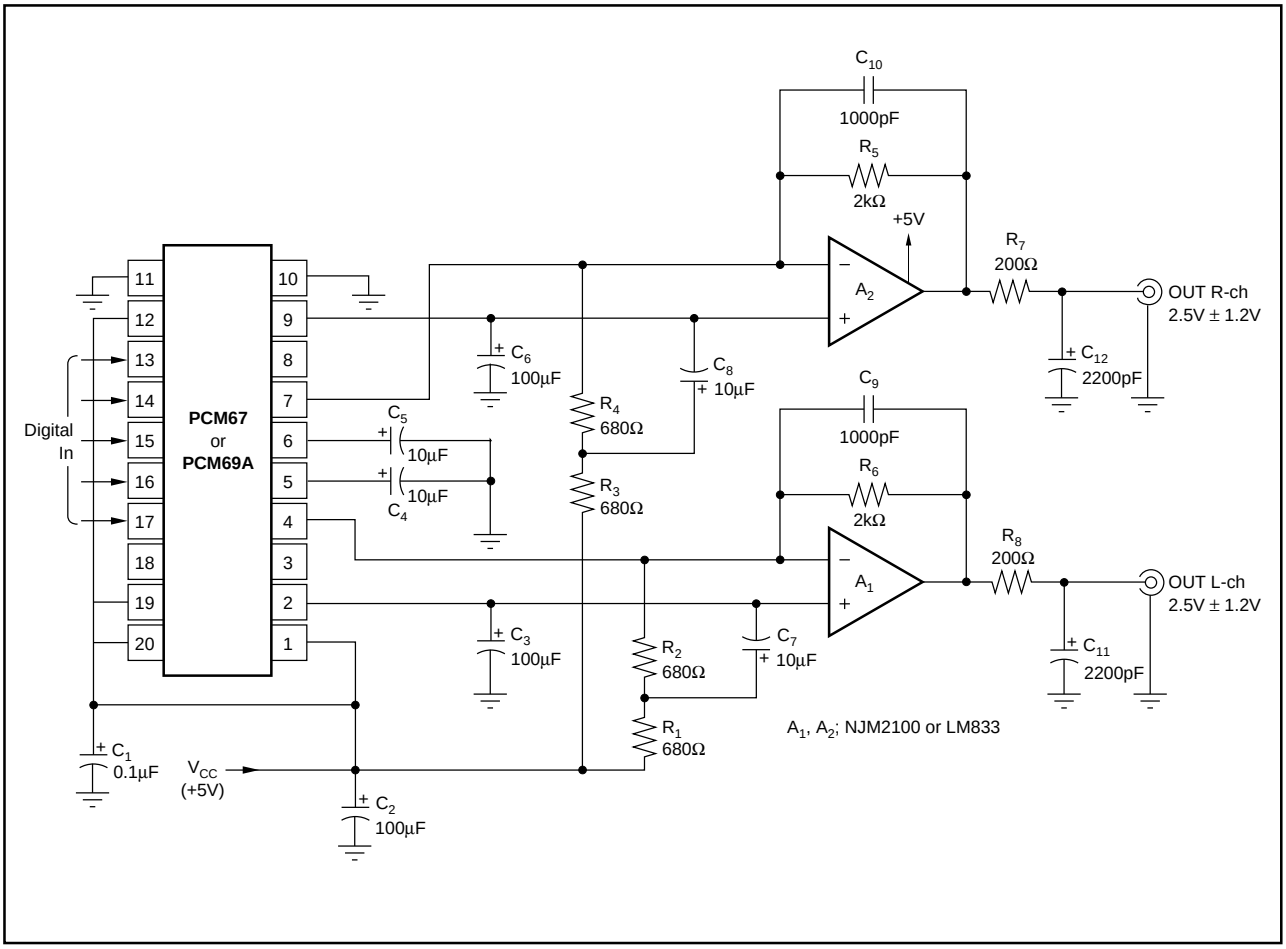


FIGURE 13. Single +5V Power Supply, with LPF, I/V Amp Application Circuit for Portable Digital Audio.

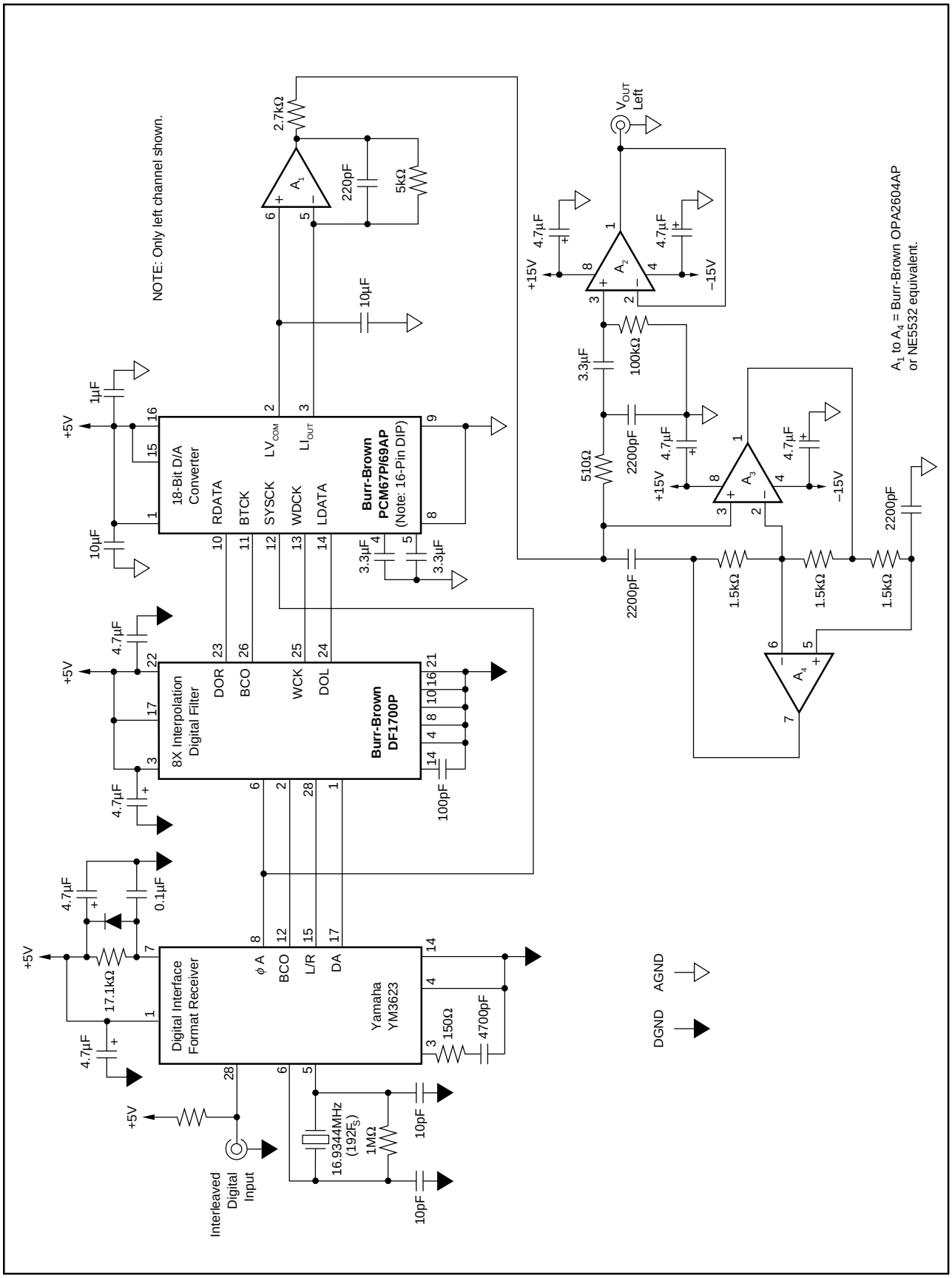


FIGURE 14. HiFi D/A Converter Unit Application with Digital Audio Interface Format.