LOW-NOISE, VERY LOW DRIFT, PRECISION VOLTAGE REFERENCE

Check for Samples: REF5020-EP, REF5025-EP, REF5040-EP, REF5050-EP

FEATURES

- **LOW TEMPERATURE DRIFT: 5 ppm/°C (max)**
- **HIGH ACCURACY: 0.08% (max)**
- **LOW NOISE: 3 μV_{PP}/V**
- **HIGH OUTPUT CURRENT: ±10 mA**

APPLICATIONS

- **16-BIT DATA ACQUISITION SYSTEMS**
- **ATE EQUIPMENT**
- **INDUSTRIAL PROCESS CONTROL**
- **MEDICAL INSTRUMENTATION**
- **OPTICAL CONTROL SYSTEMS**
- **PRECISION INSTRUMENTATION**

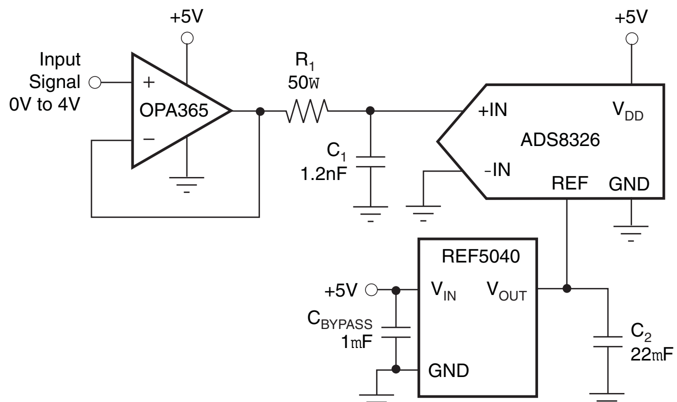
SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

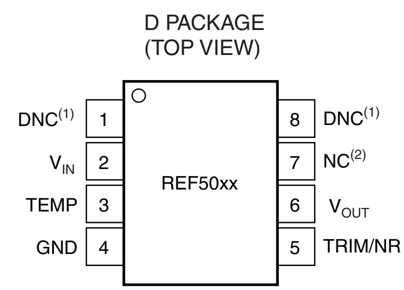
- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

DESCRIPTION

The REF50xx is a family of low-noise, low-drift, very high precision voltage references. These references are capable of both sinking and sourcing, and are very robust with regard to line and load changes.

(1) Custom temperature ranges available





NOTES: (1) DNC = Do not connect.
(2) NC = No internal connection.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	OUTPUT VOLTAGE	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
REF5020MDREP	2.048 V	SOIC-D	REF5020MDREP	5020EP
REF5025MDTEP	2.5 V	SOIC-D	REF5025MDTEP	5025EP
REF5040MDREP	4.096 V	SOIC-D	REF5040MDREP	5040EP
REF5050MDREP	5 V	SOIC-D	REF5050MDREP	5050EP

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

ABSOLUTE MAXIMUM RATINGS(1)

PARAMETER		REF50xx	UNIT
Input Voltage		18	V
Output Short-Circuit		30	mA
Operating Temperature Range		–55 to 125	°C
Storage Temperature Range		–65 to 150	°C
Junction Temperature (T_J max)		150	°C
ESD Rating	Human Body Model (HBM)	3000	V
	Charged Device Model (CDM)	1000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS: PER DEVICE

Boldface limits apply over the specified temperature range, **T_A = –55°C to 125°C.**
At T_A = 25°C, I_{LOAD} = 0, C_L = 1 μF, and V_{IN} = (V_{OUT} + 0.2 V) to 18 V, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
REF5020 (V_{OUT} = 2.048V)(1)						
OUTPUT VOLTAGE						
Output Voltage	V_{OUT}	2.7 V < V_{IN} < 18 V		2.048		V
Initial Accuracy			–0.05		0.05	%
Over Temperature			**–0.08**		**0.08**	%
NOISE						
Output Voltage Noise		f = 0.1 Hz to 10 Hz		6		μV_{PP}
REF5025 (V_{OUT} = 2.5 V)						
OUTPUT VOLTAGE						
Output Voltage	V_{OUT}			2.5		V
Initial Accuracy			–0.05		0.05	%
NOISE						
Output Voltage Noise		f = 0.1 Hz to 10 Hz		7.5		μV_{PP}
REF5040 (V_{OUT} = 4.096V)						
OUTPUT VOLTAGE						
Output Voltage	V_{OUT}			4.096		V
Initial Accuracy			–0.05		0.05	%
Over Temperature			**–0.08**		**0.08**	%
NOISE						
Output Voltage Noise		f = 0.1 Hz to 10 Hz		12		μV_{PP}
REF5050 (V_{OUT} = 5 V)						
OUTPUT VOLTAGE						
Output Voltage	V_{OUT}			5		V
Initial Accuracy			–0.05		0.05	%
Over Temperature			**–0.08**		**0.08**	%
NOISE						
Output Voltage Noise		f = 0.1 Hz to 10 Hz		15		μV_{PP}

(1) For V_{OUT} ≤ 2.5 V, the minimum supply voltage is 2.7 V.

ELECTRICAL CHARACTERISTICS: ALL DEVICES

Boldface limits apply over the specified temperature range, **T_A = –55°C to 125°C.**
At T_A = 25°C, I_{LOAD} = 0, C_L = 1 µF, and V_{IN} = (V_{OUT} + 0.2 V) to 18 V, unless otherwise noted.

PARAMETER		CONDITIONS	REF50xx MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE TEMPERATURE DRIFT						
Output Voltage Temperature Drift	dV_{OUT}/dT					
REF5025				**4**	**6.5**	**ppm/°C**
REF5050				**4**	**6.5**	**ppm/°C**
All other devices				**3**	**5**	**ppm/°C**
LINE REGULATION						
Line Regulation	dV_{OUT}/dV_{IN}					
REF5020 (1)		V_{IN} = 2.7 V to 18V		0.1	1	ppm/V
All other devices		V_{IN} = V_{OUT} + 0.2 V		0.1	1	ppm/V
Over Temperature				**1**	**3**	**ppm/V**
LOAD REGULATION						
Load Regulation	dV_{OUT}/d_{ILOAD}					
REF5020		–10 mA < I_{LOAD} < +10 mA, V_{IN} = 3 V		20	30	ppm/mA
All other devices		–10 mA < I_{LOAD} < +10 mA, V_{IN} = V_{OUT} + 0.75 V		20	30	ppm/mA
Over Temperature					**60**	**ppm/mA**
SHORT-CIRCUIT CURRENT						
Short-Circuit Current	I_{SC}	V_{OUT} = 0		25		mA
TEMP PIN						
Voltage Output		At T_A = 25°C		575		mV
Temperature Sensitivity				**2.64**		**mV/°C**
TURN-ON SETTLING TIME						
Turn-On Settling Time		To 0.1% with C_L = 1 µF		200		µs
POWER SUPPLY						
Supply Voltage	V_S	See Note (1)	V_{OUT} + 0.2 (1)		18	V
Quiescent Current				0.8	1	mA
Over Temperature					**1.25**	**mA**
TEMPERATURE RANGE						
Specified Range			–55		125	°C
Operating Range			–55		125	°C
Thermal Resistance	θ_{JA}			150		°C/W

(1) For V_{OUT} ≤ 2.5 V, the minimal supply voltage is 2.7 V.

TYPICAL CHARACTERISTICS

At T_A = 25°C, I_{LOAD} = 0, and V_S = V_{OUT} + 0.2 V, unless otherwise noted.
For V_{OUT} ≤ 2.5 V, the minimum supply voltage is 2.7 V.

TEMPERATURE DRIFT (0°C to +85°C)

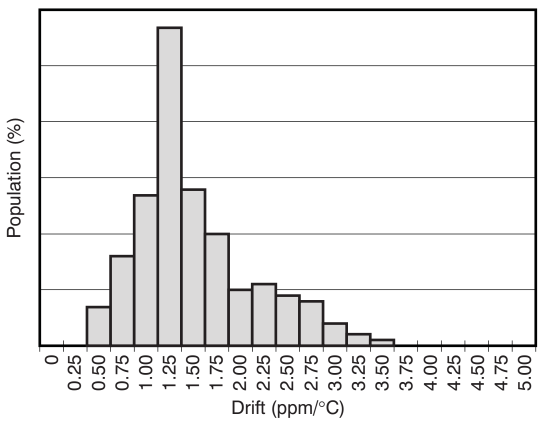


Figure 1.

TEMPERATURE DRIFT (–40°C to +125°C)

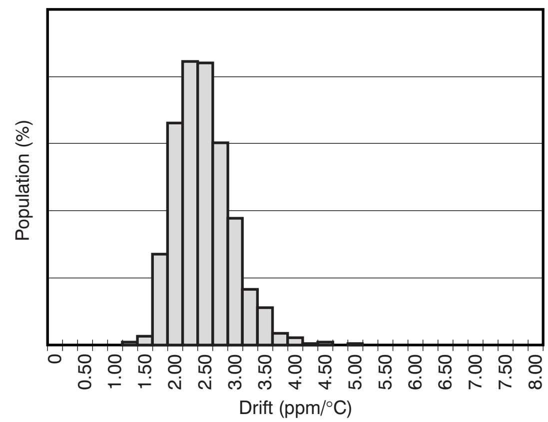


Figure 2.

OUTPUT VOLTAGE INITIAL ACCURACY

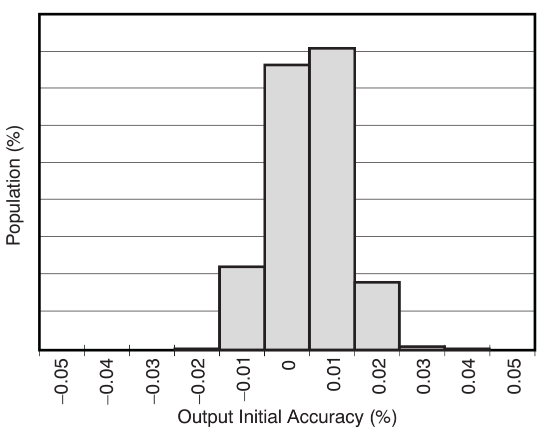


Figure 3.

OUTPUT VOLTAGE ACCURACY vs TEMPERATURE

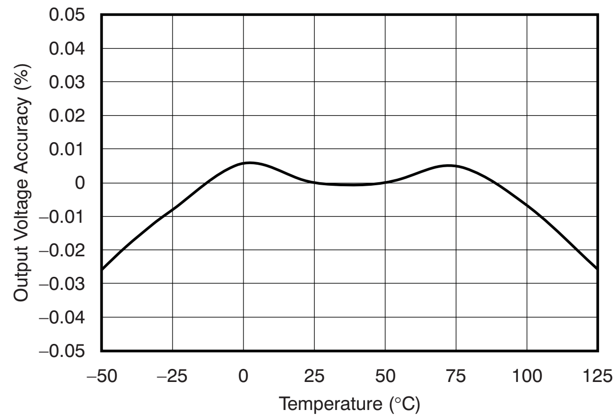


Figure 4.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, I_{LOAD} = 0, and V_S = V_{OUT} + 0.2 V, unless otherwise noted.

For V_{OUT} ≤ 2.5 V, the minimum supply voltage is 2.7 V.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

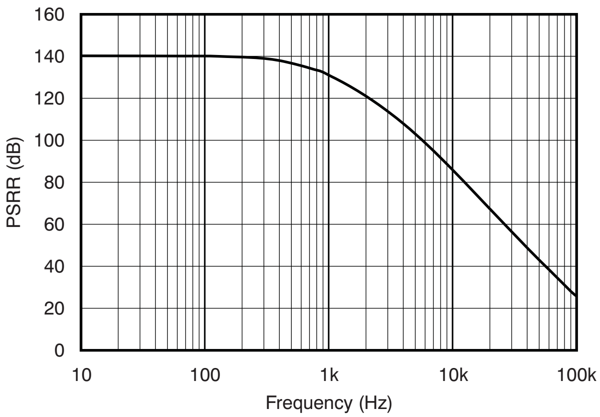


Figure 5.

DROPOUT VOLTAGE vs LOAD CURRENT

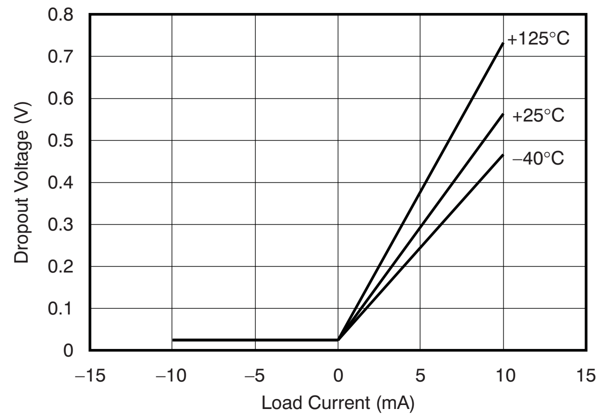


Figure 6.

REF5025 OUTPUT VOLTAGE vs LOAD CURRENT

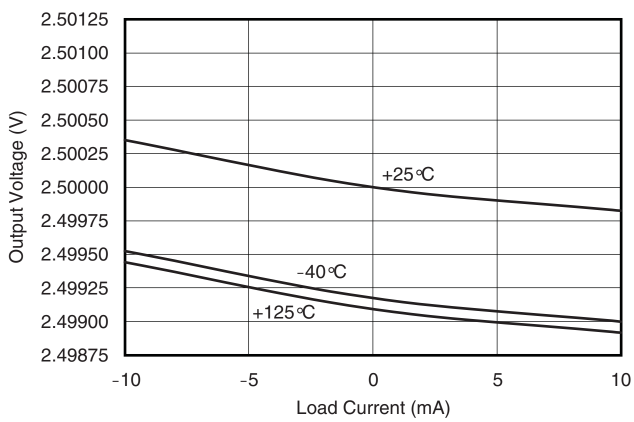


Figure 7.

TEMP PIN OUTPUT VOLTAGE vs TEMPERATURE

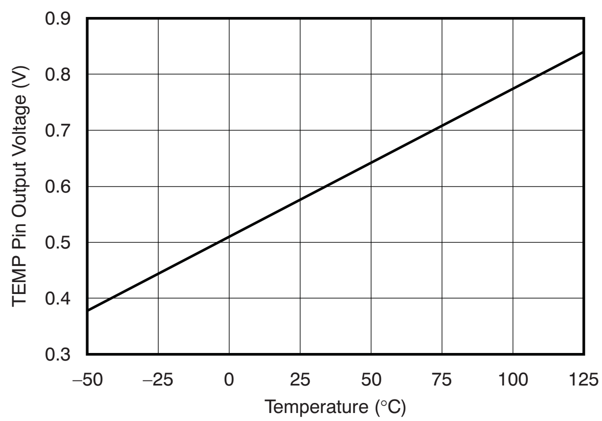


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, I_{LOAD} = 0, and V_S = V_{OUT} + 0.2 V, unless otherwise noted.

For V_{OUT} ≤ 2.5 V, the minimum supply voltage is 2.7 V.

QUIESCENT CURRENT vs TEMPERATURE

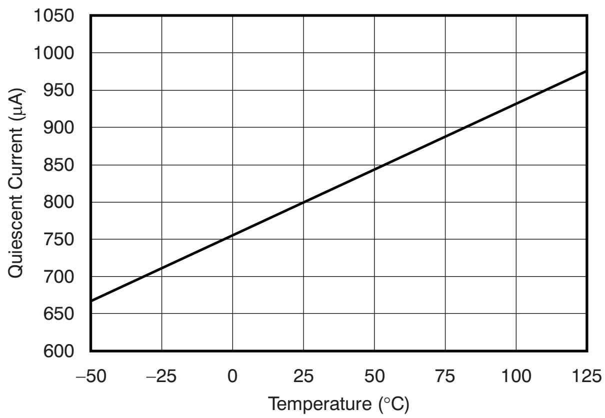


Figure 9.

QUIESCENT CURRENT vs INPUT VOLTAGE

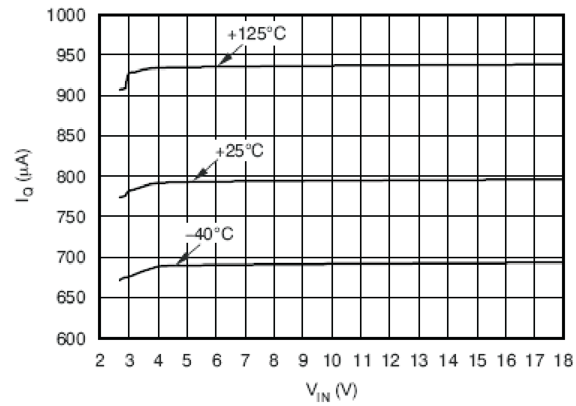


Figure 10.

LINE REGULATION vs TEMPERATURE

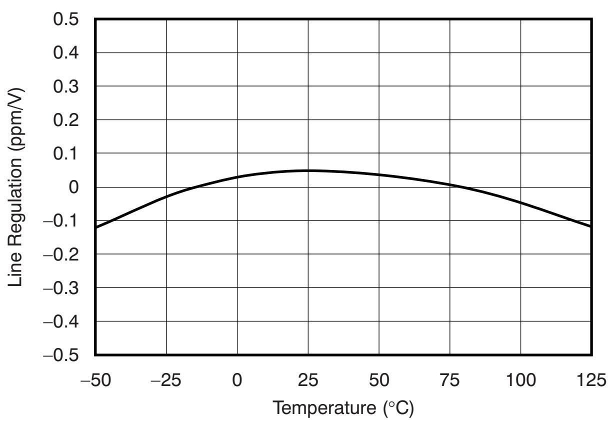


Figure 11.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

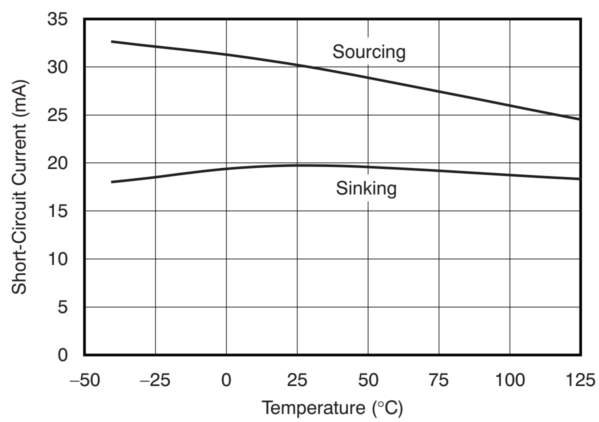


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, I_{LOAD} = 0, and V_S = V_{OUT} + 0.2 V, unless otherwise noted.

For V_{OUT} ≤ 2.5 V, the minimum supply voltage is 2.7 V.

NOISE

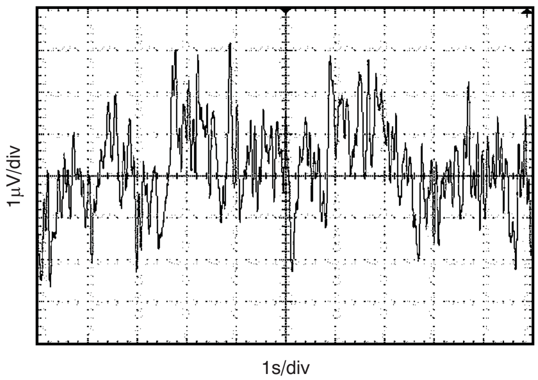


Figure 13.

STARTUP (REF5025, C_L = 1 μF)

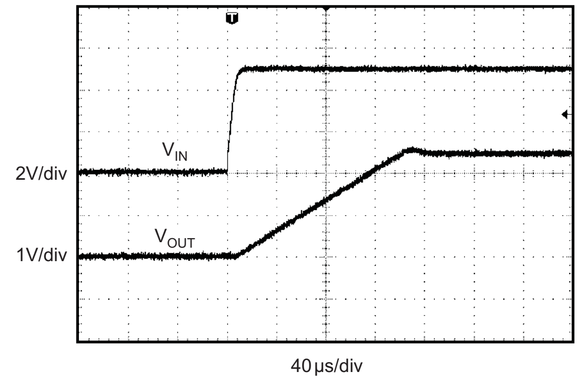


Figure 14.

STARTUP (REF5025, C_L = 10 μF)

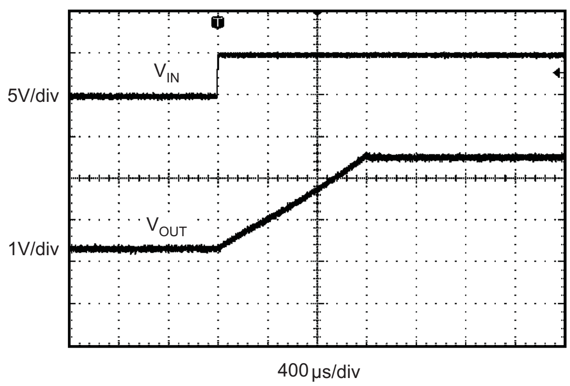


Figure 15.

LOAD TRANSIENT (C_L = 1μF, I_{OUT} = 1mA)

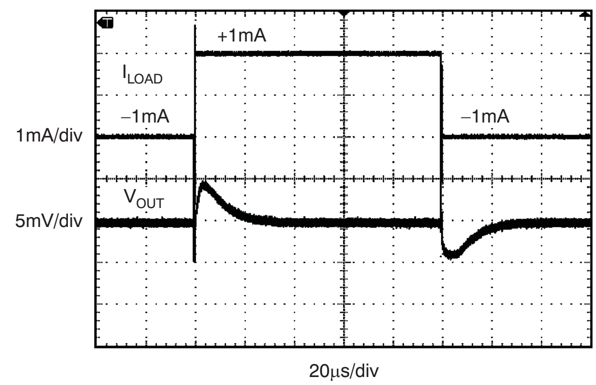


Figure 16.

LOAD TRANSIENT (C_L = 1μF, I_{OUT} = 10mA)

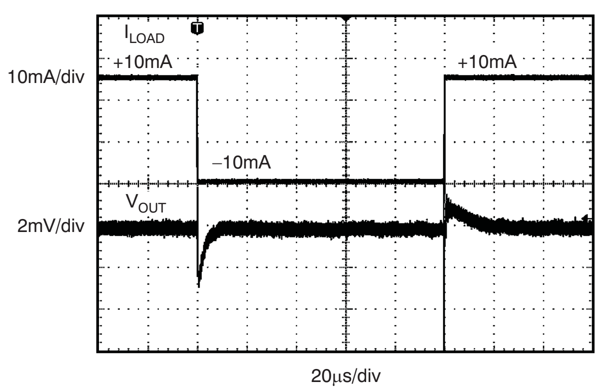


Figure 17.

LOAD TRANSIENT (C_L = 10μF, I_{OUT} = 1mA)

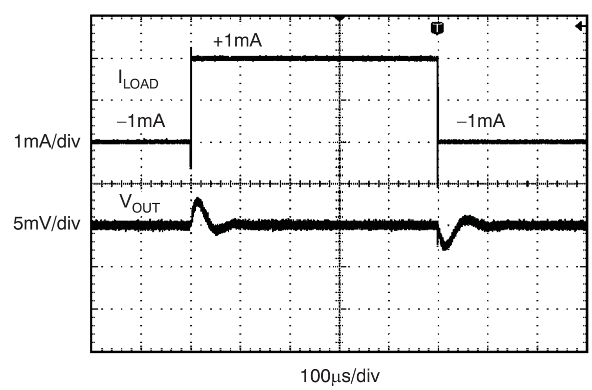


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, I_{LOAD} = 0, and V_S = V_{OUT} + 0.2 V, unless otherwise noted.

For V_{OUT} ≤ 2.5 V, the minimum supply voltage is 2.7 V.

LOAD TRANSIENT
(C_L = 10μF, I_{OUT} = 10mA)

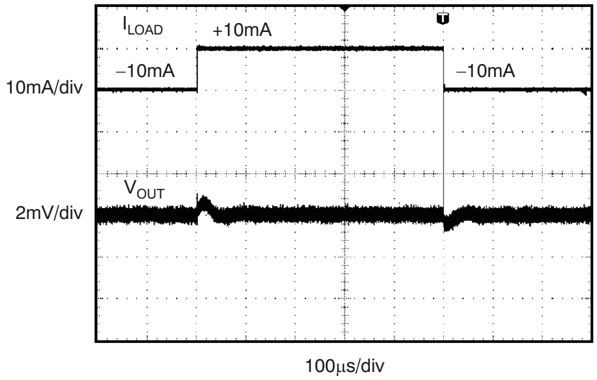


Figure 19.

LINE TRANSIENT
(C_L = 1μF)

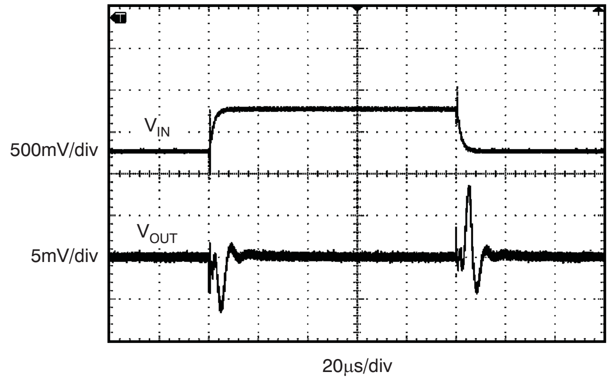


Figure 20.

LINE TRANSIENT
(C_L = 10μF)

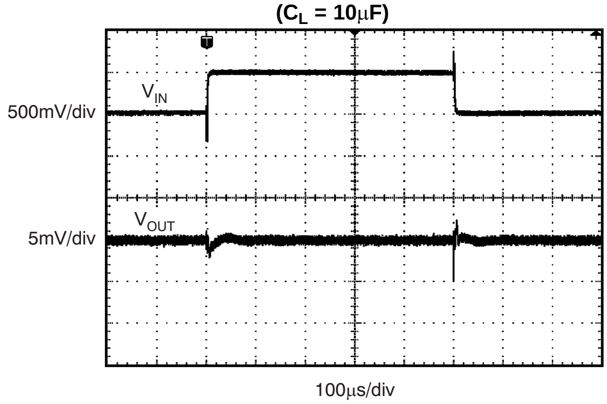


Figure 21.

APPLICATION INFORMATION

The REF50xx is family of low-noise, precision bandgap voltage references that are specifically designed for excellent initial voltage accuracy and drift. Figure 22 shows a simplified block diagram of the REF50xx.

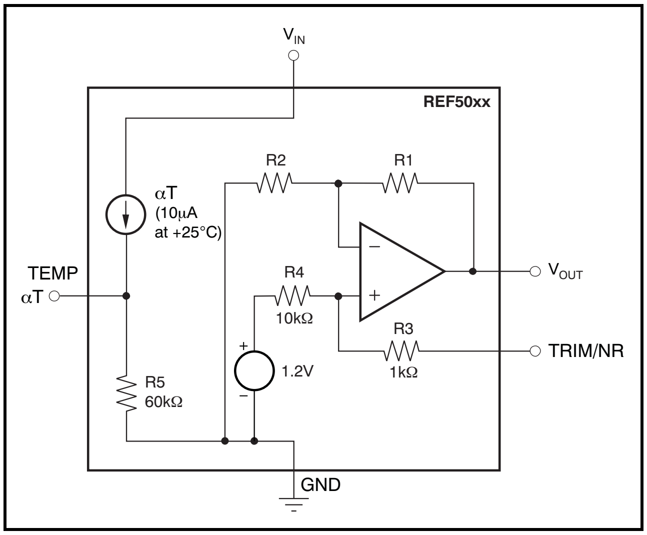


Figure 22. REF50xx Simplified Block Diagram

BASIC CONNECTIONS

Figure 23 shows the typical connections for the REF50xx. A supply bypass capacitor ranging between 1 μF to 10 μF is recommended. A 1-μF to 50-μF output capacitor (C_L) must be connected from V_{OUT} to GND. The ESR value of C_L must be less than or equal to 1.5 Ω to ensure output stability. To minimize noise, the recommended ESR of C_L is between 1 Ω and 1.5 Ω.

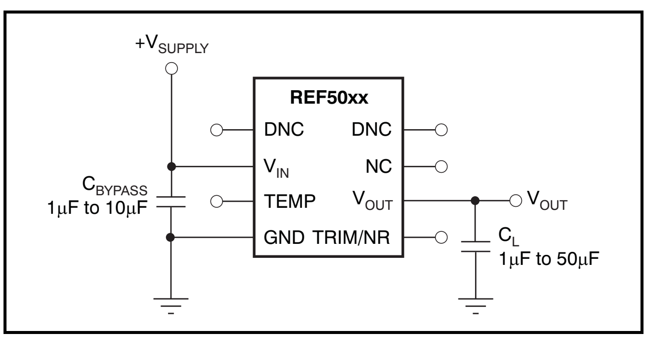


Figure 23. Basic Connections

SUPPLY VOLTAGE

The REF50xx family of voltage references features extremely low dropout voltage. With the exception of the REF5020, which has a minimum supply requirement of 2.7 V, these references can be operated with a supply of 200 mV above the output voltage in an unloaded condition. For loaded conditions, a typical dropout voltage versus load plot is shown in Figure 6 of the Typical Characteristics.

OUTPUT ADJUSTMENT USING THE TRIM/NR PIN

The REF50xx provides a very accurate, factory-trimmed voltage output. However, V_{OUT} can be adjusted using the trim and noise reduction pin (TRIM/NR, pin 5). Figure 24 shows a typical circuit that allows an output adjustment of ±15 mV

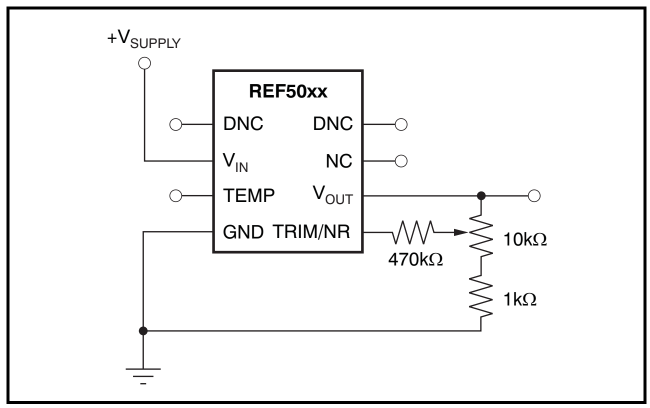


Figure 24. V_{OUT} Adjustment Using the TRIM/NR Pin

The REF50xx allows access to the bandgap through the TRIM/NR pin. Placing a capacitor from the TRIM/NR pin to GND (see Figure 25) in combination with the internal R_3 and R_4 resistors creates a low-pass filter. A capacitance of 1 μF creates a low-pass filter with the corner frequency between 10 Hz and 20 Hz. Such a filter decreases the overall noise measured on the V_{OUT} pin by half. Higher capacitance results in a lower filter cutoff frequency, further reducing output noise. Note that use of this capacitor increases startup time.

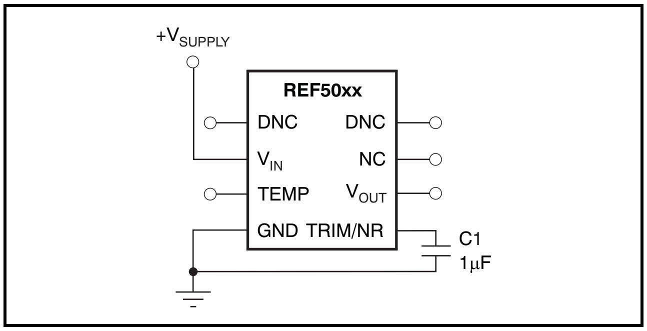


Figure 25. Noise Reduction Using the TRIM/NR Pin

TEMPERATURE DRIFT

The REF50xx is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by the following equation:

$$\text{Drift} = \left(\frac{V_{OUTMAX} - V_{OUTMIN}}{V_{OUT} \times \text{Temp Range}}\right) \times 10^6 (\text{ppm}) \quad (1)$$

The REF50xx features a maximum drift coefficient of 3 ppm/°C for the high-grade version, and 8 ppm/°C for the standard-grade.

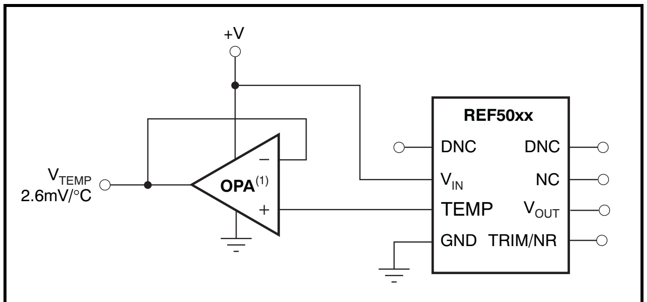
TEMPERATURE MONITORING

The temperature output terminal (TEMP, pin 3) provides a temperature-dependent voltage output with approximately 60-kΩ source impedance. As seen in Figure 8, the output voltage follows the nominal relationship:

$$V_{TEMP\ PIN} = 509\text{ mV} + 2.64 \times T(°C)$$

This pin indicates general chip temperature, accurate to approximately ±15°C. Although it is not generally suitable for accurate temperature measurements, it can be used to indicate temperature changes or for temperature compensation of analog circuitry. A temperature change of 30°C corresponds to an approximate 79 mV change in voltage at the TEMP pin.

The TEMP pin has high output impedance (see Figure 22). Loading this pin with a low-impedance circuit induces a measurement error; however, it does not have any effect on V_{OUT} accuracy. To avoid errors caused by low-impedance loading, buffer the TEMP pin output with a suitable low-temperature drift op amp, such as the OPA333, OPA335, or OPA376, as shown in Figure 26.



NOTE: (1) Low drift op amp, such as the OPA333, OPA335, or OPA376.

Figure 26. Buffering the TEMP Pin Output

POWER DISSIPATION

The REF50xx family is specified to deliver current loads of ±10 mA over the specified input voltage range. The temperature of the device increases according to the equation:

$$T_J = T_A + P_D \times \theta_{JA} \quad (2)$$

Where:

- T_J = Junction temperature (°C)
- T_A = Ambient temperature (°C)
- P_D = Power dissipated (W)
- θ_{JA} = Junction-to-ambient thermal resistance (°C/W)

The REF50xx junction temperature must not exceed the absolute maximum rating of +150°C.

NOISE PERFORMANCE

Typical 0.1-Hz to 10-Hz voltage noise for each member of the REF50xx family is specified in the *Electrical Characteristics: Per Device* table. The noise voltage increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade performance.

APPLICATION CIRCUITS

NEGATIVE REFERENCE VOLTAGE

For applications requiring a negative and positive reference voltage, the REF50xx and OPA735 can be used to provide a dual-supply reference from a 5-V supply. Figure 27 shows the REF5020 used to provide a 2.5-V supply reference voltage. The low drift performance of the REF50xx complements the low offset voltage and zero drift of the OPA735 to provide an accurate solution for split-supply applications. Care must be taken to match the temperature coefficients of R_1 and R_2.

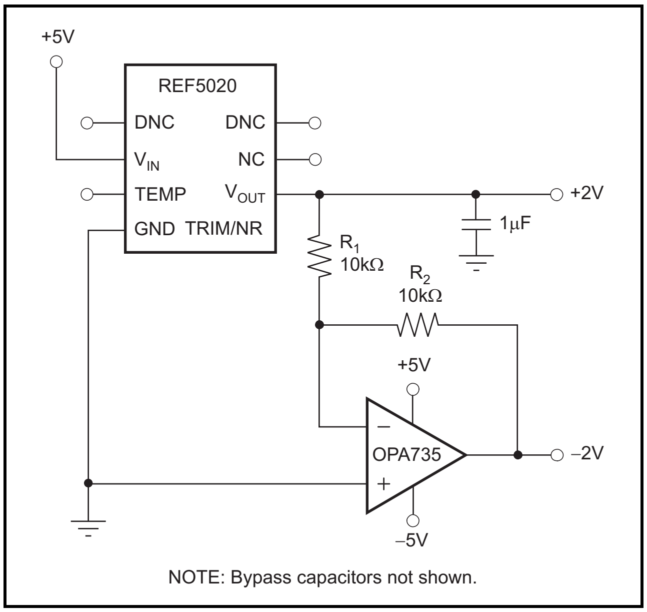


Figure 27. The REF5020 and OPA735 Create Positive and Negative Reference Voltages

DATA ACQUISITION

Data acquisition systems often require stable voltage references to maintain accuracy. The REF50xx family features low noise, very low drift, and high initial accuracy for high-performance data converters. Figure 28 shows the REF5040 in a basic data acquisition system.

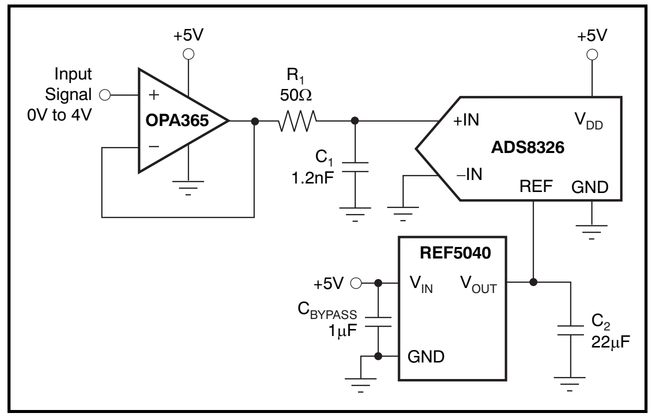


Figure 28. Basic Data Acquisition System

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
REF5020MDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
REF5025MDTEP	ACTIVE	SOIC	D	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
REF5040MDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
REF5050MDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
V62/10613-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
V62/10613-02XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
V62/10613-03XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF REF5020-EP, REF5025-EP, REF5040-EP, REF5050-EP :

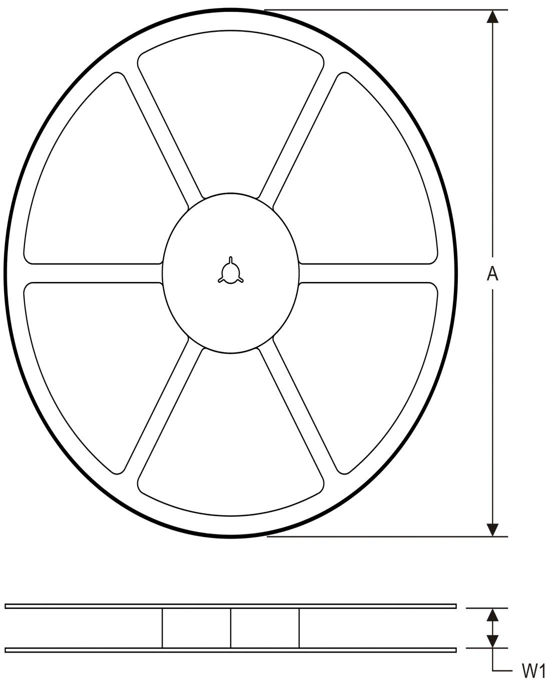
- Catalog: REF5020, REF5025, REF5040, REF5050

NOTE: Qualified Version Definitions:

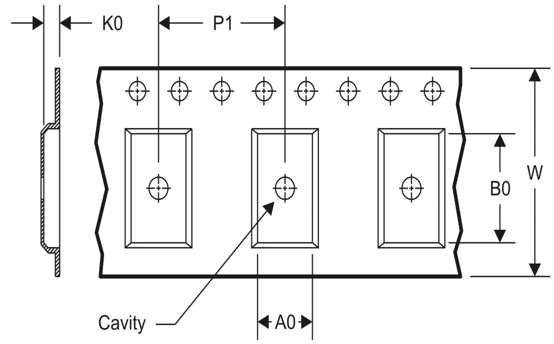
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



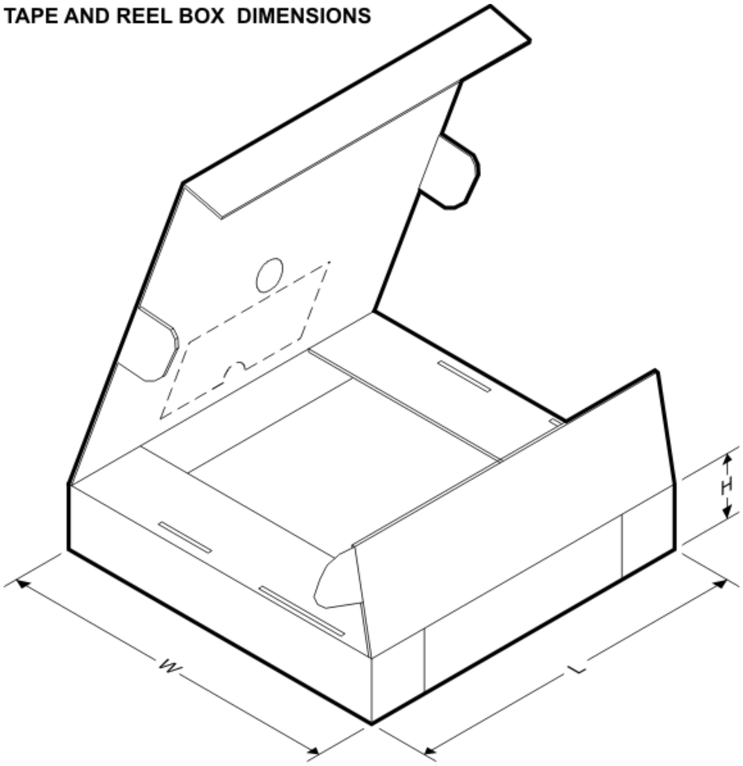
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF5020MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5025MDTEP	SOIC	D	8	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5040MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5050MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

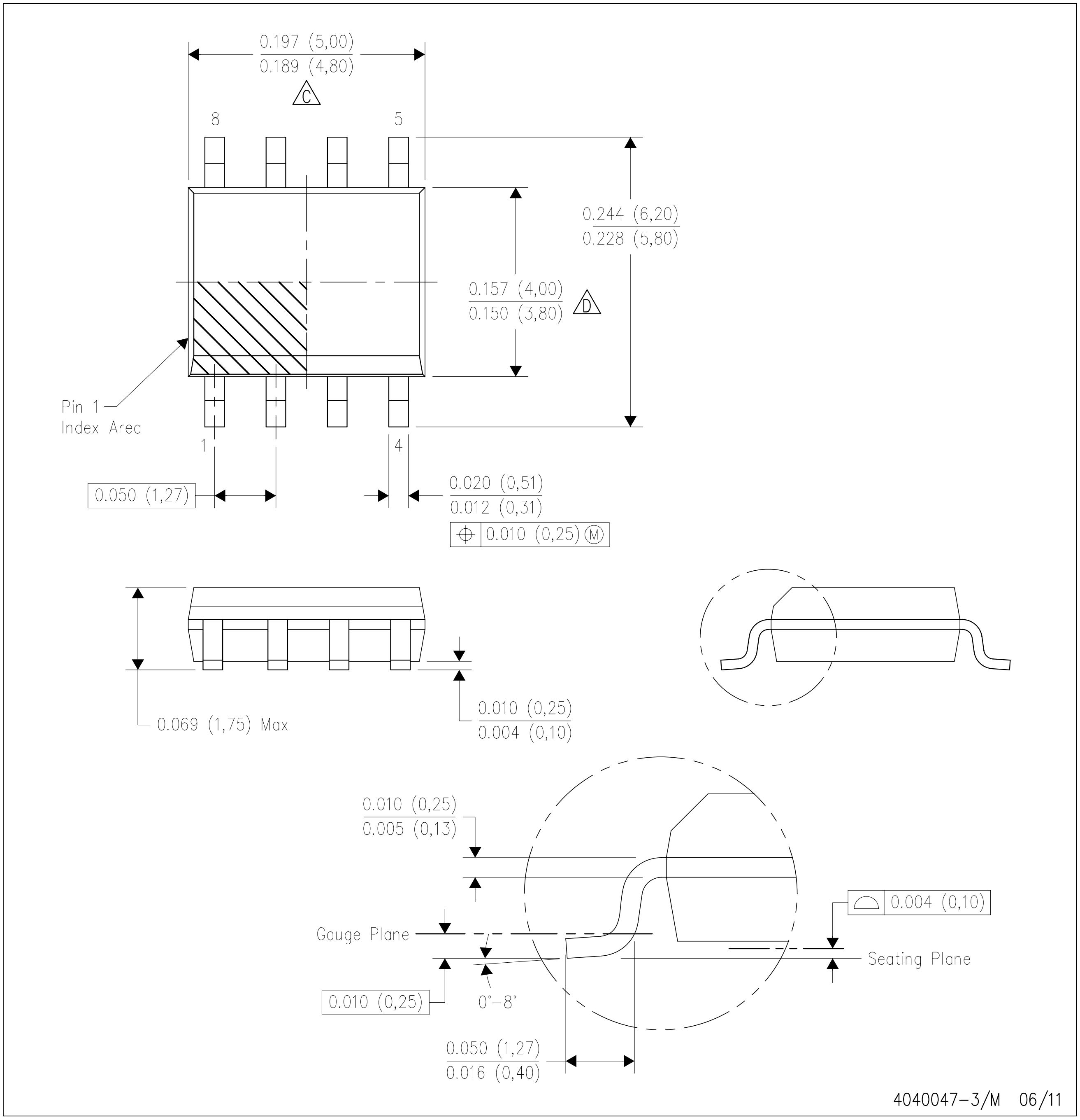
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

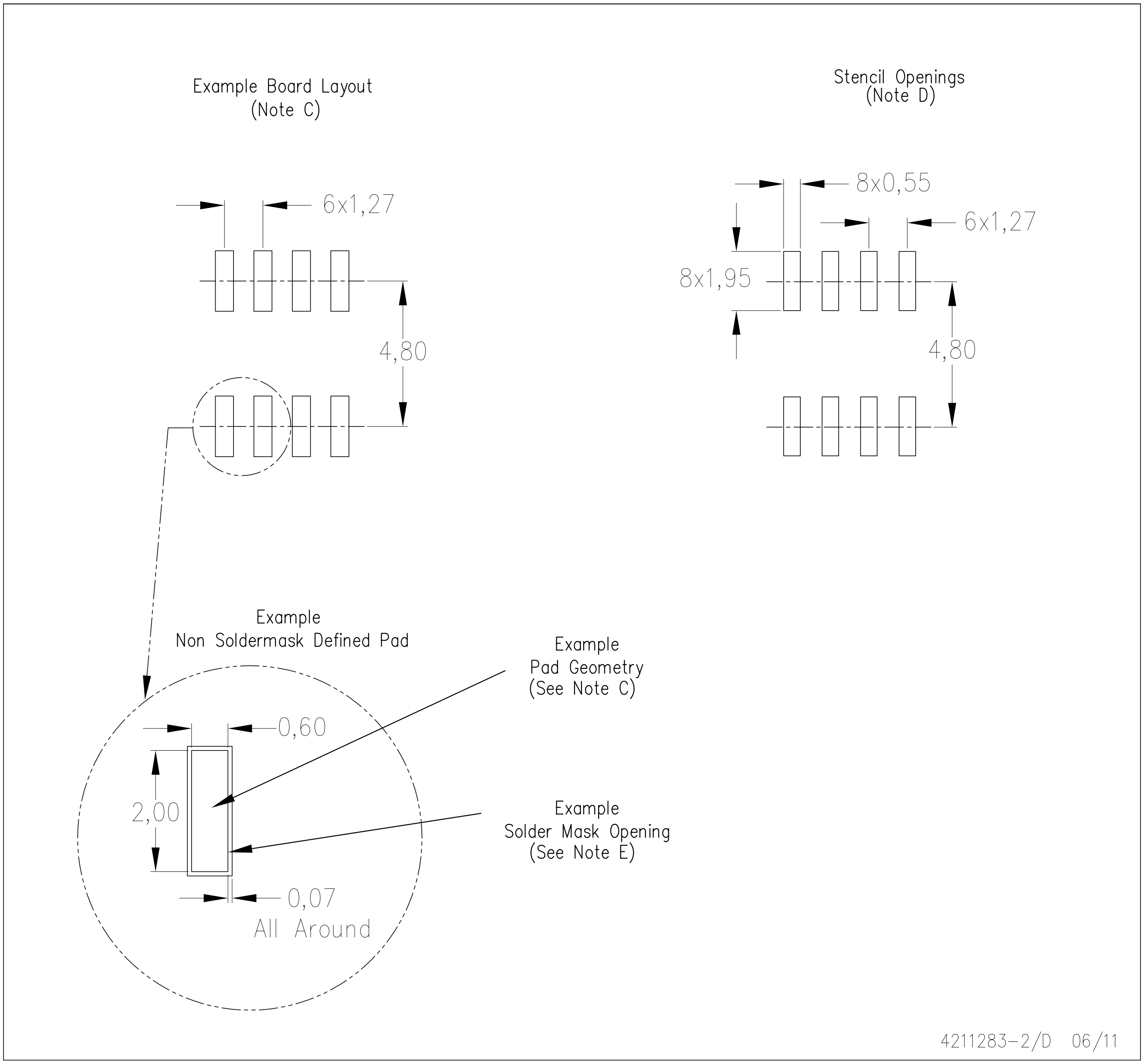
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF5020MDREP	SOIC	D	8	2500	346.0	346.0	29.0
REF5025MDTEP	SOIC	D	8	250	210.0	185.0	35.0
REF5040MDREP	SOIC	D	8	2500	346.0	346.0	29.0
REF5050MDREP	SOIC	D	8	2500	346.0	346.0	29.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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