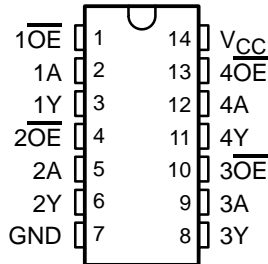


SN54AHC125, SN74AHC125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

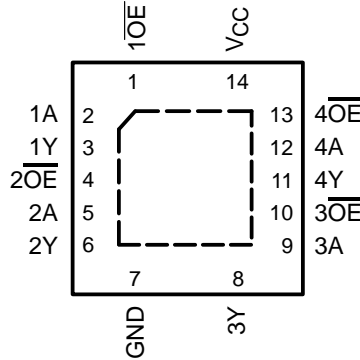
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- Operating Range 2-V to 5.5-V V_{CC}
- Latch-Up Performance Exceeds 250 mA Per JESD 17

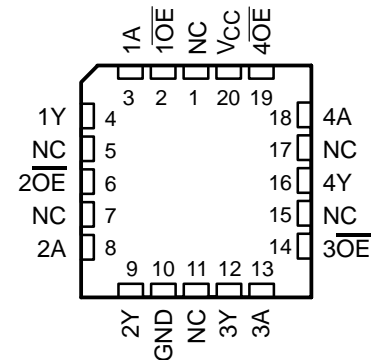
SN54AHC125 . . . J OR W PACKAGE
SN74AHC125 . . . D, DB, DGV, N, NS,
OR PW PACKAGE
(TOP VIEW)



SN74AHC125 . . . RGY PACKAGE
(TOP VIEW)



SN54AHC125 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'AHC125 devices are quadruple bus buffer gates featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high. When \overline{OE} is low, the respective gate passes the data from the A input to its Y output.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Tape and reel	SN74AHC125RGYR	HA125
	PDIP – N	Tube	SN74AHC125N	SN74AHC125N
	SOIC – D	Tube	SN74AHC125D	AHC125
		Tape and reel	SN74AHC125DR	
	SOP – NS	Tape and reel	SN74AHC125NSR	AHC125
	SSOP – DB	Tape and reel	SN74AHC125DBR	HA125
	TSSOP – PW	Tube	SN74AHC125PW	HA125
		Tape and reel	SN74AHC125PWR	
TVSOP – DGV	Tape and reel	SN74AHC125DGVR	HA125	
-55°C to 125°C	CDIP – J	Tube	SNJ54AHC125J	SNJ54AHC125J
	CFP – W	Tube	SNJ54AHC125W	SNJ54AHC125W
	LCCC – FK	Tube	SNJ54AHC125FK	SNJ54AHC125FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

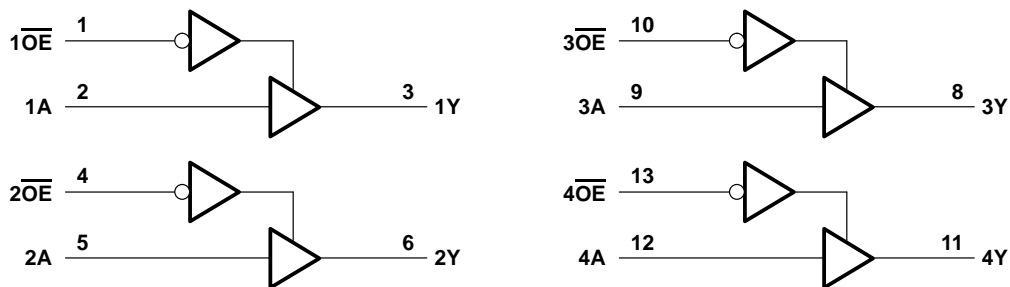
SN54AHC125, SN74AHC125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
(see Note 2): DB package	96°C/W
(see Note 2): DGV package	127°C/W
(see Note 2): N package	80°C/W
(see Note 2): NS package	76°C/W
(see Note 2): PW package	113°C/W
(see Note 3): RGY package	47°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

SN54AHC125, SN74AHC125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

		SN54AHC125		SN74AHC125		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V		1.5	1.5	V
		V _{CC} = 3 V		2.1	2.1	
		V _{CC} = 5.5 V		3.85	3.85	
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5	0.5	V
		V _{CC} = 3 V		0.9	0.9	
		V _{CC} = 5.5 V		1.65	1.65	
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		-50	-50	μA
		V _{CC} = 3.3 V ± 0.3 V		-4	-4	mA
		V _{CC} = 5 V ± 0.5 V		-8	-8	
I _{OL}	Low-level output current	V _{CC} = 2 V		50	50	μA
		V _{CC} = 3.3 V ± 0.3 V		4	4	mA
		V _{CC} = 5 V ± 0.5 V		8	8	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V		100	100	ns/V
		V _{CC} = 5 V ± 0.5 V		20	20	
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC125		SN74AHC125		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	2 V	1.9	2		1.9		1.9	V	
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1		0.1	0.1	V	
		3 V			0.1		0.1	0.1		
		4.5 V			0.1		0.1	0.1		
	I _{OL} = 4 mA	3 V			0.36		0.5	0.44		
	I _{OL} = 8 mA	4.5 V			0.36		0.5	0.44		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*	±1	μA	
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.25		±2.5	±2.5	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40	40	μA	
C _i	V _I = V _{CC} or GND	5 V		4	10			10	pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.



SN54AHC125, SN74AHC125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 V \pm 0.3 V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ C$			SN54AHC125		SN74AHC125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15 \text{ pF}$	5.6*	8*	1*	9.5*	1	9.5	ns	
t_{PHL}				5.6*	8*	1*	9.5*	1	9.5		
t_{PZH}	\overline{OE}	Y	$C_L = 15 \text{ pF}$	5.4*	8*	1*	9.5*	1	9.5	ns	
t_{PZL}				5.4*	8*	1*	9.5*	1	9.5		
t_{PHZ}	\overline{OE}	Y	$C_L = 15 \text{ pF}$	7*	9.7*	1*	11.5*	1	11.5	ns	
t_{PLZ}				7*	9.7*	1*	11.5*	1	11.5		
t_{PLH}	A	Y	$C_L = 50 \text{ pF}$	8.1	11.5	1	13	1	13	ns	
t_{PHL}				8.1	11.5	1	13	1	13		
t_{PZH}	\overline{OE}	Y	$C_L = 50 \text{ pF}$	7.9	11.5	1	13	1	13	ns	
t_{PZL}				7.9	11.5	1	13	1	13		
t_{PHZ}	\overline{OE}	Y	$C_L = 50 \text{ pF}$	9.5	13.2	1	15	1	15	ns	
t_{PLZ}				9.5	13.2	1	15	1	15		
$t_{sk(o)}$	\overline{OE}	Y	$C_L = 50 \text{ pF}$		1.5**				1.5	ns	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 V \pm 0.5 V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ C$			SN54AHC125		SN74AHC125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15 \text{ pF}$	3.8*	5.5*	1*	6.5*	1	6.5	ns	
t_{PHL}				3.8*	5.5*	1*	6.5*	1	6.5		
t_{PZH}	\overline{OE}	Y	$C_L = 15 \text{ pF}$	3.6*	5.1*	1*	6*	1	6	ns	
t_{PZL}				3.6*	5.1*	1*	6*	1	6		
t_{PHZ}	\overline{OE}	Y	$C_L = 15 \text{ pF}$	4.6*	6.8*	1*	8*	1	8	ns	
t_{PLZ}				4.6*	6.8*	1*	8*	1	8		
t_{PLH}	A	Y	$C_L = 50 \text{ pF}$	5.3	7.5	1	8.5	1	8.5	ns	
t_{PHL}				5.3	7.5	1	8.5	1	8.5		
t_{PZH}	\overline{OE}	Y	$C_L = 50 \text{ pF}$	5.1	7.1	1	8	1	8	ns	
t_{PZL}				5.1	7.1	1	8	1	8		
t_{PHZ}	\overline{OE}	Y	$C_L = 50 \text{ pF}$	6.1	8.8	1	10	1	10	ns	
t_{PLZ}				6.1	8.8	1	10	1	10		
$t_{sk(o)}$			$C_L = 50 \text{ pF}$		1**				1	ns	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.



SN54AHC125, SN74AHC125
QUADRUPLE BUS BUFFER GATES
WITH 3-STATE OUTPUTS

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noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER	SN74AHC125		UNIT
	MIN	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}	0.8		V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}	-0.8		V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}	4.4		V
$V_{IH(D)}$ High-level dynamic input voltage	3.5		V
$V_{IL(D)}$ Low-level dynamic input voltage	1.5		V

NOTE 5: Characteristics are for surface-mount packages only.

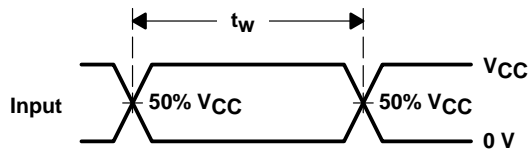
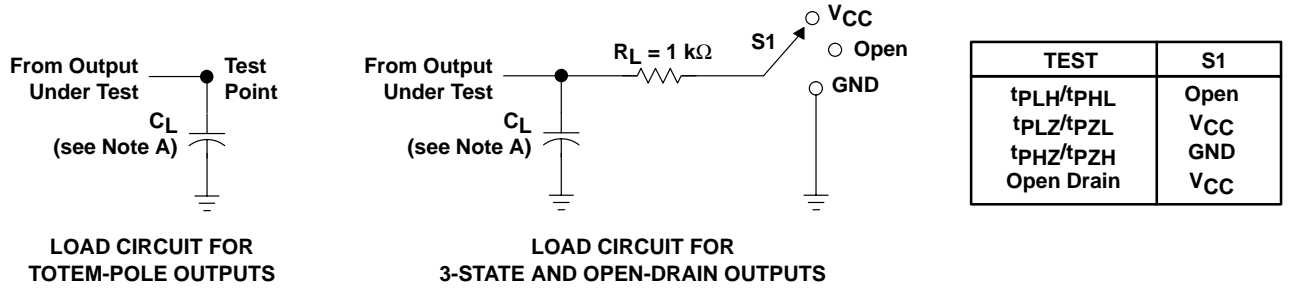
operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	14	pF

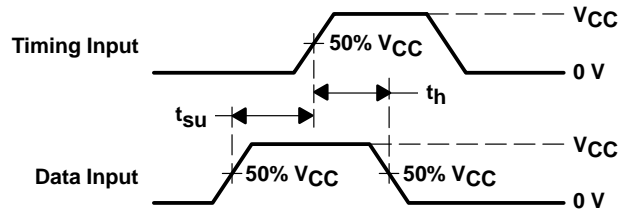
SN54AHC125, SN74AHC125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

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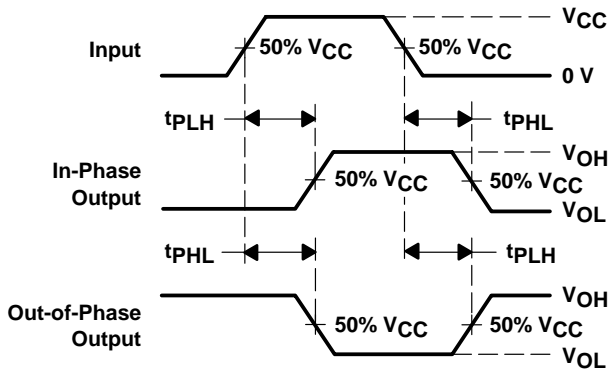
PARAMETER MEASUREMENT INFORMATION



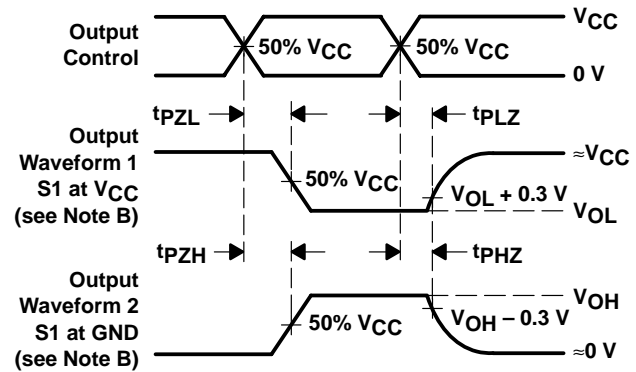
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

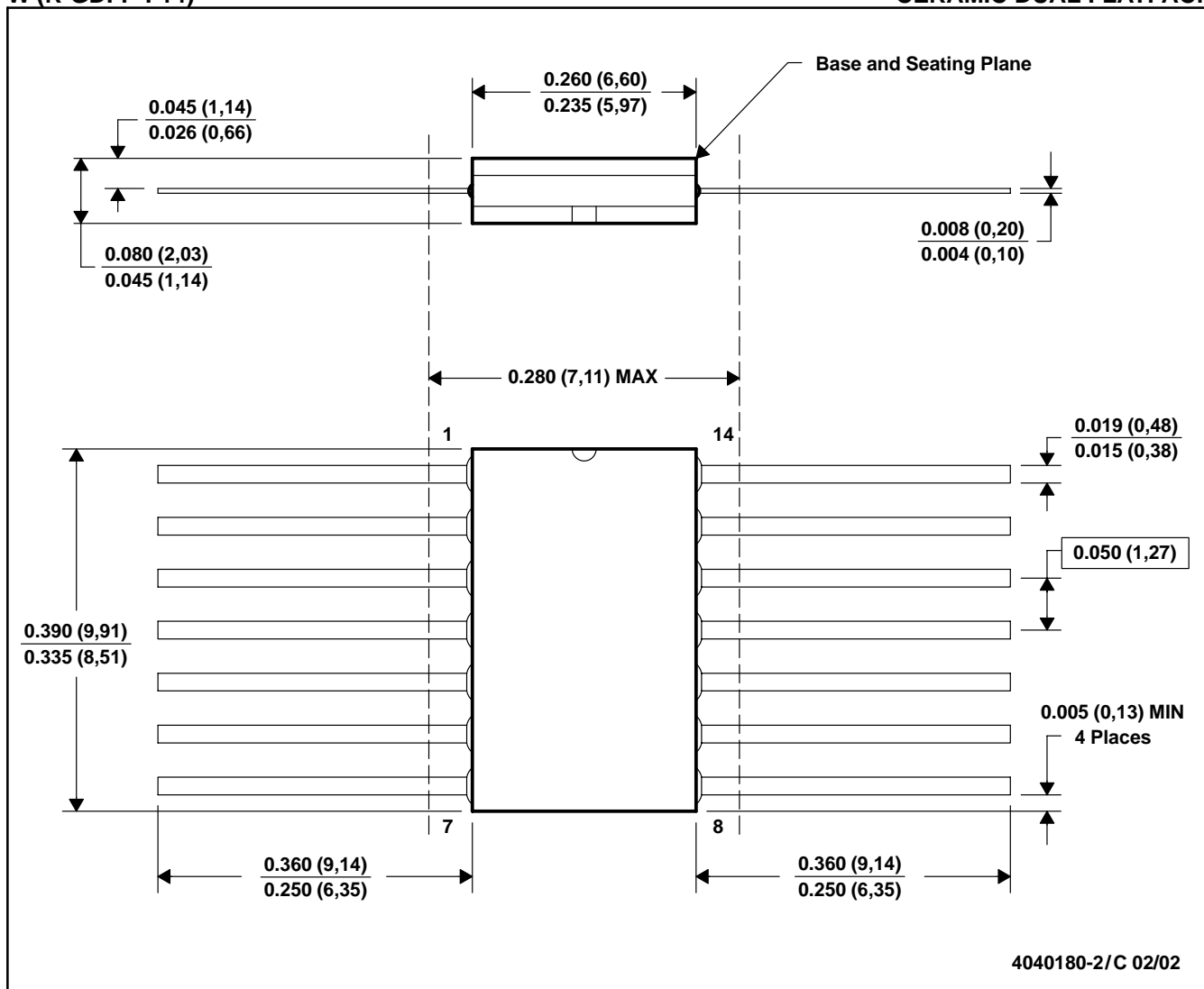


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



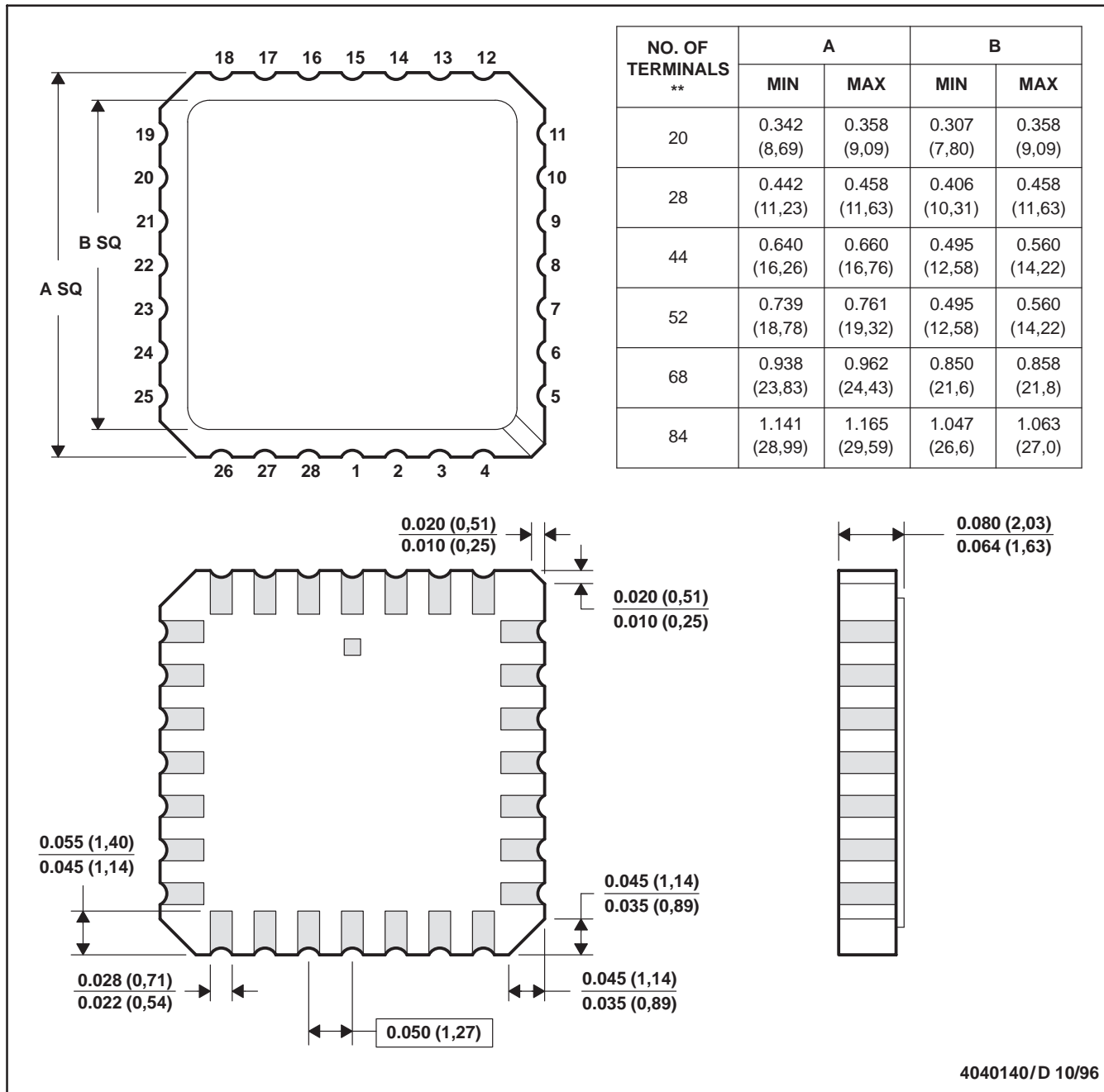
4040180-2/C 02/02

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

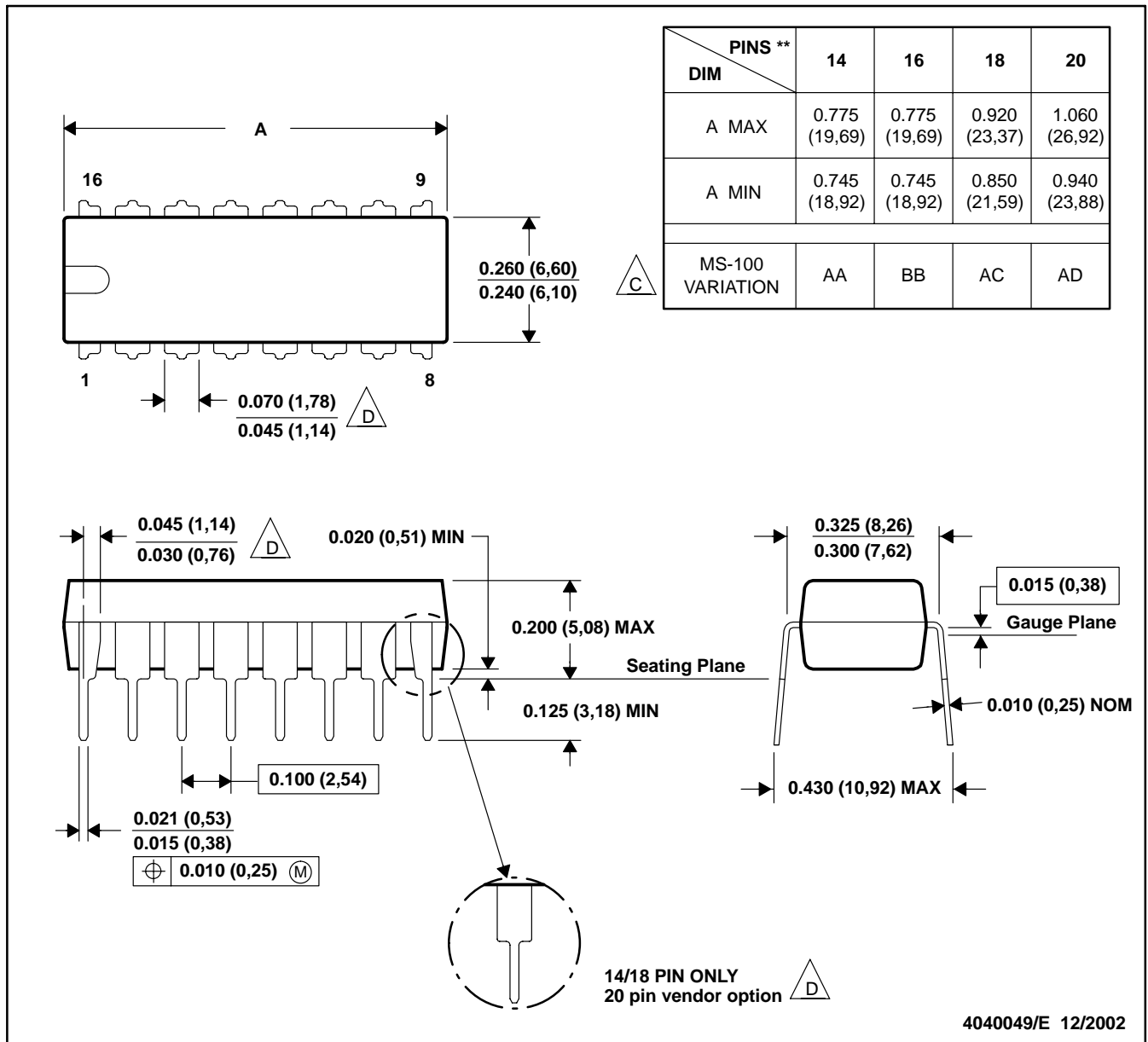


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

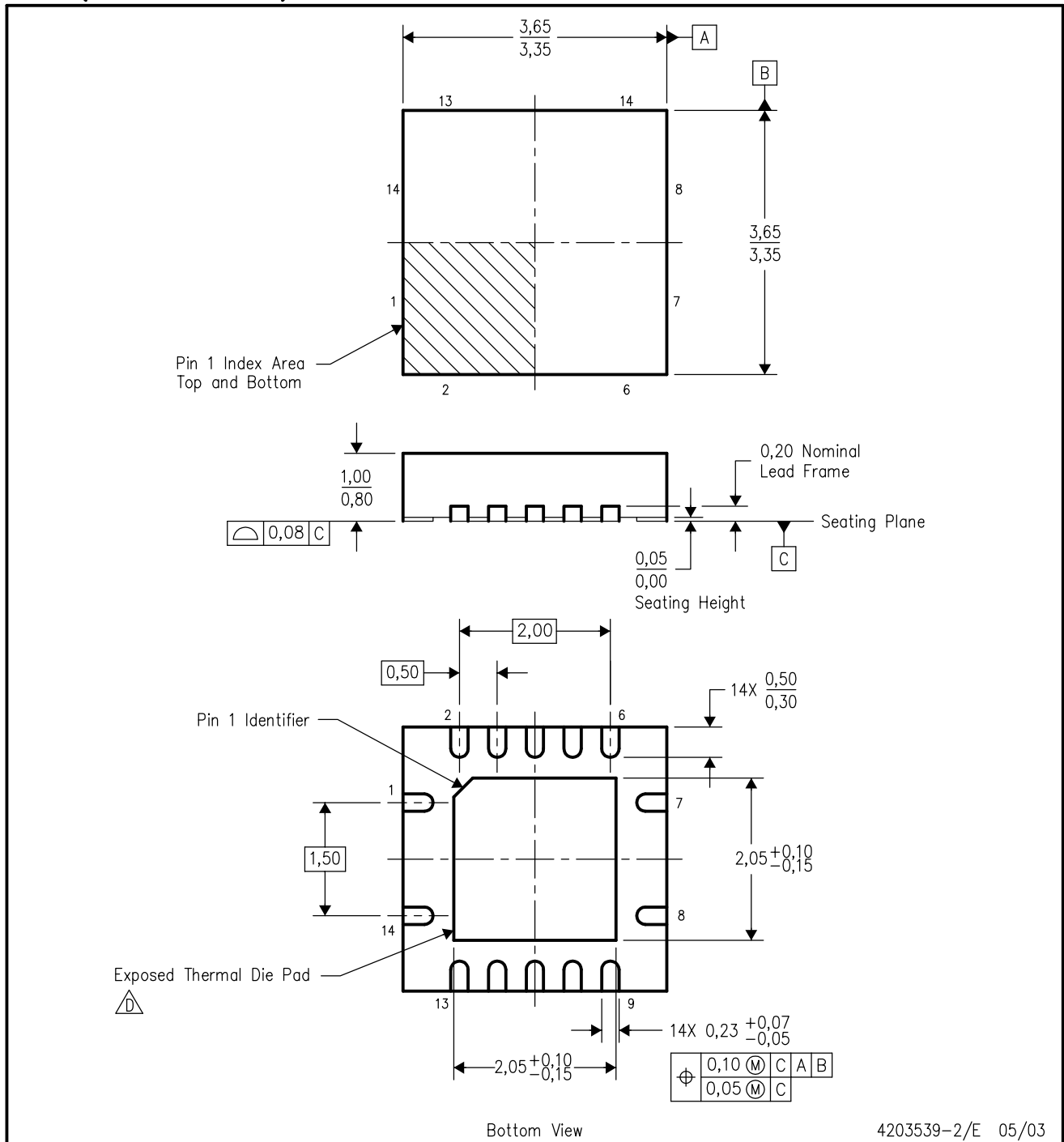
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



Bottom View

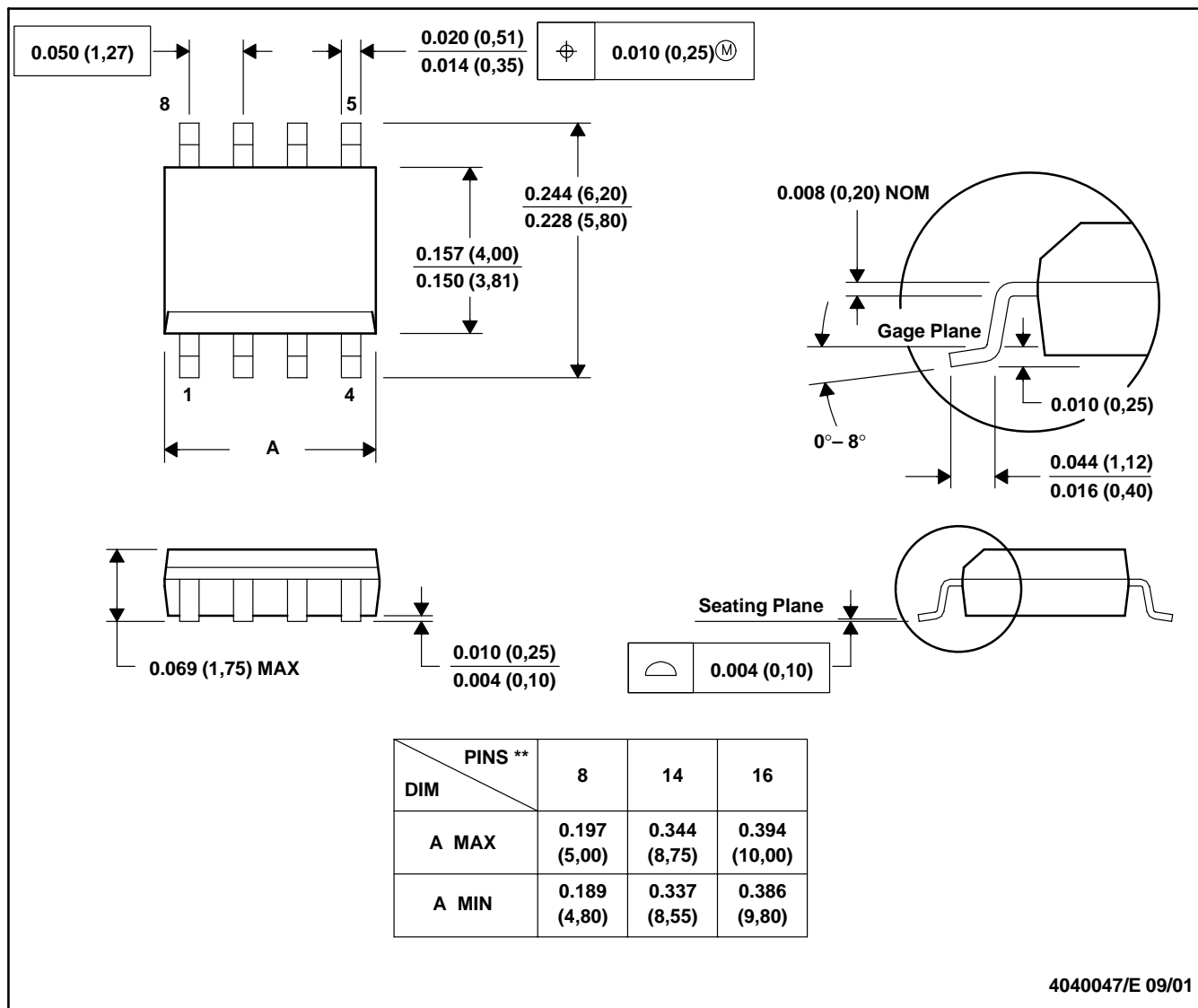
4203539-2/E 05/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - \triangle The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
 - E. Package complies to JEDEC MO-241 variation BA.

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

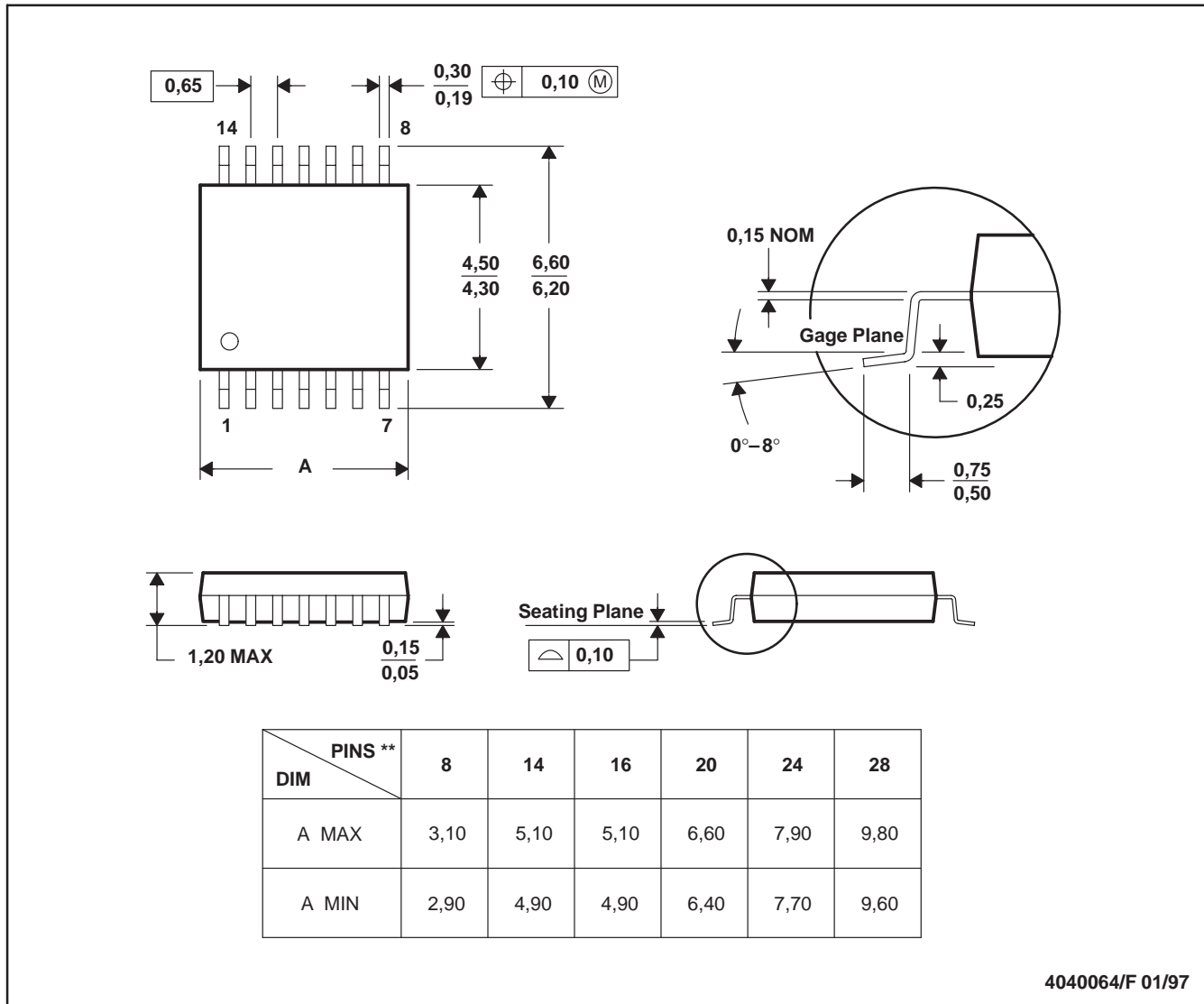


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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