

# SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

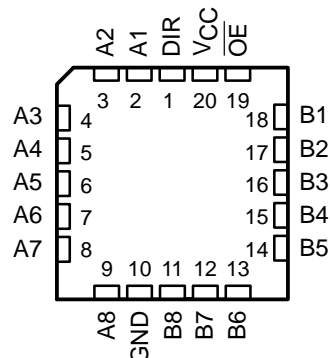
SDAS272A – NOVEMBER 1994 – REVISED JANUARY 2003

- 4.5-V to 5.5-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 5.5 ns at 5 V
- 3-State Outputs Drive Bus Lines Directly
- pnp Inputs Reduce dc Loading

SN54ALS245A . . . J OR W PACKAGE  
SN54AS245 . . . J PACKAGE  
SN74ALS245A . . . DB, DW, N, OR NS PACKAGE  
SN74AS245 . . . DW, N, OR NS PACKAGE  
(TOP VIEW)



SN54ALS245A, SN54AS245 . . . FK PACKAGE  
(TOP VIEW)



description/ordering information

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
0°C to 70°C	PDIP – N	Tube	SN74ALS245A-1N	SN74ALS245A-1N	
			SN74ALS245AN	SN74ALS245AN	
			SN74AS245N	SN74AS245N	
	SOIC – DW	Tube	SN74ALS245ADW	ALS245A	
			SN74ALS245ADWR		
		Tape and reel	SN74ALS245A-1DW	ALS245A-1	
			SN74ALS245A-1DWR		
		Tube	SN74AS245DW	AS245	
			SN74AS245DWR		
	SOP – NS	Tape and reel	SN74ALS245ANSR	ALS245A	
			SN74ALS245A-1NSR	ALS245A-1	
SN74AS245NSR			74AS245		
SSOP – DB	Tape and reel	SN74ALS245ADBR	G245A		
		CDIP – J	Tube	SNJ54ALS245AJ	SNJ54ALS245AJ
				SNJ54AS245J	SNJ54AS245J
CFP – W	Tube	SNJ54ALS245AW	SNJ54ALS245AW		
		LCCC – FK	Tube	SNJ54ALS245AFK	SNJ54ALS245AFK
				SNJ54AS245FK	SNJ54AS245FK
-55°C to 125°C	LCCC – FK	Tube	SNJ54ALS245AFK	SNJ54ALS245AFK	
			SNJ54AS245FK	SNJ54AS245FK	



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 **TEXAS  
INSTRUMENTS**

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# SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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## description/ordering information(continued)

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

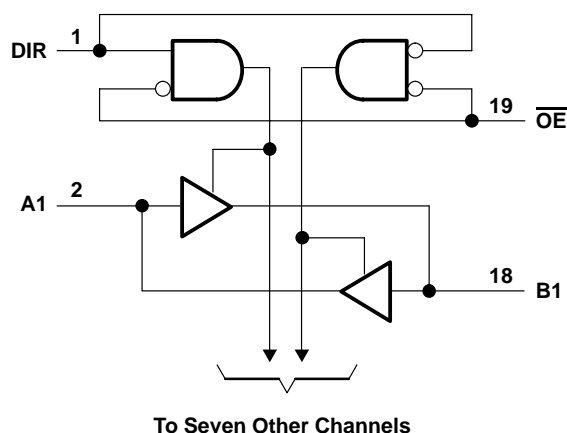
The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

The -1 version of the SN74ALS245A is identical to the standard version, except that the recommended maximum  $I_{OL}$  is increased to 48 mA. There is no -1 version of the SN54ALS245A.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## logic diagram, each gate (positive logic)



## absolute maximum ratings over operating free-air temperature range (SN54ALS245A, SN74ALS245A) (unless otherwise noted)†

Supply voltage, $V_{CC}$ .....	7 V
Input voltage, $V_I$ : All inputs .....	7 V
I/O ports .....	5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 1): DB package .....	70°C/W
DW package .....	58°C/W
N package .....	69°C/W
NS package .....	60°C/W
Storage temperature range .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.



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# SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 2)

		SN54ALS245A			SN74ALS245A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage	0.7			0.8			V
$I_{OH}$	High-level output current	-12			-15			mA
$I_{OL}$	Low-level output current	12			24			mA
					48†			
$T_A$	Operating free-air temperature	-55			125			°C

† Applies only to the -1 version and only if  $V_{CC}$  is between 4.75 V and 5.25 V

NOTE 2: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS245A			SN74ALS245A			UNIT	
				MIN	TYP‡	MAX	MIN	TYP‡	MAX		
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$		-1.5			-1.5			V	
$V_{OH}$		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OH} = -0.4\text{ mA}$		$V_{CC} - 2$			$V_{CC} - 2$			V	
		$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$		2.4	3.2	2.4	3.2			
			$I_{OH} = -12\text{ mA}$		2						
$V_{OL}$		$V_{CC} = 4.5\text{ V}$	$I_{OH} = -15\text{ mA}$		2						
			$I_{OL} = 12\text{ mA}$		0.25	0.4	0.25	0.4			
			$I_{OL} = 24\text{ mA}$				0.35	0.5			
			$I_{OL} = 48\text{ mA}^\dagger$				0.35	0.5	V		
$I_I$	Control inputs	$V_{CC} = 5.5\text{ V}$	$V_I = 7\text{ V}$		0.1			0.1			mA
	A or B ports		$V_I = 5.5\text{ V}$		0.1			0.1			
$I_{IH}$	Control inputs	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$		20			20			$\mu\text{A}$
	A or B ports§				20			20			
$I_{IL}$	Control inputs	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.4\text{ V}$		-0.1			-0.1			mA
	A or B ports§				-0.1			-0.1			
$I_{O}^\parallel$		$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.25\text{ V}$		-20	-112	-30	-112	mA		
$I_{CC}$		$V_{CC} = 5.5\text{ V}$	Outputs high		30	48	30	45	mA		
			Outputs low		36	60	36	55			
			Outputs disabled		38	63	38	58			

† Applies only to the -1 version and only if  $V_{CC}$  is between 4.75 V and 5.25 V

‡ All typical values are  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

¶ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current,  $I_{OS}$ .

# SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245

## OCTAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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#### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54ALS245A		SN74ALS245A		
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	1	19	3	10	ns
t <sub>PHL</sub>			1	14	3	10	
t <sub>PZH</sub>	$\overline{OE}$	A or B	2	30	5	20	ns
t <sub>PZL</sub>			2	29	5	20	
t <sub>PHZ</sub>	$\overline{OE}$	A or B	2	14	2	10	ns
t <sub>PLZ</sub>			2	30	4	15	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

#### absolute maximum ratings over operating free-air temperature range (SN54AS245, SN74AS245) (unless otherwise noted)‡

Supply voltage, V <sub>CC</sub>	7 V
Input voltage, V <sub>I</sub> : All inputs	7 V
I/O ports	5.5 V
Package thermal impedance, θ <sub>JA</sub> (see Note 1): DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 2)

		SN54AS245			SN74AS245			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			–12			–15	mA
I <sub>OL</sub>	Low-level output current			48			64	mA
T <sub>A</sub>	Operating free-air temperature	–55		125	0		70	°C

NOTE 2: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		SN54AS245		SN74AS245		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$		-1.2		-1.2		V	
$V_{OH}$	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OH} = -2\text{ mA}$		$V_{CC} - 2$		$V_{CC} - 2$		V	
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4	3.2	2.4	3.2		
		$I_{OH} = -12\text{ mA}$	2					
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$	0.3 0.55				V	
		$I_{OL} = 64\text{ mA}$			0.35	0.55		
$I_I$	Control inputs	$V_{CC} = 5.5\text{ V}$	$V_I = 7\text{ V}$	0.1		0.1		mA
	A or B ports		$V_I = 5.5\text{ V}$	0.1		0.1		
$I_{IH}$	Control inputs	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$	50		20		$\mu\text{A}$	
	A or B ports‡		70		70			
$I_{IL}$	Control inputs	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$	-0.5		-0.5		mA	
	A or B ports‡		-0.75		-0.75			
$I_O^{\S}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$	-50 -150		-50 -150		mA		
$I_{CC}$	$V_{CC} = 5.5\text{ V}$	Outputs high	62	97	62	97	mA	
		Outputs low	95	143	95	143		
		Outputs disabled	79	123	79	123		

† All typical values are  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current,  $I_{OS}$ .

## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_1 = 500\ \Omega$ , $R_2 = 500\ \Omega$ , $T_A = \text{MIN to MAX}^{\parallel}$				UNIT
			SN54AS245		SN74AS245		
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	2	9.5	2	7.5	ns
$t_{PHL}$			2	9	2	7	
$t_{PZH}$	$\overline{OE}$	A or B	2	11	2	9	ns
$t_{PZL}$			2	10.5	2	8.5	
$t_{PHZ}$	$\overline{OE}$	A or B	2	7.5	2	5.5	ns
$t_{PLZ}$			2	12	2	9.5	

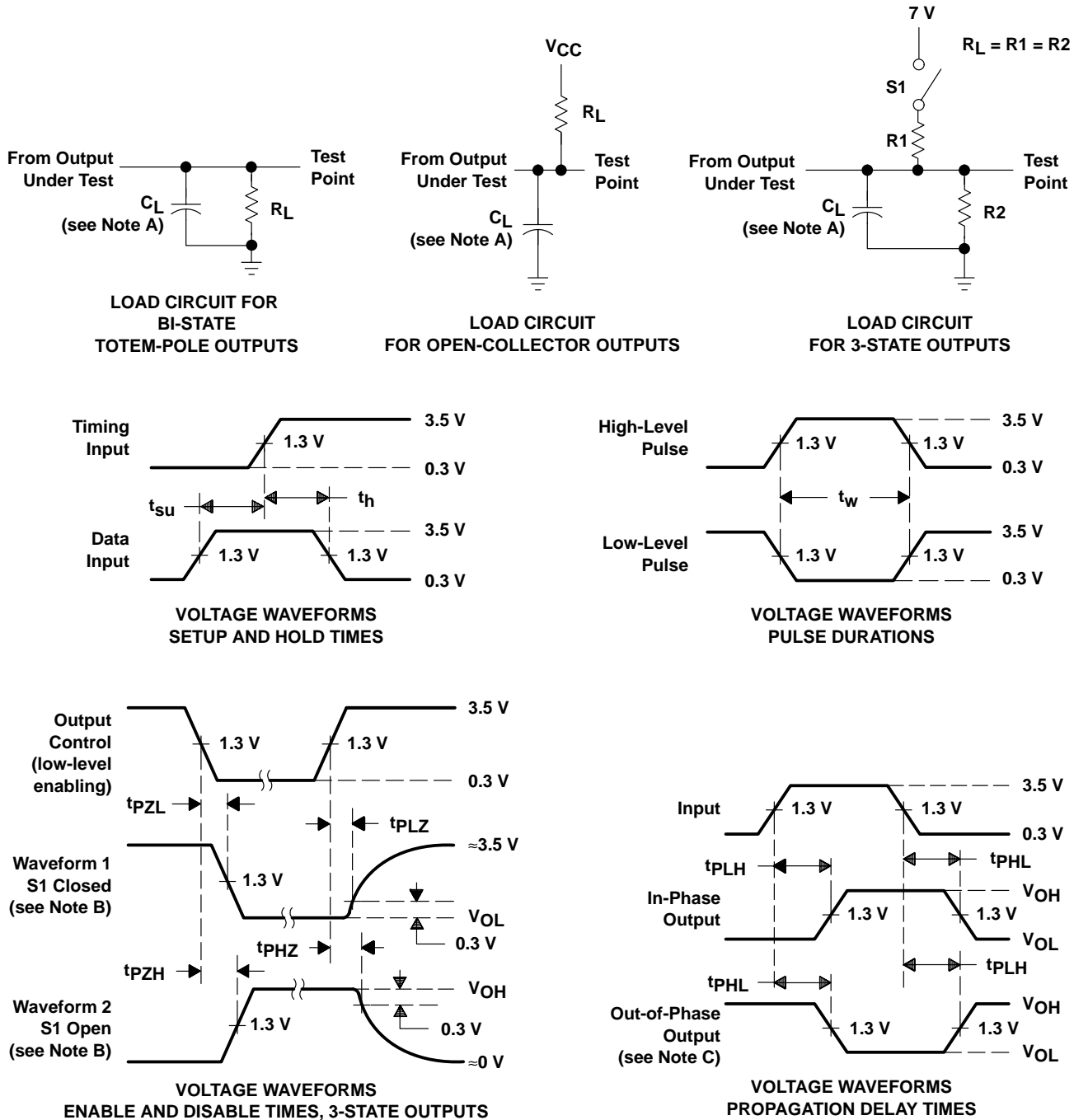
<sup>||</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



**SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245**  
**OCTAL BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

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**PARAMETER MEASUREMENT INFORMATION**  
**SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

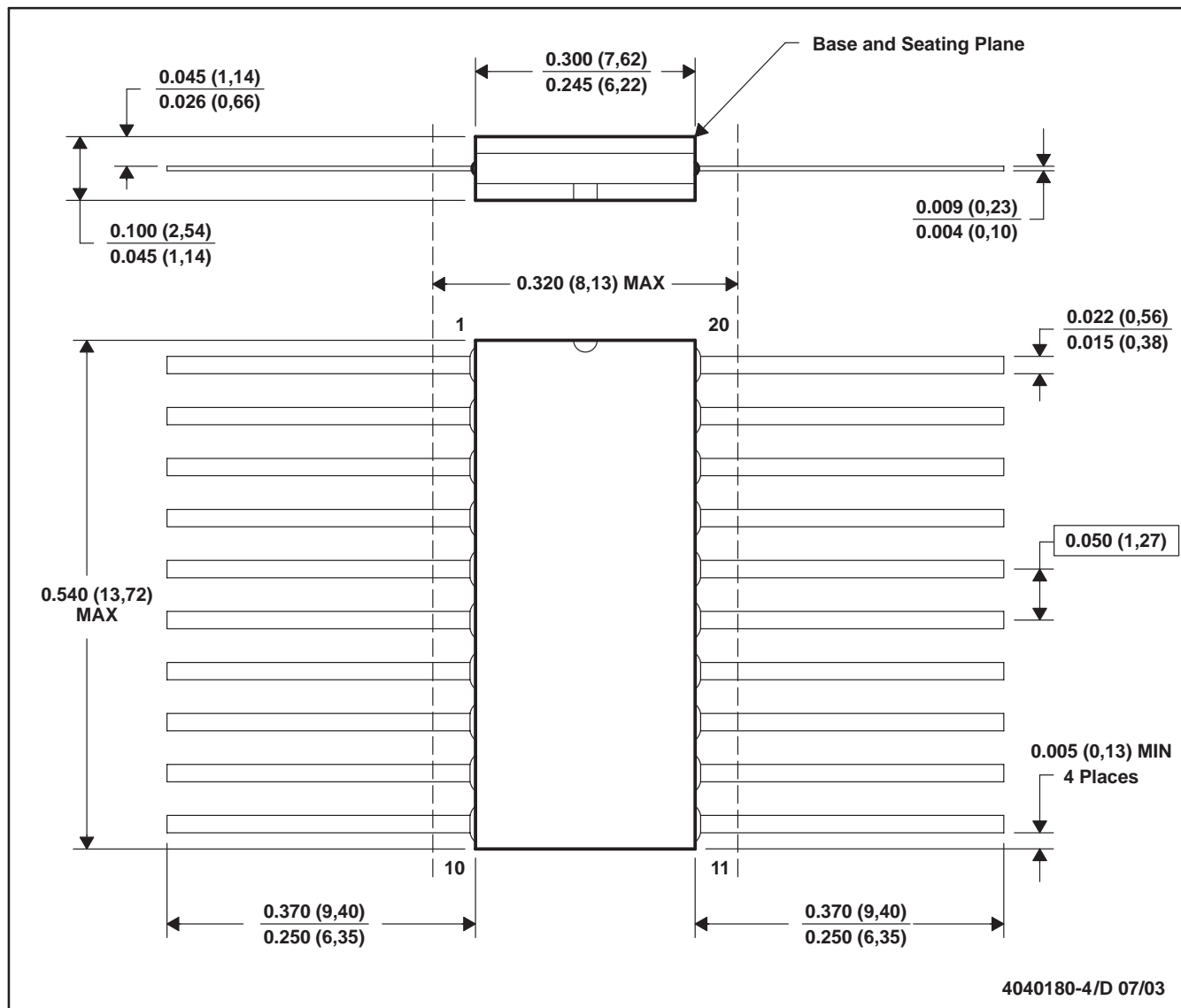


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



4040180-4/D 07/03

- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only.  
 E. Falls within Mil-Std 1835 GDFP2-F20



FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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