

**FFATURFS** 

# 24-BIT FET BUS SWITCH

2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

Check for Samples: SN74CB3T16211

FEATURES	
<ul> <li>Member of the Texas Instruments Widebus™ Family</li> </ul>	DGG, DGV, OR DL PACKAGE (TOP VIEW)
<ul> <li>Output Voltage Translation Tracks V<sub>cc</sub></li> </ul>	
Supports Mixed-Mode Signal Operation on	1A1 2 55 2 <del>0E</del>
All Data I/O Ports	1A2 🛛 3 54 🗍 1B1
<ul> <li>5-V Input Down to 3.3-V Output Level</li> </ul>	1A3 🛛 4 53 🗋 1B2
Shift With 3.3-V V <sub>CC</sub>	1A4 🛛 5 52 🗋 1B3
<ul> <li>5-V/3.3-V Input Down to 2.5-V Output</li> </ul>	1A5 <b>[</b> 6 51 <b>[</b> 1B4
Level Shift With 2.5-V V <sub>cc</sub>	1A6 7 50 1B5
5-V Tolerant I/Os With Device Powered Up	GND 8 49 GND
or Powered Down	
Bidirectional Data Flow With Near-Zero	
Propagation Delay	1A9 [] 11 46 [] 1B8 1A10 [] 12 45 [] 1B9
Low ON-State Resistance (r <sub>on</sub> ) Characteristics	1A10 [ 12 45 ] 1B9 1A11 [ 13 44 ] 1B10
$(r_{on} = 5 \Omega Typ)$	1A12 443 1B10
Low Input/Output Capacitance Minimizes	2A1 15 42 1B12
Loading (C <sub>io(OFF)</sub> = 5 pF Typ)	2A2 16 41 2B1
Data and Control Inputs Provide	V <sub>CC</sub> [] 17 40 [] 2B2
Undershoot Clamp Diodes	2A3 [ 18 39 ] 2B3
Low Power Consumption	GND [] 19 38 ] GND
(I <sub>cc</sub> = 70 μΑ Max)	2A4 🛛 20 🛛 37 🗋 2B4
• V <sub>CC</sub> Operating Range From 2.3 V to 3.6 V	2A5 21 36 2B5
<ul> <li>Data I/Os Support 0- to 5-V Signaling Levels</li> </ul>	2A6 22 35 2B6
(0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)	2A7 23 34 2B7
Control Inputs Can Be Driven by TTL	
or 5-V/3.3-V CMOS Outputs	
<ul> <li>I<sub>off</sub> Supports Partial-Power-Down Mode</li> </ul>	
Operation	2A11 [] 27   30 [] 2B11 2A12 [] 28   29 [] 2B12
Latch-Up Performance Exceeds 250 mA Per	
JESD 17	NC - No internal connection

- **ESD Performance Tested Per JESD 22** •
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- **Supports Digital Applications: Level** . Translation, PCI Interface, Bus Isolation
- Ideal for Low-Power Portable Equipment .



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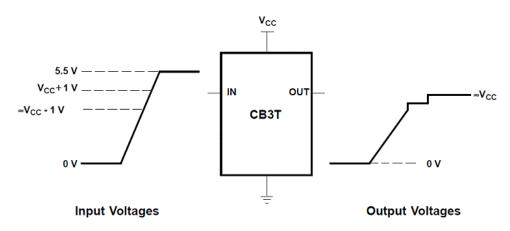


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## **DESCRIPTION/ORDERING INFORMATION**

The SN74CB3T16211 is a high-speed TTL-compatible FET bus switch with low ON-state resistance ( $r_{on}$ ), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V<sub>CC</sub>. The SN74CB3T16211 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).

# DESCRIPTION/ORDERING INFORMATION (CONTINUED)



If the input high voltage (V<sub>IH</sub>) level is greater than or equal to  $V_{CC}$ + 1V, and less than or equal to 5.5 V, the output high voltage (V<sub>OH</sub>) level will be equal to approximately the V<sub>CC</sub> voltage level.

#### Figure 1. Typical DC Voltage-Translation Characteristics

The I/O port of this device has a pullup current source that maintains the output voltage at  $V_{CC}$  when the device is ON, and the input is greater than or equal to  $V_{CC} - 1$ . Because of the pullup current source, the output voltage level may be less than  $V_{CC}$  when the operating frequency is low and the I/O port is connected to a pulldown resistor. In order to maintain the output voltage at  $V_{CC}$ , a pullup resistor must be connected to  $V_{CC}$  instead of a pulldown resistor to ground.

The SN74CB3T16211 is organized as two 12-bit bus switches with separate output-enable  $(1\overline{OE}, 2\overline{OE})$  inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When  $\overline{OE}$  is low, the associated 12-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated 12-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SSOP – DL	Tube	SN74CB3T16211DL	- CB3T16211
	550P - DL	Tape and reel	SN74CB3T16211DLR	CD3110211
	TOOOD DOO	Tube	SN74CB3T16211DGG	000740044
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74CB3T16211DGGR	- CB3T16211
	TVSOP – DGV	Tape and reel	SN74CB3T16211DGVR	KR211
	VFBGA – GQL (Pb-free)	Tape and reel	SN74CB3T16211GQLR	KR211
	VFBGA – ZQL (Pb-free)	Tape and reel	SN74CB3T16211ZQLR	KR211

#### Table 1. ORDERING INFORMATION

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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1       2       3       4       5       6         A       O       O       O       O       O       O         B       O       O       O       O       O       O       O         C       O       O       O       O       O       O       O       O         D       O       O       O       O       O       O       O       O         F       O       O       O       O       O       O       O       O         G       O       O       O       O       O       O       O       O         J       O       O       O       O       O       O       O       O         K       O       O       O       O       O       O       O       O		GQL OR ZQL PACKAGE (TOP VIEW)						
B       O O O O O O O         C       O O O O O O O         D       O O O O O O O         E       O O O O O O O         F       O O O O O O O         G       O O O O O O O         H       O O O O O O O         J       O O O O O O O		1	2	3	4	5	6	
C 000000 D 000000 E 00 000 F 00 000 G 000000 H 000000 J 000000	A	́С	С	С	С	С	0	
□ 000000 = 00 00 F 00 00 G 000000 H 000000 J 000000	в	С	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
E 00 00 F 00 00 G 000000 H 000000 J 000000	с	С	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
F         O O         O O           G         O O O O O O         O           H         O O O O O O         O           J         O O O O O O O         O	D	С	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
с с с с с с с с с с с с с с	Е	С	$\bigcirc$			$\bigcirc$	$\bigcirc$	
H 000000	F	С	$\bigcirc$			$\bigcirc$	$\bigcirc$	
1 000000	G	С	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
	н	С	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
K COCOCO	J	С	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
	к	С	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	

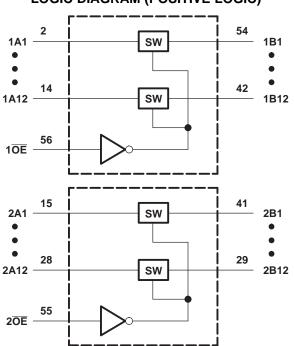
Table 2	2. TERN	IINAL A	SSIGN	MENTS	

	1	2	3	4	5	6
Α	1A2	1A1	NC <sup>(1)</sup>	1 <del>0E</del>	2 <mark>0E</mark>	1B1
В	1A5	1A4	1A3	1B2	1B3	1B4
С	1A7	GND	1A6	1B5	GND	1B6
D	1A10	1A8	1A9	1B8	1B7	1B9
Е	1A12	1A11			1B10	1B11
F	2A1	2A2			2B1	1B12
G	V <sub>CC</sub>	GND	2A3	2B3	GND	2B2
н	2A4	2A5	2A6	2B6	2B5	2B4
J	2A7	2A8	2A9	2B9	2B8	2B7
к	2A10	2A11	2A12	2B12	2B11	2B10

(1) NC - No internal connection

# Table 3. FUNCTION TABLE (EACH 12-BIT BUS SWITCH)

	INPUT/OUTPUT A	FUNCTION
L	В	A port = B port
Н	Z	Disconnect



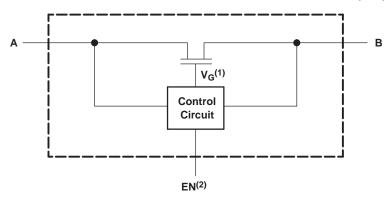
#### LOGIC DIAGRAM (POSITIVE LOGIC)

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#### SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



- (1) Gate voltage (V<sub>G</sub>) is approximately equal to V<sub>CC</sub> + V<sub>T</sub> when the switch is ON and V<sub>I</sub> > V<sub>CC</sub> + V<sub>T</sub>.
- (2) Internal enable signal applied to the switch

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range <sup>(2)</sup>	Supply voltage range <sup>(2)</sup>			
V <sub>IN</sub>	Control input voltage range <sup>(2)</sup> (3)		-0.5	7	V
V <sub>I/O</sub>	Switch I/O voltage range <sup>(2) (3) (4)</sup>		-0.5	7	V
I <sub>IK</sub>	Control input clamp current	V <sub>IN</sub> < 0		-50	mA
I <sub>I/OK</sub>	I/O port clamp current	V <sub>I/O</sub> < 0		-50	mA
I <sub>I/O</sub>	ON-state switch current <sup>(5)</sup>			±128	mA
	Continuous current through V <sub>CC</sub> or GND			±100	mA
		DGG package		64	
0	Deales as the arreal interaction of (6)	DGV package		48	°C/W
$\theta_{JA}$	Package thermal impedance <sup>(6)</sup>	DL package		56	-C/W
		GQL/ZQL package		42	
T <sub>stg</sub>	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground, unless otherwise specified.

(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(4)  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .

(5)  $I_{I}$  and  $I_{O}$  are used to denote specific conditions for  $I_{I/O}$ 

(6) The package thermal impedance is calculated in accordance with JESD 51-7.

# **Recommended Operating Conditions**<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.3	3.6	V
V <sub>IH</sub>	High lovel control input veltage	$V_{CC}$ = 2.3 V to 2.7 V	1.7	5.5	V
	High-level control input voltage $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	5.5	v	
	Low-level control input voltage $\frac{V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}}{V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}}$	0	0.7	N	
VIL		0	0.8	V	
V <sub>I/O</sub>	/I/O Data input/output voltage			5.5	V
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

 All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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## Electrical Characteristics<sup>(1)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

P/	ARAMETER	TEST CONDITIONS			TYP <sup>(2)</sup>	MAX	UNIT
V <sub>IK</sub>		$V_{CC} = 3 V, I_{I} = -18 mA$				-1.2	V
V <sub>ОН</sub>		See Figure 3 and Figure 4					
I <sub>IN</sub>	Control inputs	$V_{CC}$ = 3.6 V, $V_{IN}$ = 3.6 V to 5.5 V or GN	D			±10	μA
			$V_{I} = V_{CC} - 0.7 \text{ V to } 5.5 \text{ V}$			±20	
I <sub>I</sub>		$V_{CC} = 3.6 \text{ V}$ , Switch ON, $V_{IN} = V_{CC}$ or GND	$V_{\rm I}$ = 0.7 V to $V_{\rm CC}$ – 0.7 V			-40	μA
			$V_{I} = 0$ to 0.7 V			±5	
$I_{OZ}$ <sup>(3)</sup> $V_{CC} = 3.6 \text{ V}, V_O = 0 \text{ to } 5.5 \text{ V}, V_I = 0,$ Switch OFF, $V_{IN} = V_{CC} \text{ or GND}$					±10	μA	
I <sub>off</sub>		$V_{CC} = 0, V_{O} = 0$ to 5.5 V, $V_{I} = 0$				10	μA
		$V_{CC} = 3.6 \text{ V}, \text{ I}_{I/O} = 0,$	$V_I = V_{CC}$ or GND			70	
ICC		Switch ON or OFF, $V_{IN} = V_{CC}$ or GND	V <sub>I</sub> = 5.5 V			70	μA
$\Delta I_{CC}$ <sup>(4)</sup>	Control inputs	$V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0 Other inputs at $V_{CC}$ or GND	0.6 V,			300	μA
C <sub>in</sub>	Control inputs	$V_{CC}$ = 3.3 V, $V_{IN}$ = $V_{CC}$ or GND			4		pF
Cio(OFF)		$V_{CC}$ = 3.3 V, $V_{I/O}$ = 5.5 V, 3.3 V, or GNI Switch OFF, $V_{IN}$ = $V_{CC}$ or GND	D,		5		pF
<u> </u>		$V_{CC} = 3.3 V$ , Switch ON,	$V_{I/O} = 5.5 \text{ V or } 3.3 \text{ V}$		5		~F
C <sub>io(ON)</sub>		$V_{IN} = V_{CC}$ or GND	$V_{I/O} = GND$		13		pF
		$V_{CC} = 2.3 \text{ V}, \text{ TYP at } V_{CC} = 2.5 \text{ V},$	I <sub>O</sub> = 24 mA		5	9.5	
r <sub>on</sub> <sup>(5)</sup>		$V_1 = 0$	I <sub>O</sub> = 16 mA		5	9.5	Ω
		$y_{1} = 2y_{1}y_{2} = 0$	I <sub>O</sub> = 64 mA		5	8.5	
		$V_{CC} = 3 V, V_{I} = 0$	I <sub>O</sub> = 32 mA		5	8.5	

(1)

(2)

(3)

 $V_{IN}$  and  $I_{IN}$  refer to control inputs.  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to data pins. All typical values are at  $V_{CC} = 3.3$  V (unless otherwise noted),  $T_A = 25^{\circ}$ C. For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current. This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND. (4)

(5) Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

# **Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

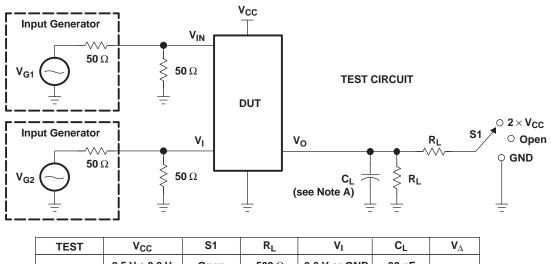
PARAMETER	FROM (INPUT)	TO	V <sub>CC</sub> = ± 0.2		V <sub>CC</sub> = 3 ± 0.3	3.3 V 8 V	UNIT
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	
t <sub>pd</sub> <sup>(1)</sup>	A or B	B or A		0.15		0.25	ns
t <sub>en</sub>	OE	A or B	1	12	1	10	ns
t <sub>dis</sub>	OE	A or B	1	7.5	1	8.5	ns

The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load (1) capacitance, when driven by an ideal voltage source (zero output impedance).

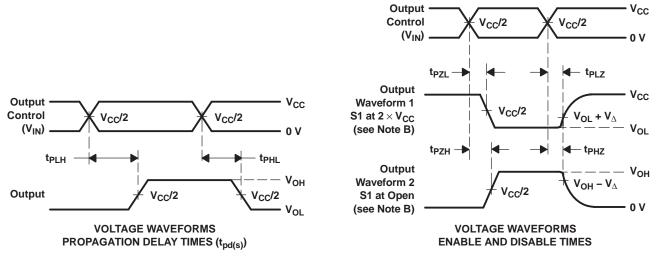
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TEST	VCC	51	ĸL	٧I	UL L	$\mathbf{v}_{\Delta}$
t <sub>pd(s)</sub>	$2.5 V \pm 0.2 V$ $3.3 V \pm 0.3 V$	Open Open	<b>500</b> Ω <b>500</b> Ω	3.6 V or GND 5.5 V or GND	30 pF 50 pF	
t <sub>PLZ</sub> /t <sub>PZL</sub>	$\begin{array}{c} 2.5 \ V \pm 0.2 \ V \\ 3.3 \ V \pm 0.3 \ V \end{array}$	$2 \times V_{CC}$ $2 \times V_{CC}$	<b>500</b> Ω <b>500</b> Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	$\begin{array}{c} \textbf{2.5 V} \pm \textbf{0.2 V} \\ \textbf{3.3 V} \pm \textbf{0.3 V} \end{array}$	Open Open	<b>500</b> Ω <b>500</b> Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V



NOTES: A. C<sub>1</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>0</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{\text{PZL}}$  and  $t_{\text{PZH}}$  are the same as  $t_{\text{en}}.$
- G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd(s)</sub>. The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

#### Figure 2. Test Circuit and Voltage Waveforms



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**TYPICAL CHARACTERISTICS** 

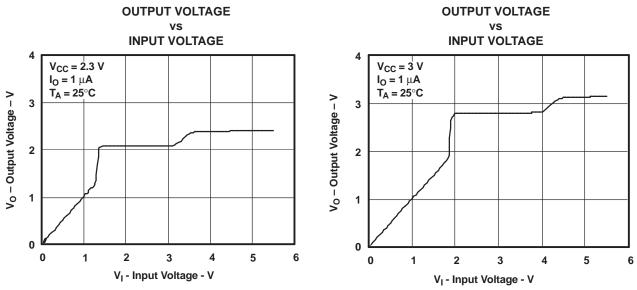
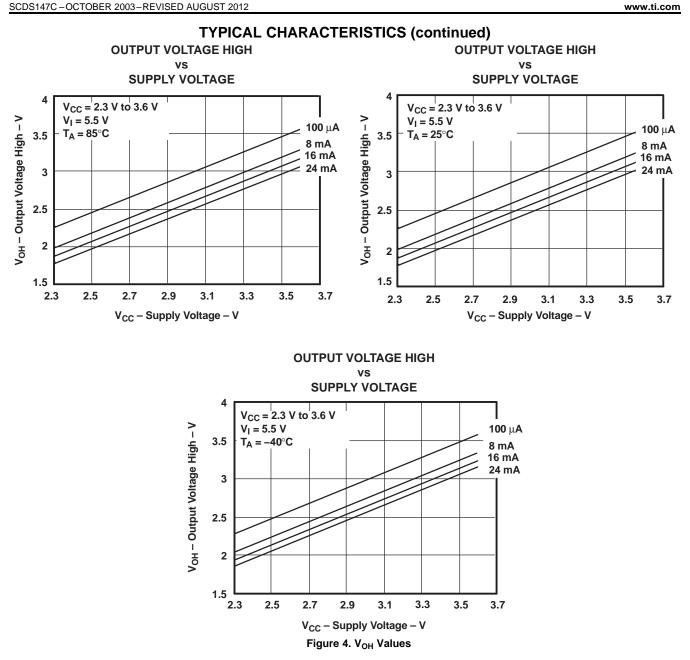


Figure 3. Data Output Voltage vs Data Input Voltage

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# **REVISION HISTORY**

Cł	Changes from Revision B (January 2006) to Revision C						
•	Updated graphic and note in figure 1.	2					



3-May-2012

## **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
74CB3T16211DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74CB3T16211DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74CB3T16211DGVRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74CB3T16211DGVRG4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74CB3T16211DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74CB3T16211DGG	PREVIEW	TSSOP	DGG	56	35	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74CB3T16211DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74CB3T16211DGVR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74CB3T16211DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74CB3T16211DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74CB3T16211DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74CB3T16211GQLR	LIFEBUY	BGA MICROSTAR JUNIOR	GQL	56	1000	TBD	SNPB	Level-1-240C-UNLIM	
SN74CB3T16211ZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.



3-May-2012

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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# PACKAGE MATERIALS INFORMATION

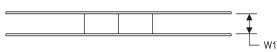
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## TAPE AND REEL INFORMATION

#### REEL DIMENSIONS

Texas Instruments





TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3T16211DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74CB3T16211DGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1
SN74CB3T16211DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN74CB3T16211GQLR	BGA MI CROSTA R JUNI OR	GQL	56	1000	330.0	16.4	4.8	7.3	1.45	8.0	16.0	Q1
SN74CB3T16211ZQLR	BGA MI CROSTA R JUNI OR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1

TEXAS INSTRUMENTS

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# PACKAGE MATERIALS INFORMATION

17-Aug-2012

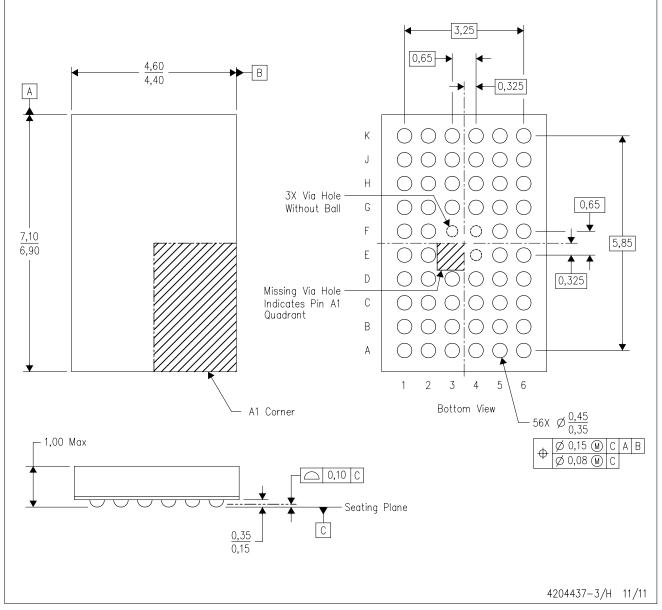


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3T16211DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74CB3T16211DGVR	TVSOP	DGV	56	2000	367.0	367.0	45.0
SN74CB3T16211DLR	SSOP	DL	56	1000	367.0	367.0	55.0
SN74CB3T16211GQLR	BGA MICROSTAR JUNIOR	GQL	56	1000	333.2	345.9	28.6
SN74CB3T16211ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	333.2	345.9	28.6

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is Pb-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

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# **MECHANICAL DATA**

PLASTIC SMALL-OUTLINE

MPDS006C - FEBRUARY 1996 - REVISED AUGUST 2000

## DGV (R-PDSO-G\*\*)

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

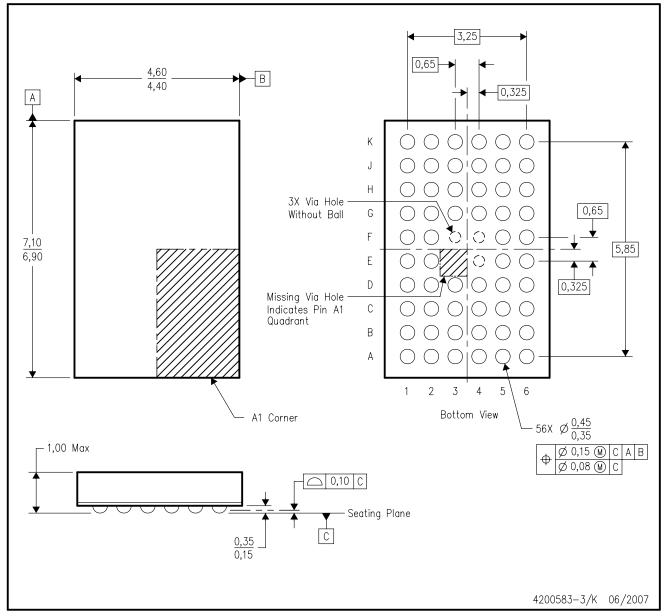
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins MO-153

14/16/20/56 Pins – MO-194



GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.



# **MECHANICAL DATA**

MSSO001C - JANUARY 1995 - REVISED DECEMBER 2001

#### PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

DL (R-PDSO-G\*\*)



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118



# **MECHANICAL DATA**

MTSS003D - JANUARY 1995 - REVISED JANUARY 1998

#### DGG (R-PDSO-G\*\*)

### PLASTIC SMALL-OUTLINE PACKAGE

**48 PINS SHOWN** 



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



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