24-BIT FET BUS SWITCH
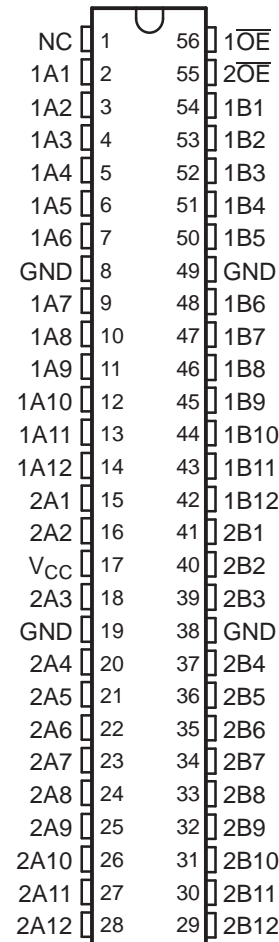# 2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

Check for Samples: SN74CB3T16211

FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **Output Voltage Translation Tracks V_{CC}**
- **Supports Mixed-Mode Signal Operation on All Data I/O Ports**
  - **5-V Input Down to 3.3-V Output Level Shift With 3.3-V V_{CC}**
  - **5-V/3.3-V Input Down to 2.5-V Output Level Shift With 2.5-V V_{CC}**
- **5-V Tolerant I/Os With Device Powered Up or Powered Down**
- **Bidirectional Data Flow With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 5 Ω Typ)**
- **Low Input/Output Capacitance Minimizes Loading ($C_{io(OFF)}$ = 5 pF Typ)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 70 µA Max)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Digital Applications: Level Translation, PCI Interface, Bus Isolation**
- **Ideal for Low-Power Portable Equipment**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)

|			
NC	1	56	1$\overline{OE}$
1A1	2	55	2$\overline{OE}$
1A2	3	54	1B1
1A3	4	53	1B2
1A4	5	52	1B3
1A5	6	51	1B4
1A6	7	50	1B5
GND	8	49	GND
1A7	9	48	1B6
1A8	10	47	1B7
1A9	11	46	1B8
1A10	12	45	1B9
1A11	13	44	1B10
1A12	14	43	1B11
2A1	15	42	1B12
2A2	16	41	2B1
V_{CC}	17	40	2B2
2A3	18	39	2B3
GND	19	38	GND
2A4	20	37	2B4
2A5	21	36	2B5
2A6	22	35	2B6
2A7	23	34	2B7
2A8	24	33	2B8
2A9	25	32	2B9
2A10	26	31	2B10
2A11	27	30	2B11
2A12	28	29	2B12

NC - No internal connection

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Widebus is a trademark of Texas Instruments.

TEXAS INSTRUMENTS

DESCRIPTION/ORDERING INFORMATION

The SN74CB3T16211 is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T16211 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).

DESCRIPTION/ORDERING INFORMATION (CONTINUED)
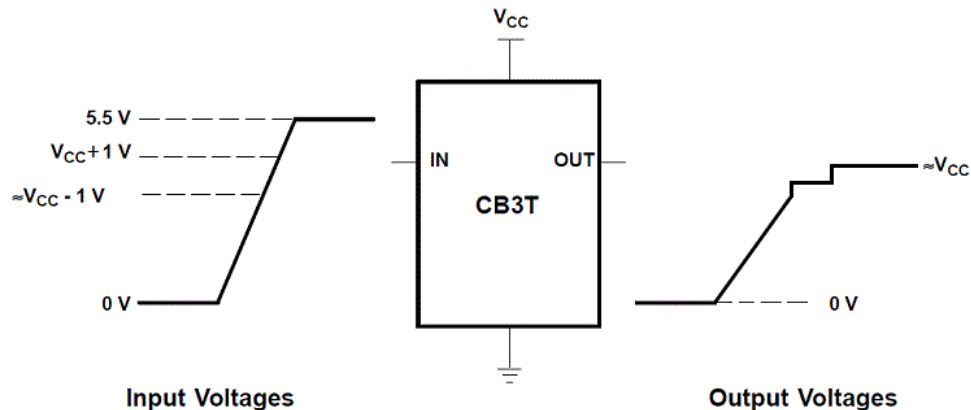
If the input high voltage (V_{IH}) level is greater than or equal to V_{CC}+ 1V, and less than or equal to 5.5 V, the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage-Translation Characteristics

The I/O port of this device has a pullup current source that maintains the output voltage at V_{CC} when the device is ON, and the input is greater than or equal to $V_{CC} - 1$. Because of the pullup current source, the output voltage level may be less than V_{CC} when the operating frequency is low and the I/O port is connected to a pulldown resistor. In order to maintain the output voltage at V_{CC}, a pullup resistor must be connected to V_{CC} instead of a pulldown resistor to ground.

The SN74CB3T16211 is organized as two 12-bit bus switches with separate output-enable ($1\overline{OE}$, $2\overline{OE}$) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When $\overline{OE}$ is low, the associated 12-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 12-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Table 1. ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP – DL	Tube	SN74CB3T16211DL	CB3T16211
		Tape and reel	SN74CB3T16211DLR	
	TSSOP – DGG	Tube	SN74CB3T16211DGG	CB3T16211
		Tape and reel	SN74CB3T16211DGGR	
	TVSOP – DGV	Tape and reel	SN74CB3T16211DGVR	KR211
	VFBGA – GQL (Pb-free)	Tape and reel	SN74CB3T16211GQLR	KR211
	VFBGA – ZQL (Pb-free)	Tape and reel	SN74CB3T16211ZQLR	KR211

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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GQL OR ZQL PACKAGE
(TOP VIEW)
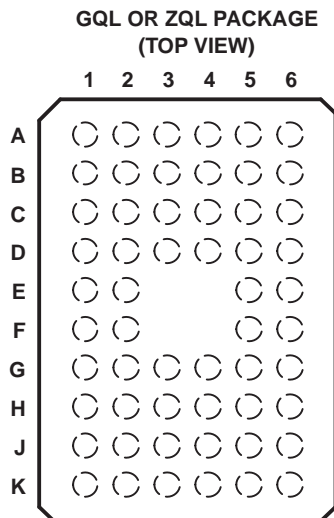
Table 2. TERMINAL ASSIGNMENTS

	1	2	3	4	5	6
A	1A2	1A1	NC[(1)]	1$\overline{OE}$	2$\overline{OE}$	1B1
B	1A5	1A4	1A3	1B2	1B3	1B4
C	1A7	GND	1A6	1B5	GND	1B6
D	1A10	1A8	1A9	1B8	1B7	1B9
E	1A12	1A11			1B10	1B11
F	2A1	2A2			2B1	1B12
G	V_{CC}	GND	2A3	2B3	GND	2B2
H	2A4	2A5	2A6	2B6	2B5	2B4
J	2A7	2A8	2A9	2B9	2B8	2B7
K	2A10	2A11	2A12	2B12	2B11	2B10

(1)   NC – No internal connection

Table 3. FUNCTION TABLE
(EACH 12-BIT BUS SWITCH)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

LOGIC DIAGRAM (POSITIVE LOGIC)
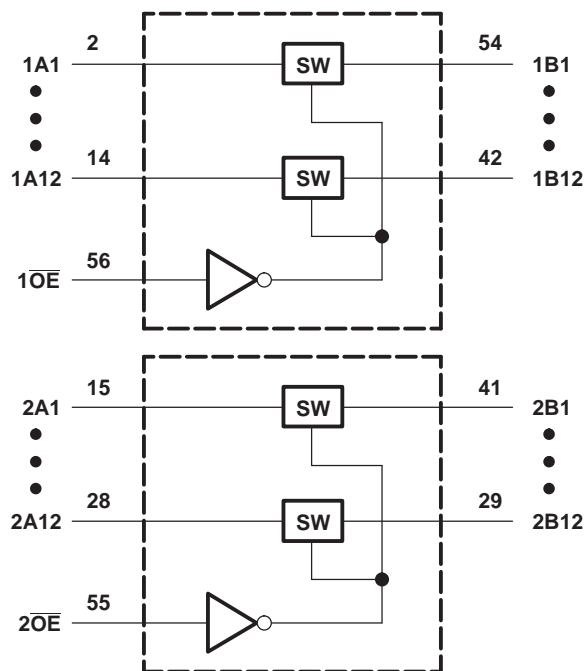
SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)
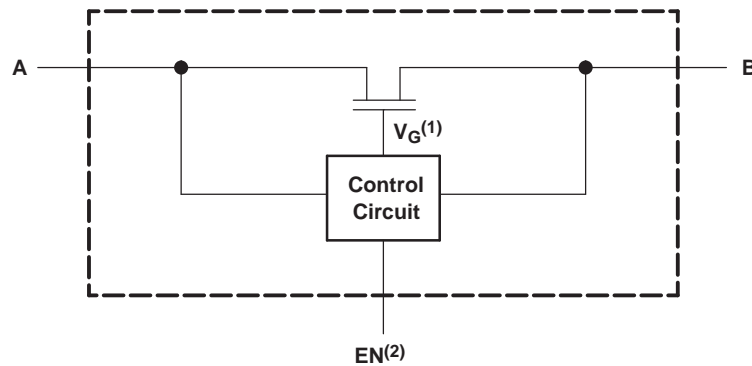
(1) Gate voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.
(2) Internal enable signal applied to the switch

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range[2]		−0.5	7	V
V_{IN}	Control input voltage range[2] [3]		−0.5	7	V
$V_{I/O}$	Switch I/O voltage range[2] [3] [4]		−0.5	7	V
I_{IK}	Control input clamp current	$V_{IN} < 0$		−50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$		−50	mA
$I_{I/O}$	ON-state switch current[5]			±128	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[6]	DGG package		64	°C/W
		DGV package		48	
		DL package		56	
		GQL/ZQL package		42	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Product Folder Links: *SN74CB3T16211*

Electrical Characteristics[1]

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
V_{IK}		V_{CC} = 3 V, I_I = −18 mA				−1.2	V
V_{OH}		See Figure 3 and Figure 4					
I_{IN}	Control inputs	V_{CC} = 3.6 V, V_{IN} = 3.6 V to 5.5 V or GND				±10	µA
I_I		V_{CC} = 3.6 V, Switch ON, V_{IN} = V_{CC} or GND	V_I = V_{CC} − 0.7 V to 5.5 V			±20	µA
			V_I = 0.7 V to V_{CC} − 0.7 V			−40	
			V_I = 0 to 0.7 V			±5	
I_{OZ} [3]		V_{CC} = 3.6 V, V_O = 0 to 5.5 V, V_I = 0, Switch OFF, V_{IN} = V_{CC} or GND				±10	µA
I_{off}		V_{CC} = 0, V_O = 0 to 5.5 V, V_I = 0				10	µA
I_{CC}		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} = V_{CC} or GND	V_I = V_{CC} or GND			70	µA
			V_I = 5.5 V			70	
ΔI_{CC} [4]	Control inputs	V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				300	µA
C_{in}	Control inputs	V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND			4		pF
$C_{io(OFF)}$		V_{CC} = 3.3 V, $V_{I/O}$ = 5.5 V, 3.3 V, or GND, Switch OFF, V_{IN} = V_{CC} or GND			5		pF
$C_{io(ON)}$		V_{CC} = 3.3 V, Switch ON, V_{IN} = V_{CC} or GND	$V_{I/O}$ = 5.5 V or 3.3 V		5		pF
			$V_{I/O}$ = GND		13		
r_{on} [5]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V, V_I = 0	I_O = 24 mA		5	9.5	Ω
			I_O = 16 mA		5	9.5	
		V_{CC} = 3 V, V_I = 0	I_O = 64 mA		5	8.5	
			I_O = 32 mA		5	8.5	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

Switching Characteristics

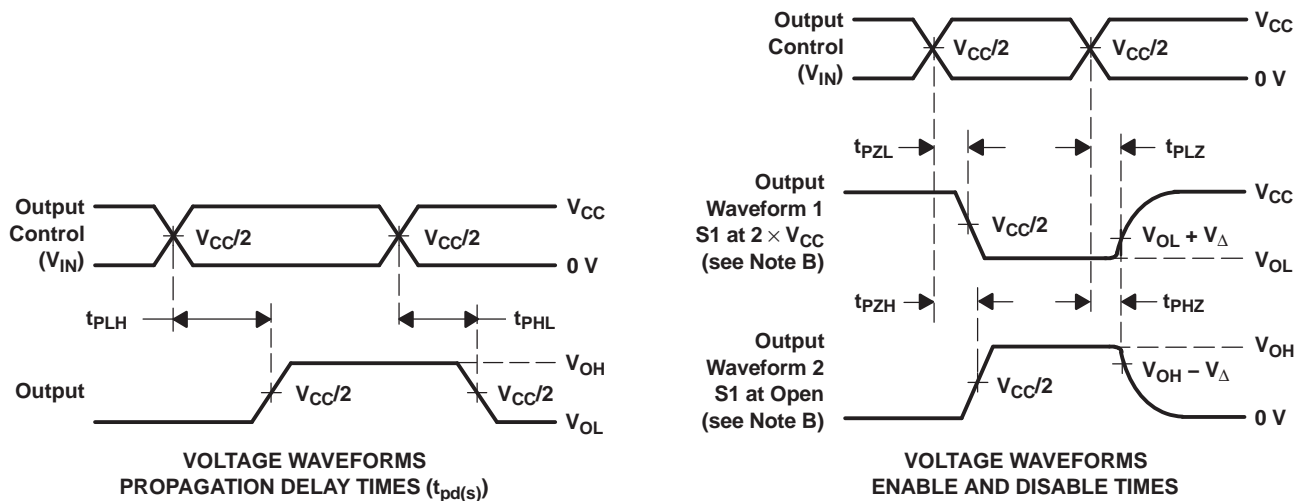over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd} [1]	A or B	B or A		0.15		0.25	ns
t_{en}	$\overline{OE}$	A or B	1	12	1	10	ns
t_{dis}	$\overline{OE}$	A or B	1	7.5	1	8.5	ns

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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SN74CB3T16211

PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT
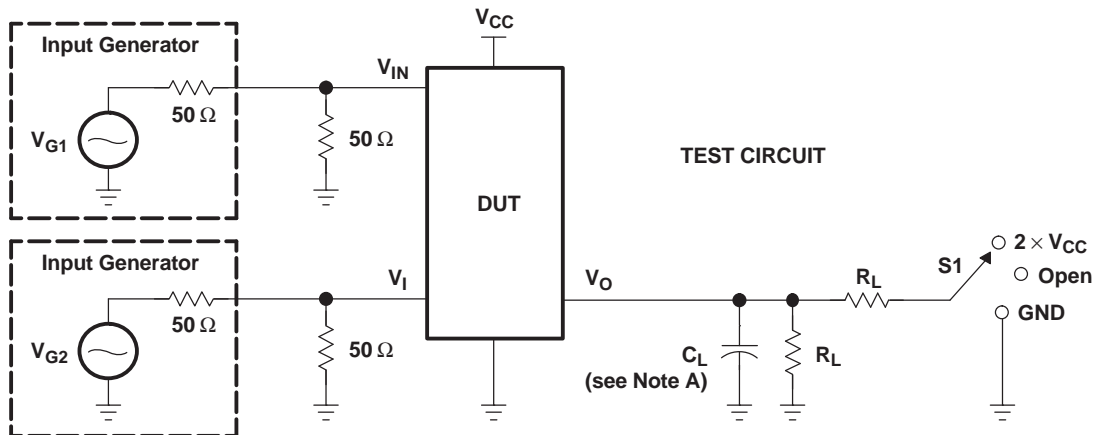
TEST	V$_{CC}$	S1	R$_L$	V$_I$	C$_L$	V$_\Delta$
t$_{pd(s)}$	2.5 V ± 0.2 V	Open	500 Ω	3.6 V or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	5.5 V or GND	50 pF	
t$_{PLZ}$/t$_{PZL}$	2.5 V ± 0.2 V	2 × V$_{CC}$	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V$_{CC}$	500 Ω	GND	50 pF	0.3 V
t$_{PHZ}$/t$_{PZH}$	2.5 V ± 0.2 V	Open	500 Ω	3.6 V	30 pF	0.15 V
	3.3 V ± 0.3 V	Open	500 Ω	5.5 V	50 pF	0.3 V

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (t$_{pd(s)}$)**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

NOTES: A. C$_L$ includes probe and jig capacitance.
    B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
     Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
    C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z$_O$ = 50 Ω, t$_r$ ≤ 2.5 ns, t$_f$ ≤ 2.5 ns.
    D. The outputs are measured one at a time, with one transition per measurement.
    E. t$_{PLZ}$ and t$_{PHZ}$ are the same as t$_{dis}$.
    F. t$_{PZL}$ and t$_{PZH}$ are the same as t$_{en}$.
    G. t$_{PLH}$ and t$_{PHL}$ are the same as t$_{pd(s)}$. The t$_{pd}$ propagation delay is the calculated RC time constant of the typical ON-state resistance
     of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
    H. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

Product Folder Links: *SN74CB3T16211*

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

OUTPUT VOLTAGE
vs
INPUT VOLTAGE
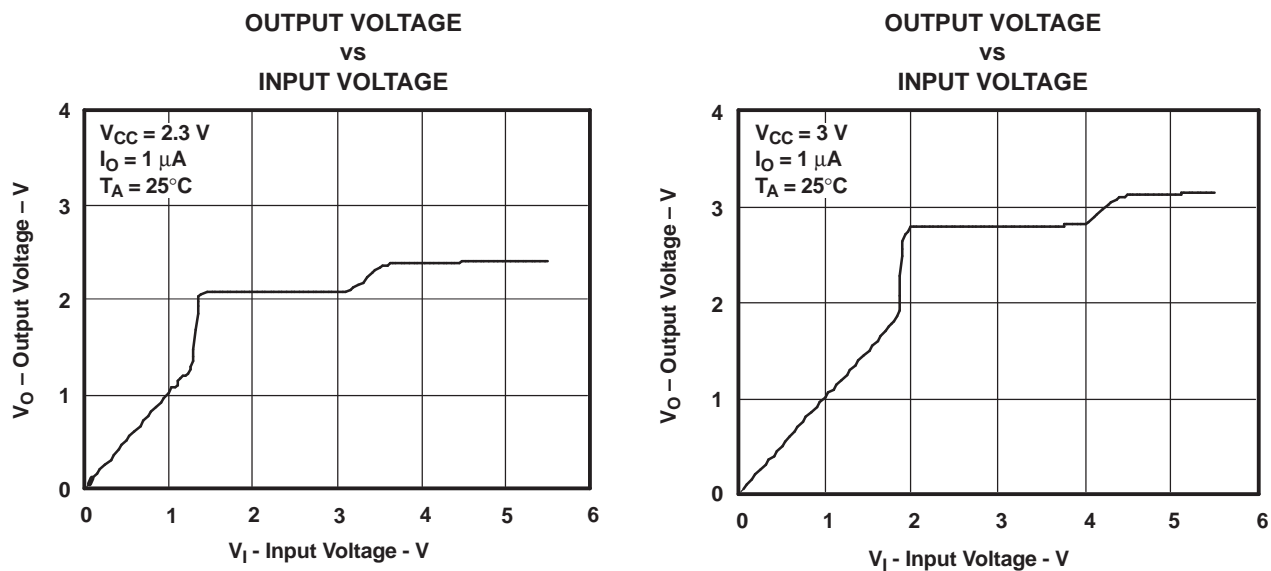
Figure 3. Data Output Voltage vs Data Input Voltage

Product Folder Links: *SN74CB3T16211*

TYPICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE
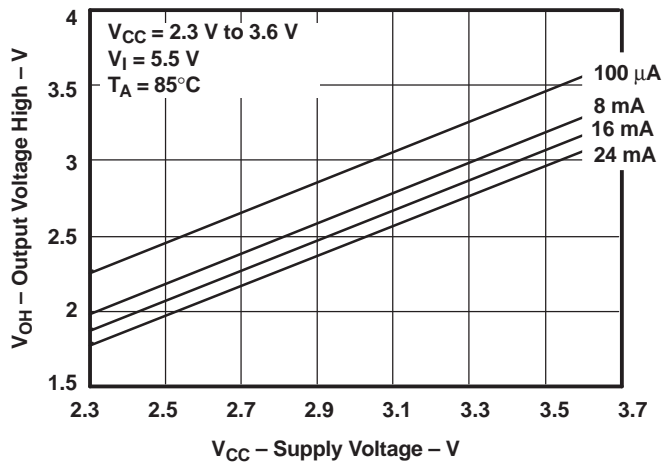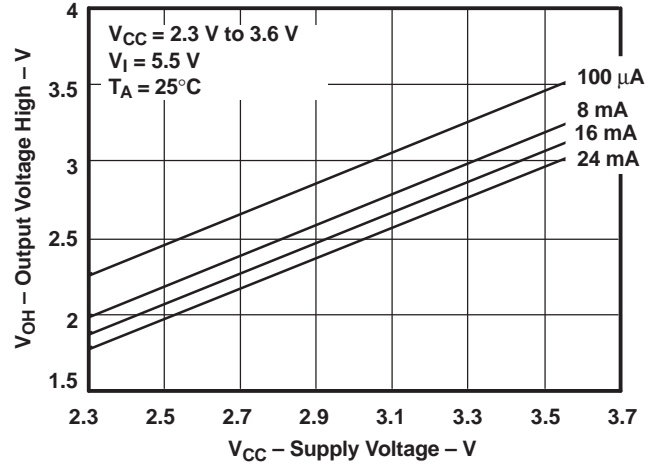
V_{CC} = 2.3 V to 3.6 V
V_I = 5.5 V
T_A = 85°C

100 μA
8 mA
16 mA
24 mA

V_{OH} – Output Voltage High – V

V_{CC} – Supply Voltage – V

OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE

V_{CC} = 2.3 V to 3.6 V
V_I = 5.5 V
T_A = 25°C

100 μA
8 mA
16 mA
24 mA

V_{OH} – Output Voltage High – V

V_{CC} – Supply Voltage – V

OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE

V_{CC} = 2.3 V to 3.6 V
V_I = 5.5 V
T_A = −40°C

100 μA
8 mA
16 mA
24 mA

V_{OH} – Output Voltage High – V

V_{CC} – Supply Voltage – V

Figure 4. V_{OH} Values

Product Folder Links: *SN74CB3T16211*

REVISION HISTORY

![Texas Instruments logo]
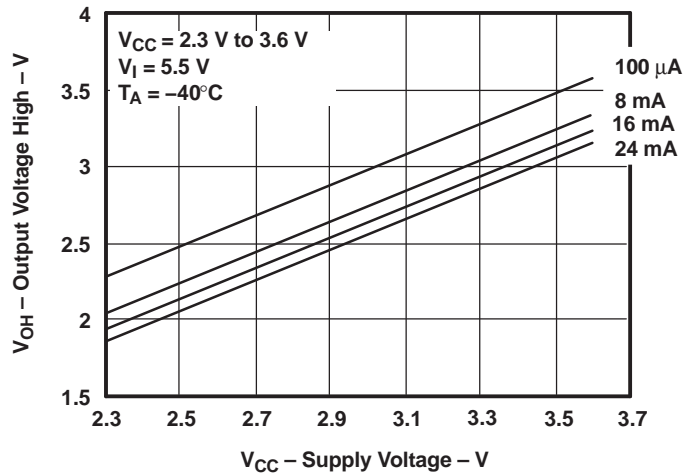
PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
74CB3T16211DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74CB3T16211DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74CB3T16211DGVRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74CB3T16211DGVRG4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74CB3T16211DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74CB3T16211DGG	PREVIEW	TSSOP	DGG	56	35	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74CB3T16211DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74CB3T16211DGVR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74CB3T16211DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74CB3T16211DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74CB3T16211DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74CB3T16211GQLR	LIFEBUY	BGA MICROSTAR JUNIOR	GQL	56	1000	TBD	SNPB	Level-1-240C-UNLIM	
SN74CB3T16211ZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS
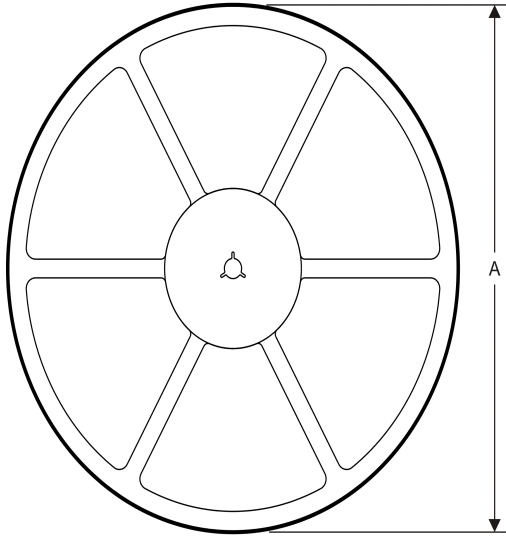
TAPE DIMENSIONS
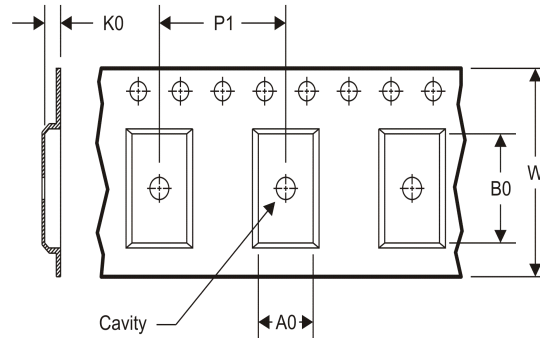
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3T16211DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74CB3T16211DGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1
SN74CB3T16211DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN74CB3T16211GQLR	BGA MICROSTAR JUNIOR	GQL	56	1000	330.0	16.4	4.8	7.3	1.45	8.0	16.0	Q1
SN74CB3T16211ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3T16211DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74CB3T16211DGVR	TVSOP	DGV	56	2000	367.0	367.0	45.0
SN74CB3T16211DLR	SSOP	DL	56	1000	367.0	367.0	55.0
SN74CB3T16211GQLR	BGA MICROSTAR JUNIOR	GQL	56	1000	333.2	345.9	28.6
SN74CB3T16211ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	333.2	345.9	28.6

ZQL (R−PBGA−N56)   PLASTIC BALL GRID ARRAY
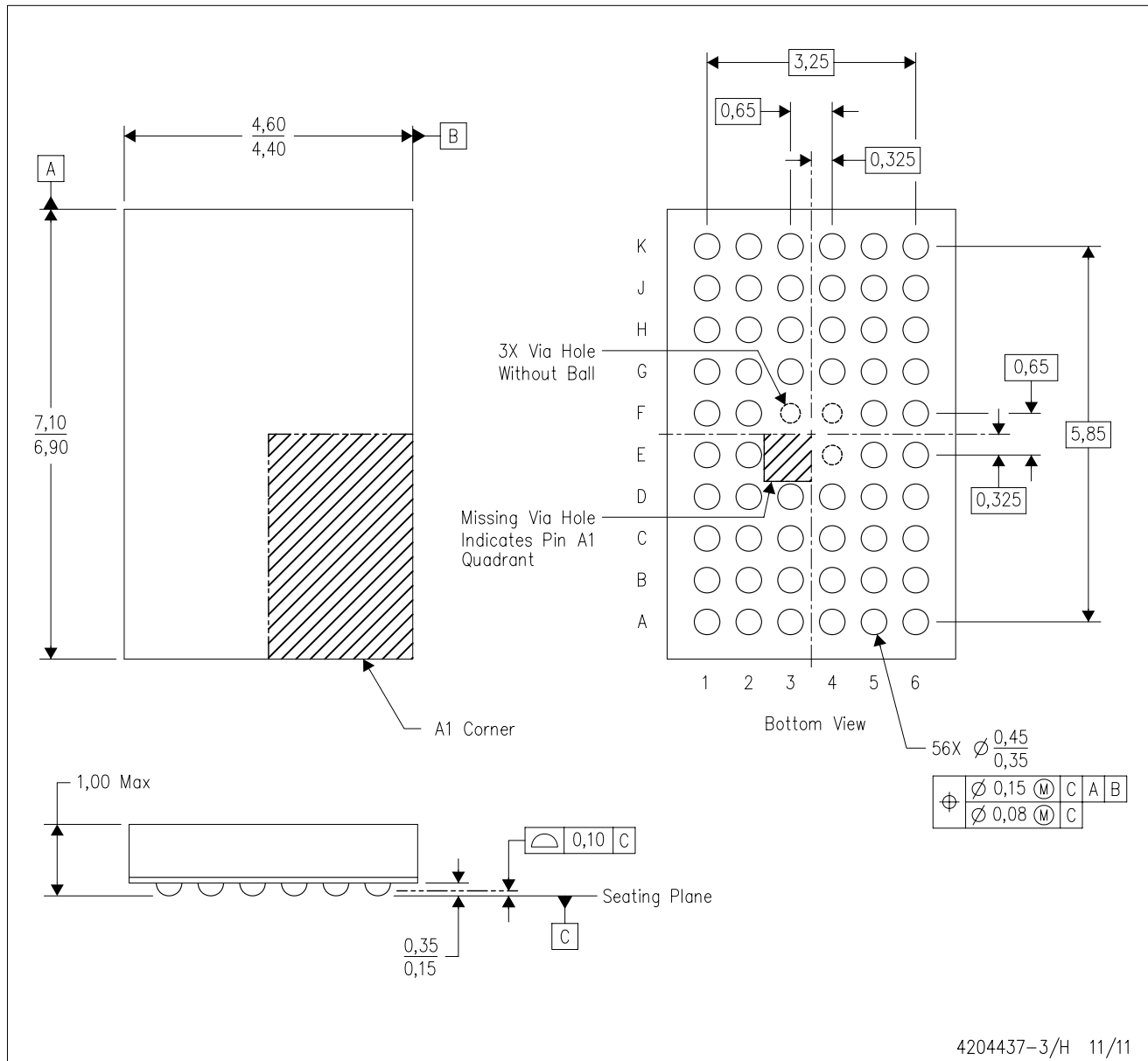
3,25

0,65

0,325

4,60
4,40

B

A

7,10
6,90

K
J
H

3X Via Hole
Without Ball

G

F

0,65

5,85

E

D

0,325

Missing Via Hole
Indicates Pin A1
Quadrant

C

B

A

1　2　3　4　5　6

Bottom View

A1 Corner

56X Ø $\frac{0,45}{0,35}$

1,00 Max

$\oplus$ | Ø 0,15 Ⓜ | C | A | B
Ø 0,08 Ⓜ | C

⌒ | 0,10 | C

Seating Plane

$\frac{0,35}{0,15}$

C

4204437−3/H 11/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MO−285 variation BA−2.
        D. This package is Pb−free. Refer to the 56 GQL package (drawing 4200583) for tin−lead (SnPb).

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DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

GQL (R−PBGA−N56)   PLASTIC BALL GRID ARRAY
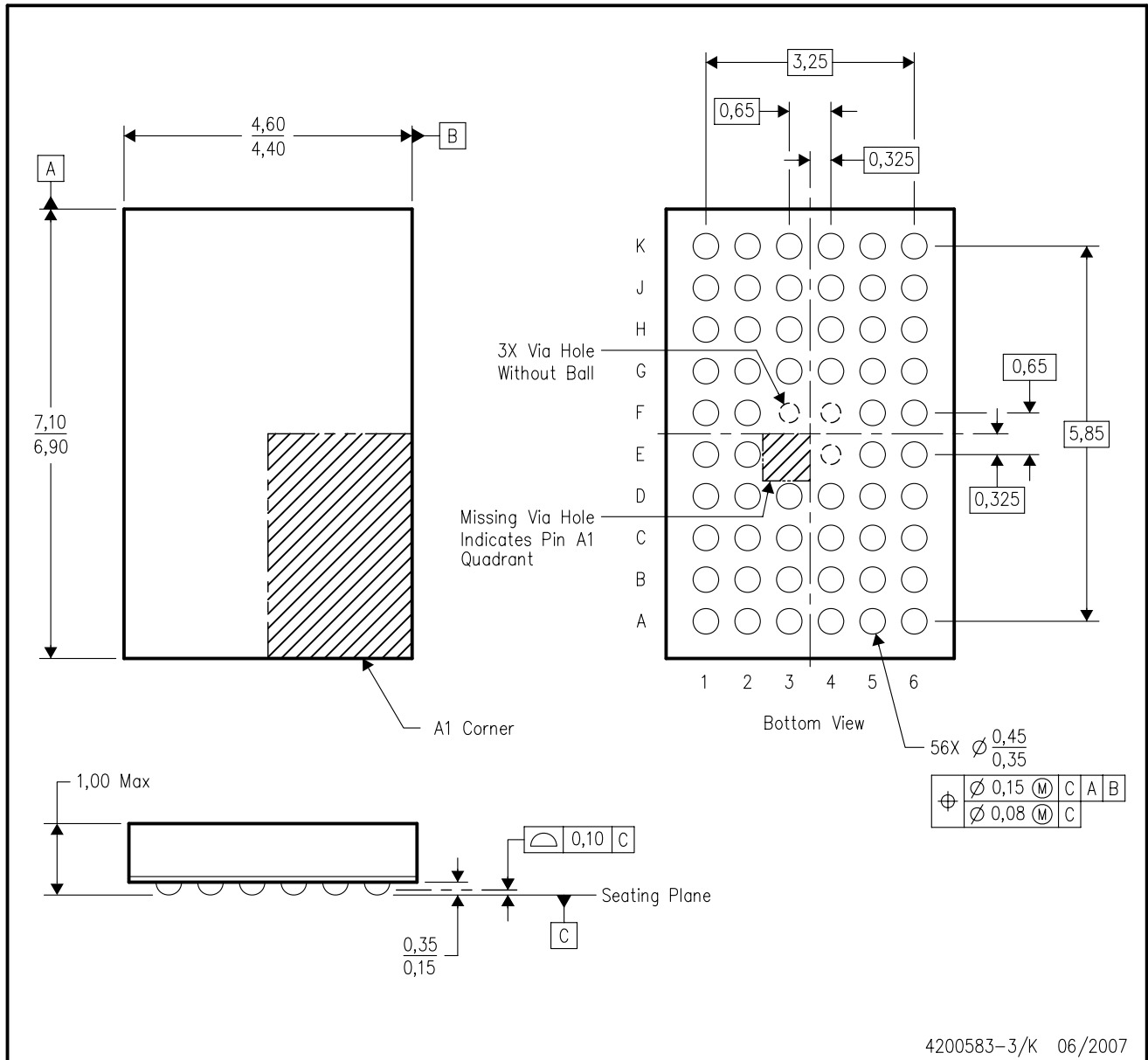
3,25

0,65

0,325

4,60
4,40
B

A

7,10
6,90

K
J
H
G
F
E
D
C
B
A

1 2 3 4 5 6

3X Via Hole
Without Ball

0,65

5,85

0,325

Missing Via Hole
Indicates Pin A1
Quadrant

A1 Corner

Bottom View

56X Ø 0,45
        0,35

1,00 Max

0,10 C

Seating Plane

0,35
0,15

C

⊕ Ø 0,15 Ⓜ C A B
  Ø 0,08 Ⓜ C

4200583−3/K 06/2007

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MO−285 variation BA−2.
        D. This package is tin−lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead−free.

TEXAS
INSTRUMENTS
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DL (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

PINS ** DIM	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048 / E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D. Falls within JEDEC MO-118

DGG (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

	PINS **	48	56	64
DIM				
A MAX		12,60	14,10	17,10
A MIN		12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold protrusion not to exceed 0,15.
   D. Falls within JEDEC MO-153

IMPORTANT NOTICE

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