

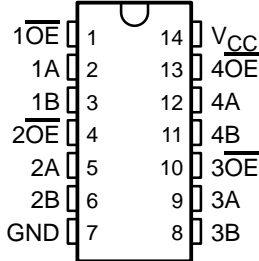
SN74CBT3125 QUADRUPLE FET BUS SWITCH

SCDS0211 – MAY 1995 – REVISED SEPTEMBER 2002

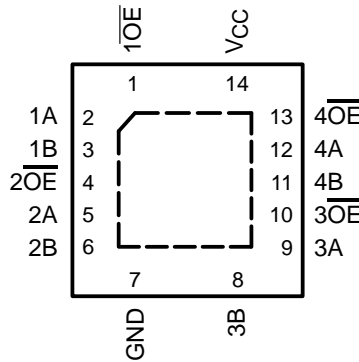
- Standard '125-Type Pinout (D, DB, DGV, and PW Packages)

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels

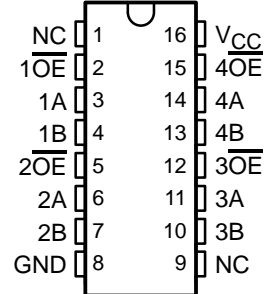
**D, DB, DGV, OR PW PACKAGE
(TOP VIEW)**



**RGY PACKAGE
(TOP VIEW)**



**DBQ PACKAGE
(TOP VIEW)**



NC – No internal connection

description/ordering information

The SN74CBT3125 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (\overline{OE}) input is high.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74CBT3125RGYR	CU125
	SOIC – D	Tube	SN74CBT3125D	CBT3125
		Tape and reel	SN74CBT3125DR	
	SSOP – DB	Tape and reel	SN74CBT3125DBR	CU125
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBT3125DBQR	CU125
	TSSOP – PW	Tape and reel	SN74CBT3125PWR	CU125
TVSOP – DGV	Tape and reel	SN74CBT3125DGV	CU125	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE
(each bus switch)**

INPUT \overline{OE}	FUNCTION
L	A port = B port
H	Disconnect



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

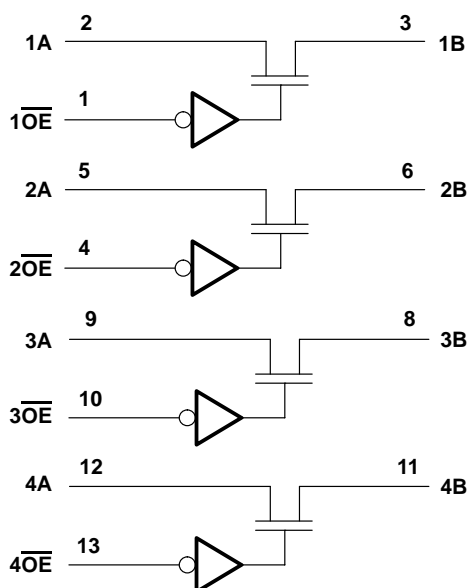
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logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, PW, and RGY packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_K ($V_{I/O} < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
(see Note 2): DB package	96°C/W
(see Note 2): DBQ package	90°C/W
(see Note 2): DGV package	127°C/W
(see Note 2): PW package	113°C/W
(see Note 3): RGY package	47°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.
 3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

	MIN	MAX	UNIT
V_{CC} Supply voltage	4	5.5	V
V_{IH} High-level control input voltage	2		V
V_{IL} Low-level control input voltage		0.8	V
T_A Operating free-air temperature	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
I_I		$V_{CC} = 5.5\text{ V}$,	$V_I = 5.5\text{ V}$ or GND			± 1	μA
I_{CC}		$V_{CC} = 5.5\text{ V}$,	$I_O = 0$, $V_I = V_{CC}$ or GND			3	μA
ΔI_{CC}^\ddagger	Control inputs	$V_{CC} = 5.5\text{ V}$,	One input at 3.4 V, Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	$V_I = 3\text{ V}$ or 0				3	pF
$C_{io(OFF)}$		$V_O = 3\text{ V}$ or 0,	$\overline{OE} = V_{CC}$			4	pF
r_{on}^\S		$V_{CC} = 4\text{ V}$, TYP at $V_{CC} = 4\text{ V}$	$V_I = 2.4\text{ V}$,	$I_I = 15\text{ mA}$	16	22	Ω
			$V_I = 0$	$I_I = 64\text{ mA}$	5	7	
		$V_{CC} = 4.5\text{ V}$	$V_I = 0$	$I_I = 30\text{ mA}$	5	7	
			$V_I = 2.4\text{ V}$,	$I_I = 15\text{ mA}$	10	15	

† All typical values are at $V_{CC} = 5\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

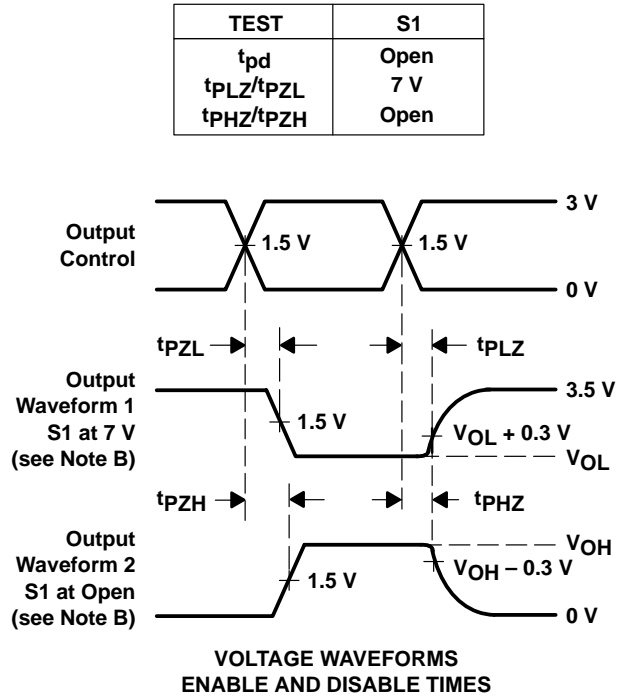
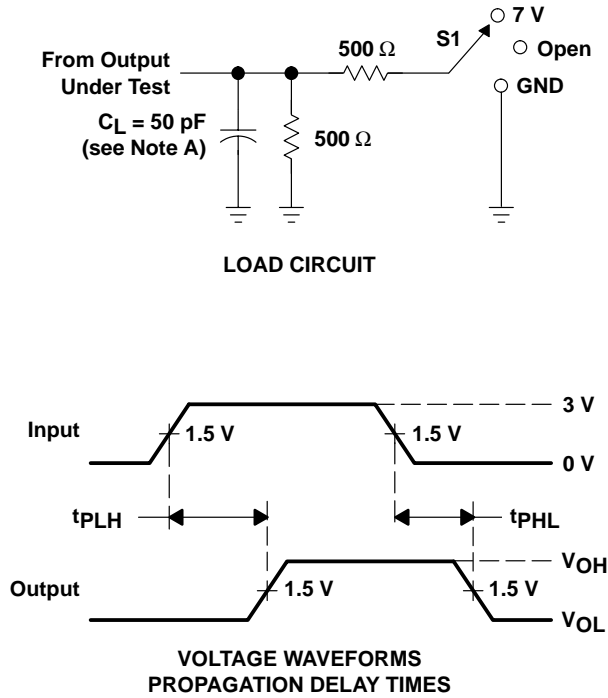
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}^{\parallel}	A or B	B or A	0.35		0.25		ns
t_{en}	\overline{OE}	A or B	6		1.6	5.4	ns
t_{dis}	\overline{OE}	A or B	5.1		1	4.7	ns

\parallel The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd}.
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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