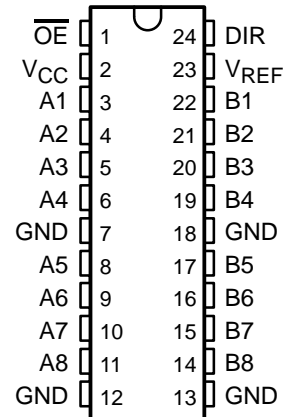


SN74GTLPH306 8-BIT LVTTTL-TO-GTLP BUS TRANSCEIVER

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- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTTL Logic Levels**
- **LVTTTL Interfaces Are 5-V Tolerant**
- **Medium-Drive GTLP Outputs (50 mA)**
- **LVTTTL Outputs (–24 mA/24 mA)**
- **GTLP Rise and Fall Times Designed for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on A-Port Data Inputs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DG, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74GTLPH306 is a medium-drive, 8-bit bus transceiver that provides LVTTTL-to-GTLP and GTLP-to-LVTTTL signal-level translation. The device provides a high-speed interface between cards operating at LVTTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard LVTTTL or TTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The medium drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 19 Ω.

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH306 is given only at the preferred higher-noise-margin GTLP, but the user has the flexibility of using this device at either GTL ($V_{TT} = 1.2$ V and $V_{REF} = 0.8$ V) or GTLP ($V_{TT} = 1.5$ V and $V_{REF} = 1$ V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.



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SN74GTLPH306

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description (continued)

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

Active bus-hold circuitry holds unused or undriven LVTTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable (\overline{OE}) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – DW	Tube	SN74GTLPH306DW	GTLPH306
		Tape and reel	SN74GTLPH306DWR	
	TSSOP – PW	Tape and reel	SN74GTLPH306PWR	GH306
	TVSOP – DGV	Tape and reel	SN74GTLPH306DGV	GH306

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLPH306 is an 8-bit bus transceiver and is designed for asynchronous communication between data buses. The device transmits data from the A port to the B port or from the B port to the A port, depending on the logic level at the direction-control (DIR) input. \overline{OE} can be used to disable the device so the buses are effectively isolated. Data polarity is noninverting.

For A-to-B data flow, when \overline{OE} is low and DIR is high, the B outputs take on the logic value of the A inputs. When \overline{OE} is high, the outputs are in the high-impedance state.

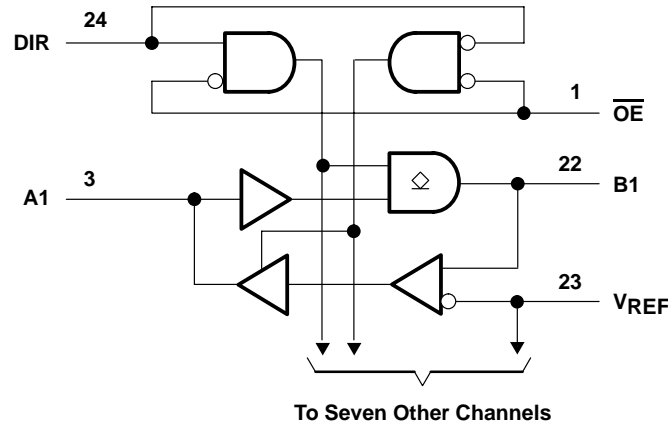
The data flow for B to A is similar to A to B, except \overline{OE} and DIR are low.

FUNCTION TABLE

INPUTS		OUTPUT	MODE
\overline{OE}	DIR		
H	X	Z	Isolation
L	L	B data to A port	True transparent
L	H	A data to B port	



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A port and control inputs	-0.5 V to 7 V
B port and V_{REF}	-0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): A port	-0.5 V to 7 V
B port	-0.5 V to 4.6 V
Current into any output in the low state, I_O : A port	48 mA
B port	100 mA
Current into any A port output in the high state, I_O (see Note 2)	48 mA
Continuous current through each V_{CC} or GND	± 100 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGV package	86°C/W
DW package	46°C/W
PW package	88°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Notes 4 through 7)

		MIN	NOM	MAX	UNIT	
V _{CC}	Supply voltage	3.15	3.3	3.45	V	
V _{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V _{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V _I	Input voltage	B port	V _{TT}		V	
		Except B port	V _{CC}	5.5		
V _{IH}	High-level input voltage	B port	V _{REF} +0.05		V	
		Except B port	2			
V _{IL}	Low-level input voltage	B port	V _{REF} -0.05		V	
		Except B port	0.8			
I _{IK}	Input clamp current			-18	mA	
I _{OH}	High-level output current	A port			-24	mA
I _{OL}	Low-level output current	A port			24	mA
		B port			50	
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	ns/V	
Δt/ΔV _{CC}	Power-up ramp rate	20			μs/V	
T _A	Operating free-air temperature	-40		85	°C	

- NOTES: 4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.



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electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 3.15\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
V_{OH}	A port	$V_{CC} = 3.15\text{ V to }3.45\text{ V}$,	$I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			V
		$V_{CC} = 3.15\text{ V}$	$I_{OH} = -12\text{ mA}$	2.4			
			$I_{OH} = -24\text{ mA}$	2			
V_{OL}	A port	$V_{CC} = 3.15\text{ V to }3.45\text{ V}$,	$I_{OL} = 100\text{ }\mu\text{A}$			0.2	V
		$V_{CC} = 3.15\text{ V}$	$I_{OL} = 12\text{ mA}$			0.4	
			$I_{OL} = 24\text{ mA}$			0.5	
	B port	$V_{CC} = 3.15\text{ V}$	$I_{OL} = 40\text{ mA}$			0.4	
			$I_{OL} = 50\text{ mA}$			0.55	
I_I^\ddagger	A-port and control inputs	$V_{CC} = 3.45\text{ V}$	$V_I = 0\text{ or }V_{CC}$			± 5	μA
			$V_I = 5.5\text{ V}$			± 20	
	B port		$V_I = 0\text{ to }1.5\text{ V}$			± 5	
I_{BHL}^\S	A port	$V_{CC} = 3.15\text{ V}$,	$V_I = 0.8\text{ V}$	75			μA
I_{BHH}^\parallel	A port	$V_{CC} = 3.15\text{ V}$,	$V_I = 2\text{ V}$	-75			μA
$I_{BHLO}^\#$	A port	$V_{CC} = 3.45\text{ V}$,	$V_I = 0\text{ to }V_{CC}$	500			μA
I_{BHHO}^\parallel	A port	$V_{CC} = 3.45\text{ V}$,	$V_I = 0\text{ to }V_{CC}$	-500			μA
I_{CC}	A or B port	$V_{CC} = 3.45\text{ V}$, $I_O = 0$, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			20	mA
			Outputs low			20	
			Outputs disabled			20	
ΔI_{CC}^\star		$V_{CC} = 3.45\text{ V}$, One A-port or control input at $V_{CC} - 0.6\text{ V}$, Other A-port or control inputs at V_{CC} or GND				1.5	mA
C_i	Control inputs	$V_I = 3.15\text{ V or }0$			4.5	5	pF
C_{io}	A port	$V_O = 3.15\text{ V or }0$			7.5	9	pF
	B port	$V_O = 1.5\text{ V or }0$			7.5	9	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameter I_I includes the off-state output leakage current.

§ The bus-hold circuit can sink at least the minimum low sustaining current at V_{ILmax} . I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{ILmax} .

¶ The bus-hold circuit can source at least the minimum high sustaining current at V_{IHmin} . I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IHmin} .

An external driver must source at least I_{BHLO} to switch this node from low to high.

|| An external driver must sink at least I_{BHHO} to switch this node from high to low.

* This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	$V_{CC} = 0$,	V_I or $V_O = 0\text{ to }5.5\text{ V}$			10	μA
I_{OZPU}	$V_{CC} = 0\text{ to }1.5\text{ V}$,	$V_O = 0.5\text{ V to }3\text{ V}$,	$\overline{OE} = 0$		± 30	μA
I_{OZPD}	$V_{CC} = 1.5\text{ V to }0$,	$V_O = 0.5\text{ V to }3\text{ V}$,	$\overline{OE} = 0$		± 30	μA



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hot-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
I_{off}	$V_{CC} = 0,$	V_I or $V_O = 0$ to 1.5 V		10	μA
I_{OZPU}	$V_{CC} = 0$ to 1.5 V,	$V_O = 0.5$ V to 1.5 V, $\overline{OE} = 0$		± 30	μA
I_{OZPD}	$V_{CC} = 1.5$ V to 0,	$V_O = 0.5$ V to 1.5 V, $\overline{OE} = 0$		± 30	μA

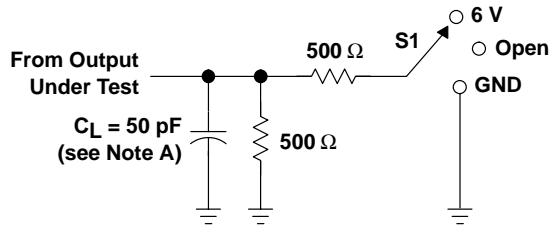
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $V_{TT} = 1.5$ V and $V_{REF} = 1$ V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	A	B	1		7.5	ns
t_{PHL}			1		7.5	
t_{en}	\overline{OE}	B	1		8	ns
t_{dis}			1		8	
t_r	Rise time, B outputs (20% to 80%)		2.2			ns
t_f	Fall time, B outputs (80% to 20%)		2.1			ns
t_r	Rise time, A outputs (10% to 90%)		4.1			ns
t_f	Fall time, A outputs (90% to 10%)		3.3			ns
t_{PLH}	B	A	1		7	ns
t_{PHL}			1		7	
t_{en}	\overline{OE}	A	1		8	ns
t_{dis}			1		8	

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ C$.

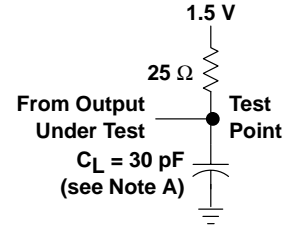


PARAMETER MEASUREMENT INFORMATION

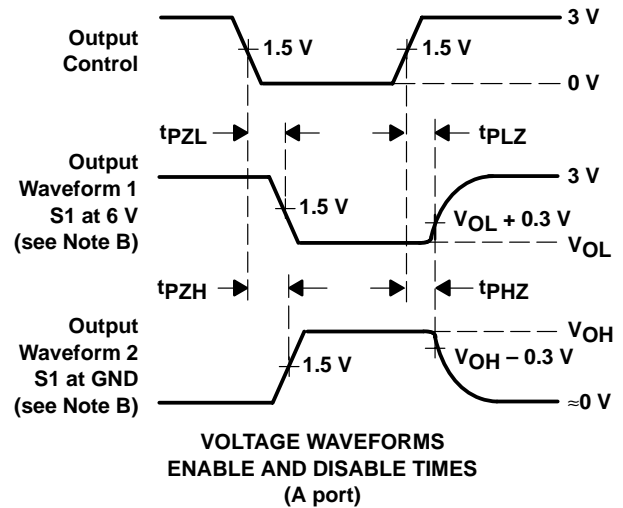
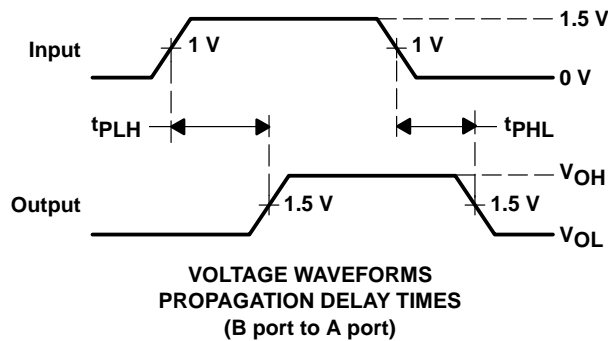
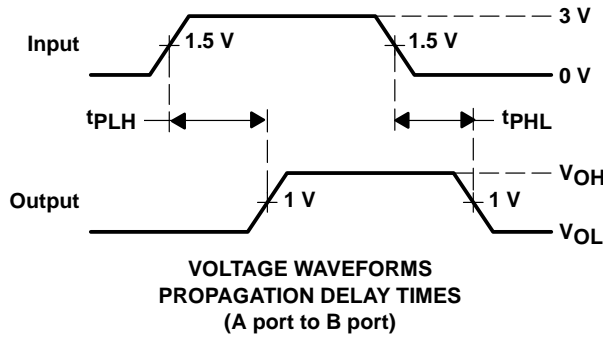


LOAD CIRCUIT FOR A OUTPUTS

TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	6 V
tPHZ/tPZH	GND



LOAD CIRCUIT FOR B OUTPUTS



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \approx 10 MHz, $Z_O = 50 \Omega$, $t_r \approx 2$ ns, $t_f \approx 2$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

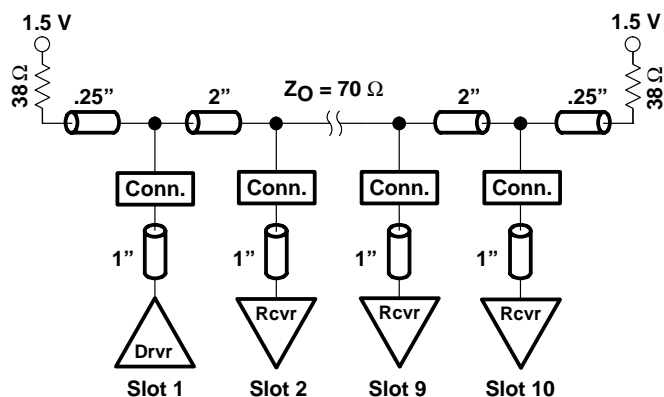


Figure 2. Medium-Drive Test Backplane

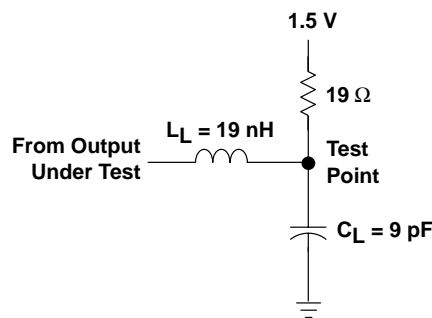


Figure 3. Medium-Drive RLC Network

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $V_{TT} = 1.5\text{ V}$ and $V_{REF} = 1\text{ V}$ for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TYP†	UNIT
t_{PLH}	A	B	3.6	ns
t_{PHL}			4.1	
t_{en}	\overline{OE}	B	4.4	ns
t_{dis}			4.6	
t_r	Rise time, B outputs (20% to 80%)		1.2	ns
t_f	Fall time, B outputs (80% to 20%)		2.2	ns

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$. All values are derived from TI-SPICE models.

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