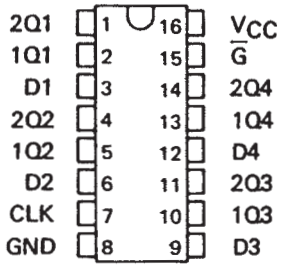
- Parallel Access
- Typical Propagation Delay Time . . . 20 ns
- Typical Power Dissipation . . . 120 mW
- Applications:
  - N-Bit Storage Files
  - Hex/BCD Serial-To-Parallel Converters

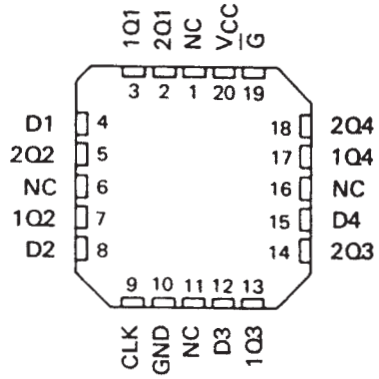
description

These octal registers are organized as two 4-bit bytes of storage. Upon application of a positive-going clock signal, the information stored in byte 1 is transferred into byte 2 as a new 4-bit byte is loaded into the byte 1 location via the four data lines. The full 8-bit word is available at the outputs after two clock cycles. Both the clock and the strobe lines are fully buffered.

SN54LS396 . . . J OR W PACKAGE
SN74LS396 . . . D OR N PACKAGE
(TOP VIEW)

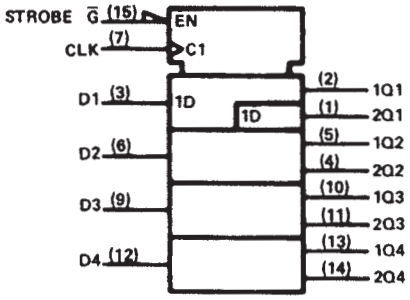


SN54LS396 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

logic symbol†



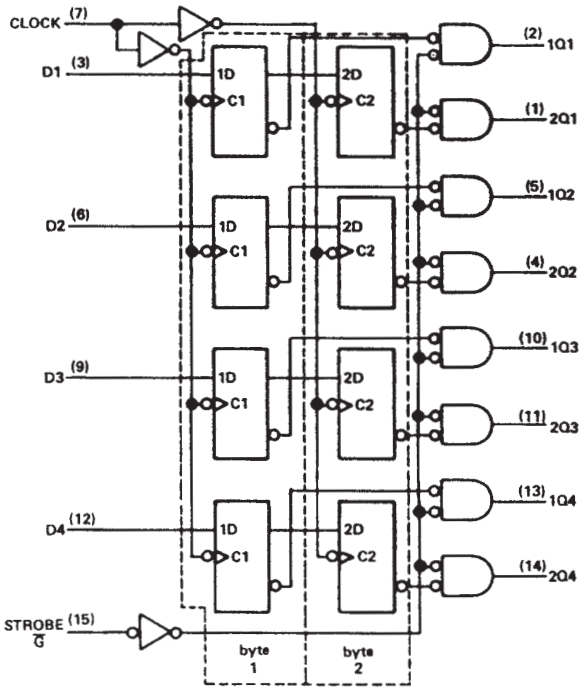
†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

FUNCTION TABLE

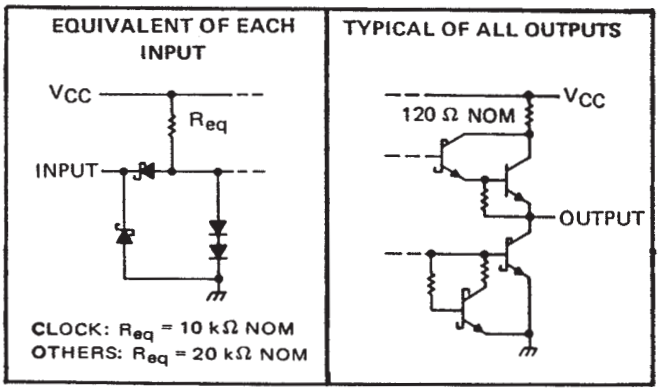
INPUTS						OUTPUTS							
STROBE $\overline{G}$	CLOCK	DATA				BYTE 1				BYTE 2			
		D1	D2	D3	D4	1Q1	1Q2	1Q3	1Q4	2Q1	2Q2	2Q3	2Q4
H	X	X	X	X	X	L	L	L	L	L	L	L	L
L	↑	a	b	c	d	a	b	c	d	$1Q1_n$	$1Q2_n$	$1Q3_n$	$1Q4_n$

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↑ = transition from low to high level
$1Q1_n$, $1Q2_n$, $1Q3_n$, $1Q4_n$ = the level of 1Q1, 1Q2, 1Q3, and 1Q4, respectively, before the most recent ↑ transition of the clock.

logic diagram (positive logic)



schematics of inputs and outputs



Pin numbers shown are for D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS396 . . . . . −55°C to 125°C
SN74LS396 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS396			SN74LS396			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock pulse, t_w	20			20			ns
Setup time, t_{su}	20			20			ns
Hold time, t_h	5			5			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS396			SN74LS396			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Clock input	V_{CC} = MAX,	V_I = 7 V			0.2			0.2	mA
		Other inputs					0.1			0.1	
I_{IH}	High-level input current	Clock input	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
		Other inputs					20			20	
I_{IL}	Low-level input current	Clock input	V_{CC} = MAX,	V_I = 0.4 V			−0.8			−0.8	mA
		Other inputs					−0.4			−0.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		24	40		24	40	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	C_L = 15 pF, R_L = 2 kΩ, See Note 3		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			20	30	
t_{PLH}	Propagation delay time, low-to-high-level output from strobe			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from strobe			20	30	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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