

SN54LV175A, SN74LV175A QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SCLS400E – APRIL 1998 – REVISED JULY 2003

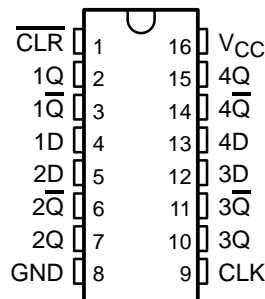
- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 7.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- Contain Four Flip-Flops With Double-Rail Outputs
- Applications Include:
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

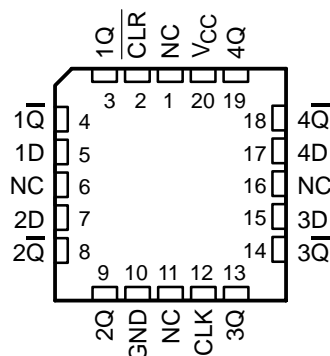
The 'LV175A devices are quadruple D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation.

These devices have a direct clear ($\overline{\text{CLR}}$) input and feature complementary outputs from each flip-flop.

SN54LV175A ... J OR W PACKAGE
SN74LV175A ... D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV175A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – D	Tube of 40	SN74LV175AD	LV175A
		Reel of 2500	SN74LV175ADR	
	SOP – NS	Reel of 2000	SN74LV175ANSR	74LV175A
	SSOP – DB	Reel of 2000	SN74LV175ADBR	LV175A
	TSSOP – PW	Tube of 90	SN74LV175APW	LV175A
		Reel of 2000	SN74LV175APWR	
		Reel of 250	SN74LV175APWT	
TVSOP – DGV	Reel of 2000	SN74LV175ADGVR	LV175A	
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV175AJ	SNJ54LV175AJ
	CFP – W	Tube of 150	SNJ54LV175AW	SNJ54LV175AW
	LCCC – FK	Tube of 55	SNJ54LV175AFK	SNJ54LV175AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

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description/ordering information (continued)

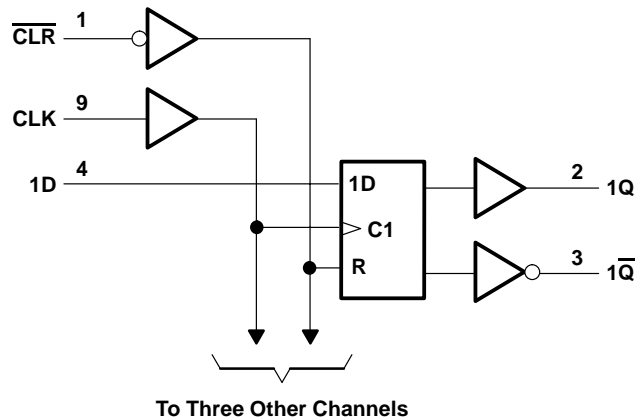
Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse.

Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUTS	
$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	\overline{Q}_0

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
DB package	82°C/W
DGV package	20°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Note 4)

		SN54LV175A		SN74LV175A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	1.5		V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$	0.5	0.5		V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$		
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2\text{ V}$		-50	-50	μA
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		-2	-2	mA
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		-6	-6	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		-12	-12	
I_{OL}	Low-level output current	$V_{CC} = 2\text{ V}$		50	50	μA
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		2	2	mA
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		6	6	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		12	12	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		200	200	ns/V
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		100	100	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		20	20	
T_A	Operating free-air temperature	-55	125	-40	85	$^{\circ}\text{C}$

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV175A			SN74LV175A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	$I_{OH} = -50\ \mu\text{A}$	2 V to 5.5 V	$V_{CC}-0.1$			$V_{CC}-0.1$			V
	$I_{OH} = -2\ \text{mA}$	2.3 V	2			2			
	$I_{OH} = -6\ \text{mA}$	3 V	2.48			2.48			
	$I_{OH} = -12\ \text{mA}$	4.5 V	3.8			3.8			
V_{OL}	$I_{OL} = 50\ \mu\text{A}$	2 V to 5.5 V	0.1			0.1			V
	$I_{OL} = 2\ \text{mA}$	2.3 V	0.4			0.4			
	$I_{OL} = 6\ \text{mA}$	3 V	0.44			0.44			
	$I_{OL} = 12\ \text{mA}$	4.5 V	0.55			0.55			
I_I	$V_I = 5.5\ \text{V or GND}$	0 to 5.5 V	± 1			± 1			μA
I_{CC}	$V_I = V_{CC}\ \text{or GND, } I_O = 0$	5.5 V	20			20			μA
I_{off}	$V_I\ \text{or } V_O = 0\ \text{to } 5.5\ \text{V}$	0	5			5			μA
C_i	$V_I = V_{CC}\ \text{or GND}$	3.3 V	1.4			1.4			pF

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV175A		SN74LV175A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{\text{CLR}}$ low	6	6	6	6	ns	
		CLK high or low	6.5	7	7	7		
t_{su}	Setup time before $\text{CLK}\uparrow$	Data	7	7.5	7.5	7.5	ns	
		$\overline{\text{CLR}}$ inactive	7	7.5	7.5	7.5		
t_h	Hold time, data after $\text{CLK}\uparrow$	0.5	1	1	1	ns		

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV175A		SN74LV175A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{\text{CLR}}$ low	5	5	5	5	ns	
		CLK high or low	5	5	5	5		
t_{su}	Setup time before $\text{CLK}\uparrow$	Data	5	5	5	5	ns	
		$\overline{\text{CLR}}$ inactive	5	5	5	5		
t_h	Hold time, data after $\text{CLK}\uparrow$	1	1	1	1	ns		

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV175A		SN74LV175A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{\text{CLR}}$ low	5	5	5	5	ns	
		CLK high or low	5	5	5	5		
t_{su}	Setup time before $\text{CLK}\uparrow$	Data	4	4	4	4	ns	
		$\overline{\text{CLR}}$ inactive	5	5	5	5		
t_h	Hold time, data after $\text{CLK}\uparrow$	1	1	1	1	ns		

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV175A		SN74LV175A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	50*	105*	45*	45	45	MHz		
			$C_L = 50\text{ pF}$	40	80	35	35	35			
t_{pd}	$\overline{\text{CLR}}$	Any	$C_L = 15\text{ pF}$	7.9*	16.6*	1*	20*	1	20	ns	
	CLK	Any		9.3*	18.8*	1*	22*	1	22		
t_{pd}	$\overline{\text{CLR}}$	Any	$C_L = 50\text{ pF}$	10.4	21.6	1	25.5	1	25.5	ns	
	CLK	Any		12	23.3	1	27	1	27		
$t_{sk(o)}$			$C_L = 50\text{ pF}$	2					2	ns	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV175A		SN74LV175A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	90*	155*		75*		75		MHz
			$C_L = 50\text{ pF}$	50	120		45		45		
t_{pd}	$\overline{\text{CLR}}$	Any	$C_L = 15\text{ pF}$	5.5*	10.1*		1*	12*	1	12	ns
	CLK	Any		6.5*	11.5*		1*	13.5*	1	13.5	
t_{pd}	$\overline{\text{CLR}}$	Any	$C_L = 50\text{ pF}$	7.4	13.6		1	15.5	1	15.5	ns
	CLK	Any		8.4	15		1	17	1	17	
$t_{\text{sk(o)}}$			$C_L = 50\text{ pF}$			1.5				1.5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV175A		SN74LV175A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	150*	215*		125*		125		MHz
			$C_L = 50\text{ pF}$	85	165		75		75		
t_{pd}	$\overline{\text{CLR}}$	Any	$C_L = 15\text{ pF}$	3.7*	6.4*		1*	7.5*	1	7.5	ns
	CLK	Any		4.6*	7.3*		1*	8.5*	1	8.5	
t_{pd}	$\overline{\text{CLR}}$	Any	$C_L = 50\text{ pF}$	5.3	8.4		1	9.5	1	9.5	ns
	CLK	Any		6	9.3		1	10.5	1	10.5	
$t_{\text{sk(o)}}$			$C_L = 50\text{ pF}$			1				1	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV175A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.3	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

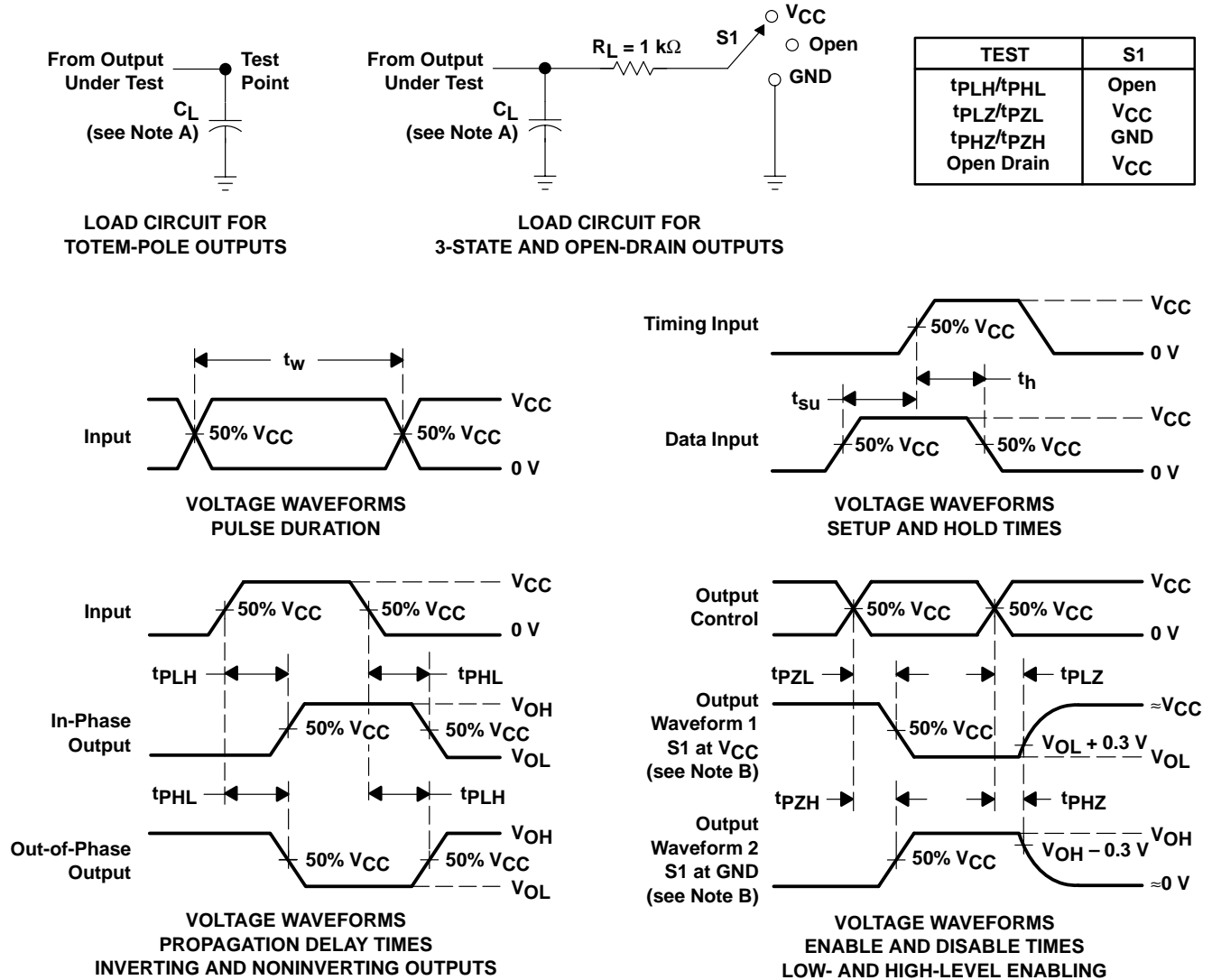
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	13.6	pF
			5 V	14.5	

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

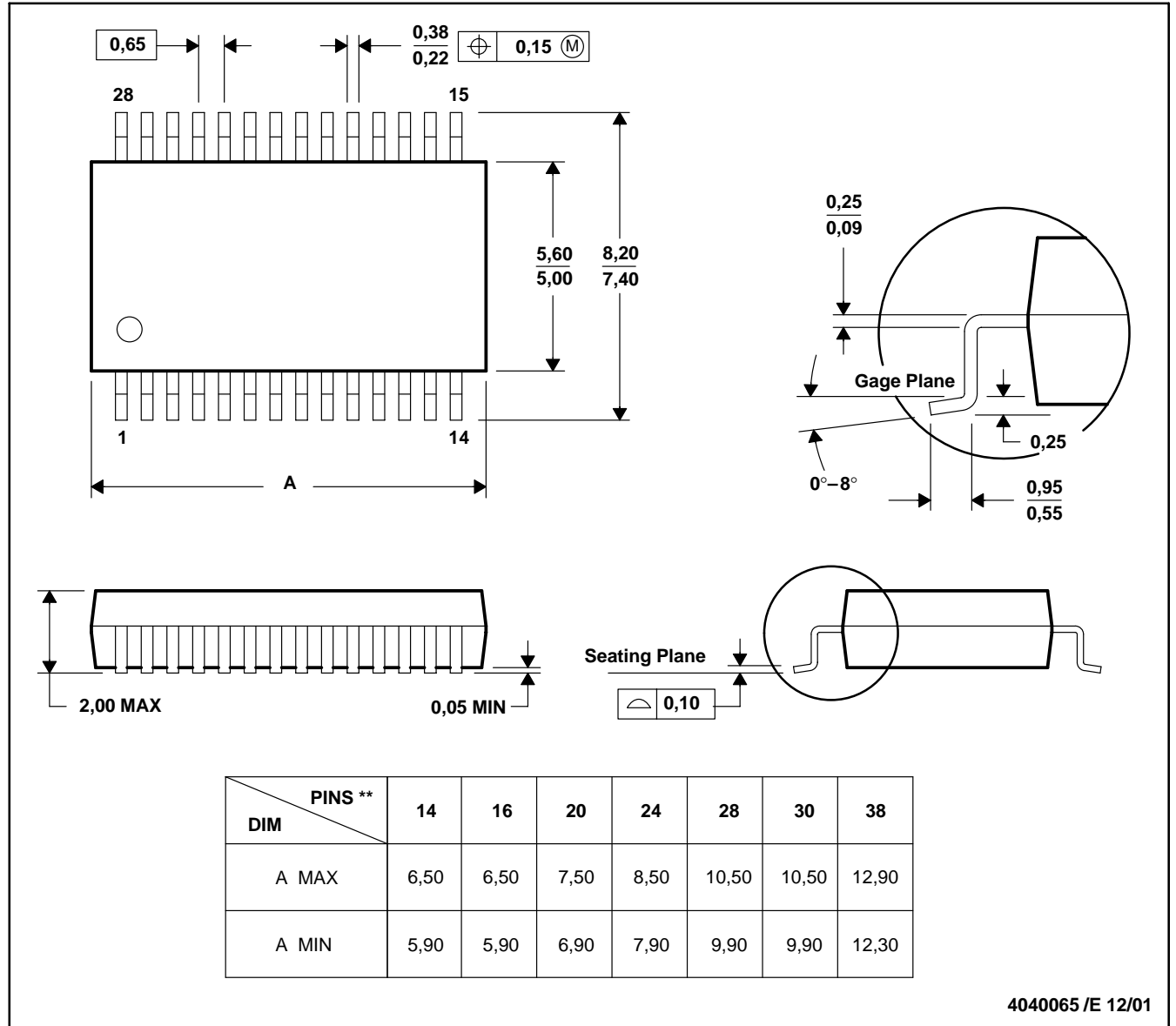


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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