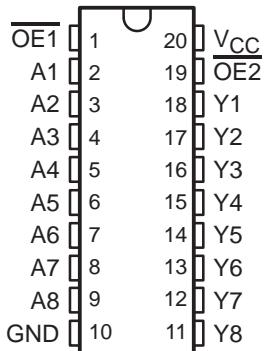


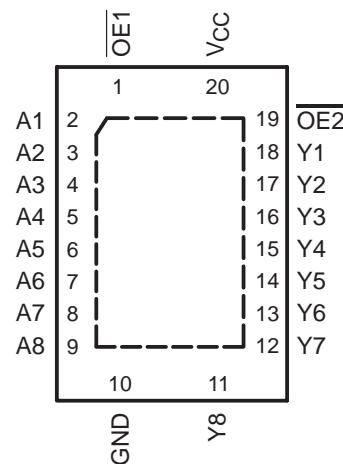
- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 6 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot)
 >2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54LV541A . . . J OR W PACKAGE
SN74LV541A . . . DB, DGV, DW, NS,
OR PW PACKAGE

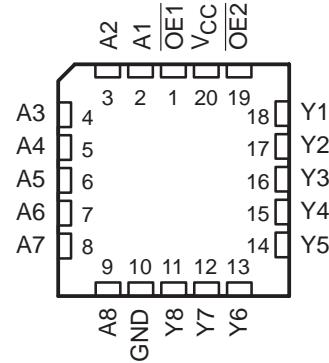
(TOP VIEW)



SN74LV541A . . . RGY PACKAGE
(TOP VIEW)



SN54LV541A . . . FK PACKAGE
(TOP VIEW)



description/ordering information

The 'LV541A devices are octal buffers/drivers designed for 2-V to 5.5-V V_{CC} operation.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LV541ARGYR	LV541A
	SOIC – DW	Tube of 25	SN74LV541ADW	LV541A
		Reel of 2000	SN74LV541ADWR	
	SOP – NS	Reel of 2000	SN74LV541ANSR	74LV541A
	SSOP – DB	Reel of 2000	SN74LV541ADBR	LV541A
	TSSOP – PW	Tube of 70	SN74LV541APW	LV541A
		Reel of 2000	SN74LV541APWR	
		Reel of 250	SN74LV541APWT	
–55°C to 125°C	TVSOP – DGV	Reel of 2000	SN74LV541ADGVR	LV541A
	CDIP – J	Tube of 20	SNJ54LV541AJ	SNJ54LV541AJ
	CFP – W	Tube of 85	SNJ54LV541AW	SNJ54LV541AW
	LCCC – FK	Tube of 55	SNJ54LV541AFK	SNJ54LV541AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN54LV541A, SN74LV541A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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description/ordering information (continued)

These devices are ideal for driving bus lines or buffer memory address registers. They feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide noninverted data when they are not in the high-impedance state.

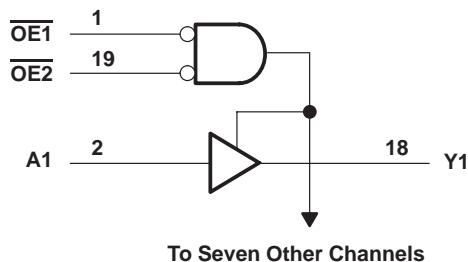
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE
(each buffer/driver)

INPUTS			OUTPUT
$OE1$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

1. The input and output voltage ratings may be exceeded if the input and output current is exceeded.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

SN54LV541A, SN74LV541A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS410G – APRIL 1998 – REVISED AUGUST 2003

recommended operating conditions (see Note 5)

		SN54LV541A		SN74LV541A		UNIT	
		MIN	MAX	MIN	MAX		
V _{CC}	Supply voltage	2	5.5	2	5.5	V	
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5		V	
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	V _{CC} × 0.7			
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	V _{CC} × 0.7			
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	V _{CC} × 0.7			
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5		V	
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	V _{CC} × 0.3			
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	V _{CC} × 0.3			
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	V _{CC} × 0.3			
V _I	Input voltage	0	5.5	0	5.5	V	
V _O	Output voltage	High or low state	0	V _{CC}	0	V _{CC}	V
		3-state	0	5.5	0	5.5	
I _{OH}	High-level output current	V _{CC} = 2 V	–50	–50	–50	μA	
		V _{CC} = 2.3 V to 2.7 V	–2	–2	–2		
		V _{CC} = 3 V to 3.6 V	–8	–8	–8		
		V _{CC} = 4.5 V to 5.5 V	–16	–16	–16		
I _{OL}	Low-level output current	V _{CC} = 2 V	50	50	50	μA	
		V _{CC} = 2.3 V to 2.7 V	2	2	2		
		V _{CC} = 3 V to 3.6 V	8	8	8		
		V _{CC} = 4.5 V to 5.5 V	16	16	16		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	200	200	200		
		V _{CC} = 3 V to 3.6 V	100	100	100		
		V _{CC} = 4.5 V to 5.5 V	20	20	20		
T _A	Operating free-air temperature	–55	125	–40	85	°C	

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV541A			SN74LV541A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} – 0.1			V _{CC} – 0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –8 mA	3 V	2.48			2.48			
	I _{OH} = –16 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V		0.1			0.1		V
	I _{OL} = 2 mA	2.3 V		0.4			0.4		
	I _{OL} = 8 mA	3 V		0.44			0.44		
	I _{OL} = 16 mA	4.5 V		0.55			0.55		
I _I	V _I = 5.5 V or GND	0 to 5.5 V		±1			±1		μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V		±5			±5		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		20			20		μA
I _{off}	V _I or V _O = 0 to 5.5 V	0		5			5		μA
C _i	V _I = V _{CC} or GND	3.3 V		2			2		pF

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**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV541A		SN74LV541A		UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t_{pd}	A	Y	$C_L = 15 \text{ pF}$	6.7*	11.3*	1*	13.5*	1	13.5	ns	ns	
t_{en}	\overline{OE}	Y		8.5*	16.6*	1*	19.5*	1	19.5	ns		
t_{dis}	\overline{OE}	Y		8.4*	13.1*	1*	15*	1	15			
t_{pd}	A	Y	$C_L = 50 \text{ pF}$	8.7	15.9	1	18.5	1	18.5	ns	ns	
t_{en}	\overline{OE}	Y		10.5	20.7	1	24	1	24			
t_{dis}	\overline{OE}	Y		12.3	17.9	1	20	1	20			
$t_{sk(o)}$					2				2			

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV541A		SN74LV541A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	$C_L = 15 \text{ pF}$	4.8*	7*	1*	8.5*	1	8.5	ns	ns
t_{en}	\overline{OE}	Y		6.1*	10.5*	1*	12.5*	1	12.5		
t_{dis}	\overline{OE}	Y		5.8*	11*	1*	12*	1	12		
t_{pd}	A	Y	$C_L = 50 \text{ pF}$	6.1	10.5	1	12	1	12	ns	ns
t_{en}	\overline{OE}	Y		7.4	14	1	16	1	16		
t_{dis}	\overline{OE}	Y		8.8	15.4	1	17.5	1	17.5		
$t_{sk(o)}$					1.5				1.5		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV541A		SN74LV541A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	$C_L = 15 \text{ pF}$	3.5*	5*	1*	6*	1	6	ns	ns
t_{en}	\overline{OE}	Y		4.3*	7.2*	1*	8.5*	1	8.5		
t_{dis}	\overline{OE}	Y		3.9*	7.5*	1*	8*	1	8		
t_{pd}	A	Y	$C_L = 50 \text{ pF}$	4.3	7	1	8	1	8	ns	ns
t_{en}	\overline{OE}	Y		5.3	9.2	1	10.5	1	10.5		
t_{dis}	\overline{OE}	Y		5.6	8.8	1	10	1	10		
$t_{sk(o)}$					1				1		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**SN54LV541A, SN74LV541A
OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS**

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noise characteristics, $V_{CC} = 3.3$ V, $C_L = 50$ pF, $T_A = 25^\circ\text{C}$ (see Note 6)

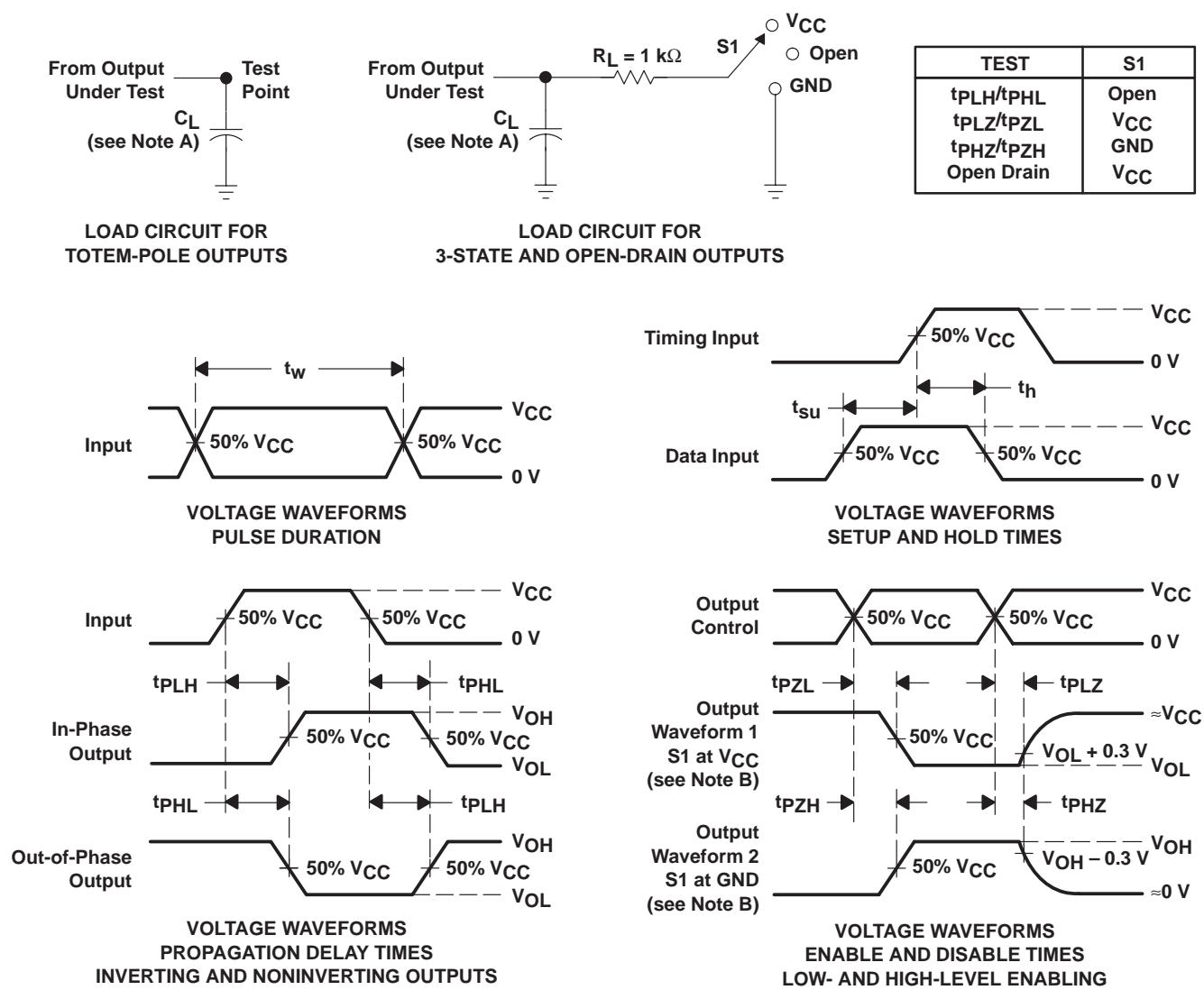
PARAMETER	SN74LV541A			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}	0.5	0.8		V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}	-0.4	-0.8		V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}	2.9			V
$V_{IH(D)}$ High-level dynamic input voltage	2.31			V
$V_{IL(D)}$ Low-level dynamic input voltage	0.99			V

NOTE 6: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		V_{CC}	TYP	UNIT
	Outputs enabled	$C_L = 50$ pF, $f = 10$ MHz			
C_{pd} Power dissipation capacitance			3.3 V	16.3	
			5 V	17.8	pF

PARAMETER MEASUREMENT INFORMATION



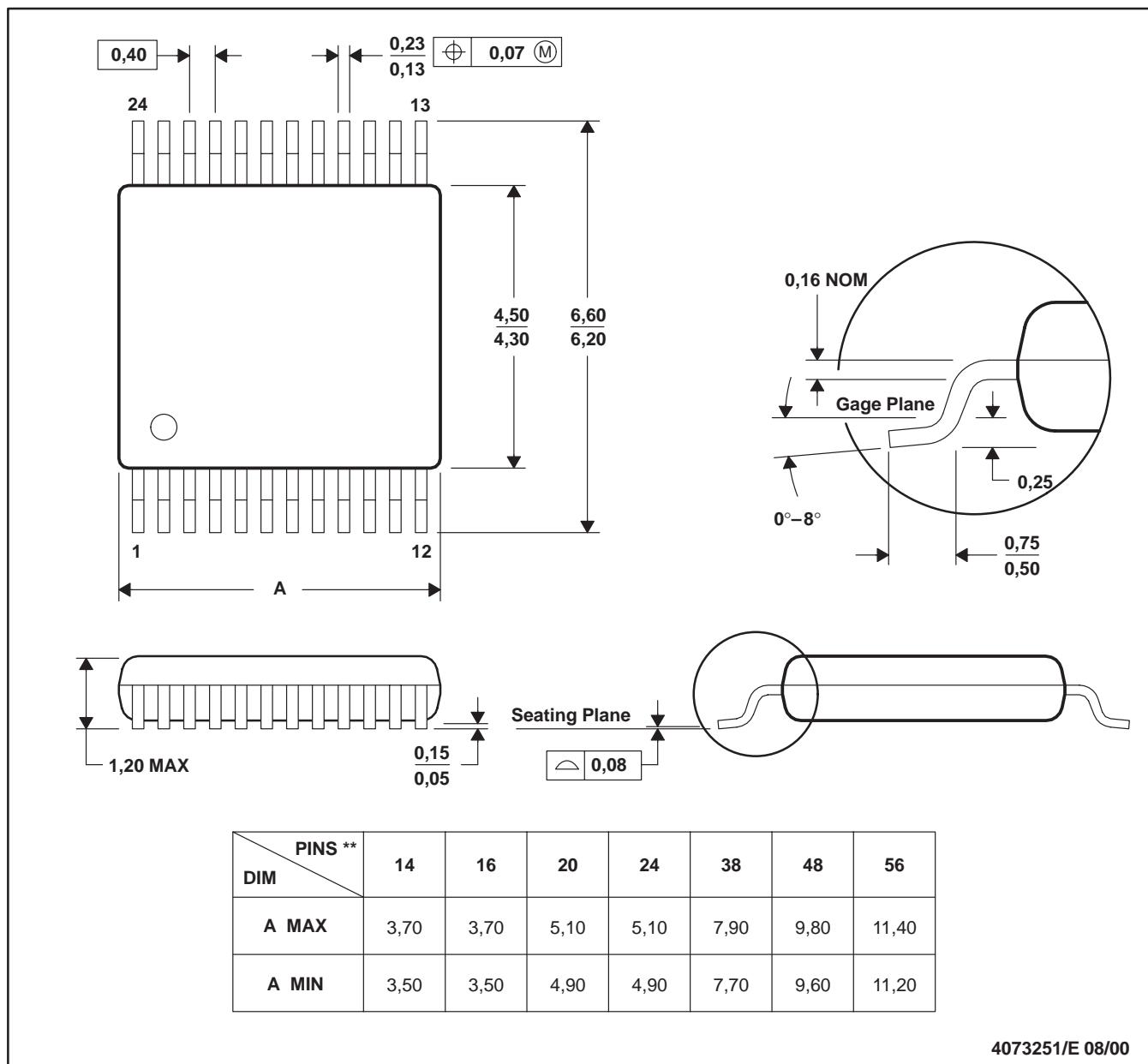
- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PZL} and t_{PHZ} are the same as t_{dis}.
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PHL} and t_{PLH} are the same as t_{pd}.
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

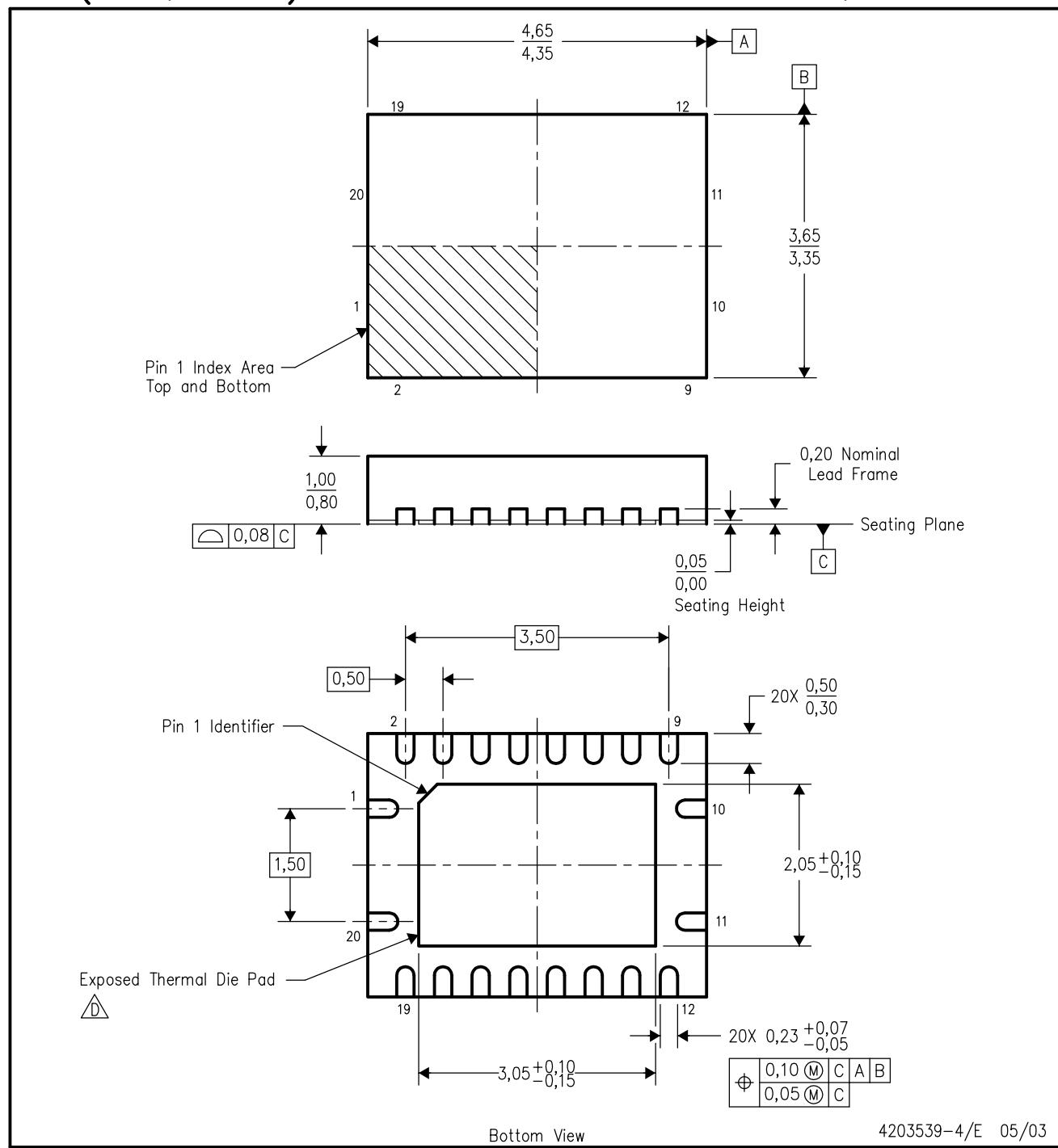


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 - D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

MECHANICAL DATA

RGY (R-PQFP-N20)

PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. QFN (Quad Flatpack No-Lead) package configuration.

D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.

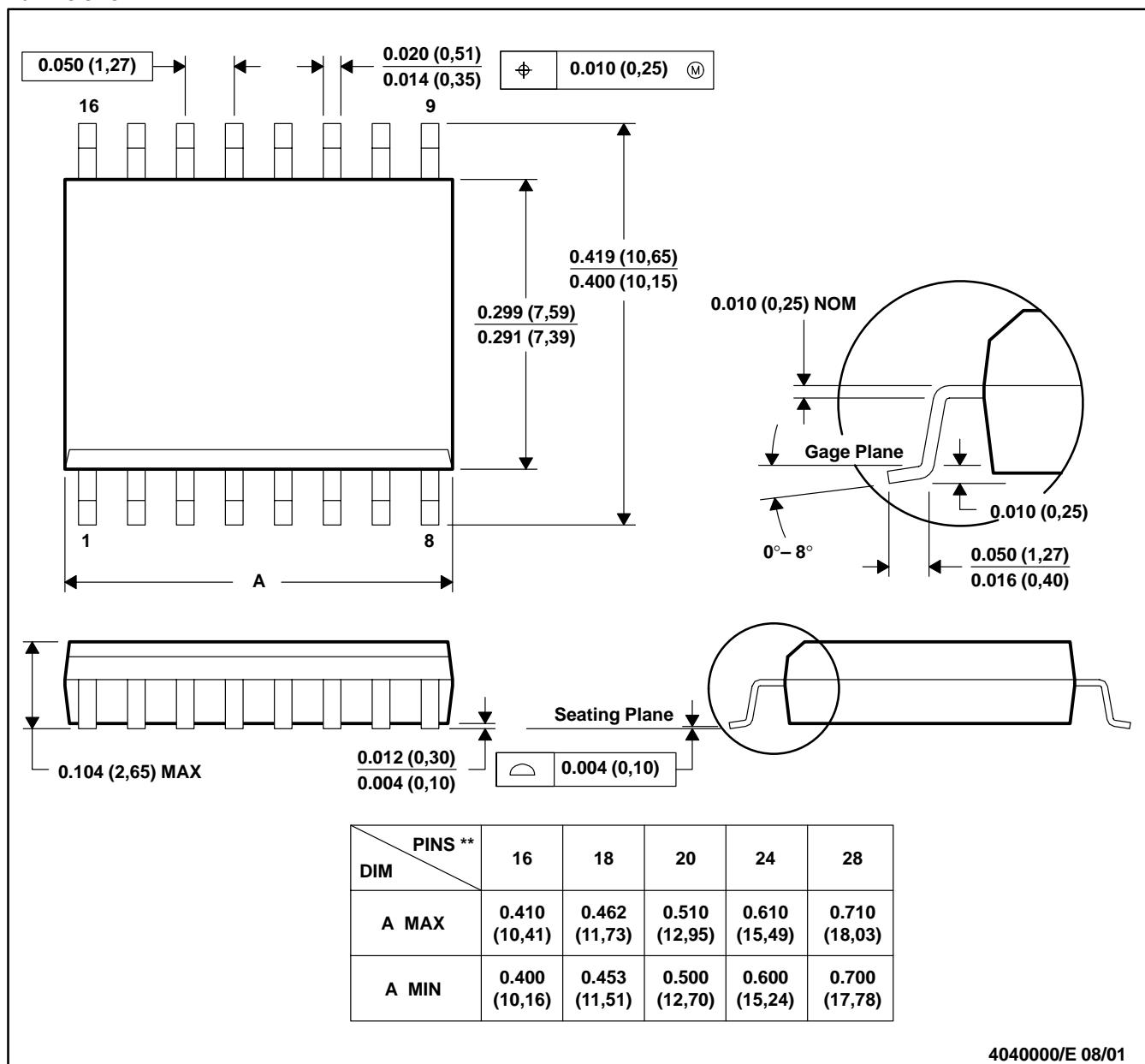
E. Package complies to JEDEC MO-241 variation BC.

4203539-4/E 05/03

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



404000/E 08/01

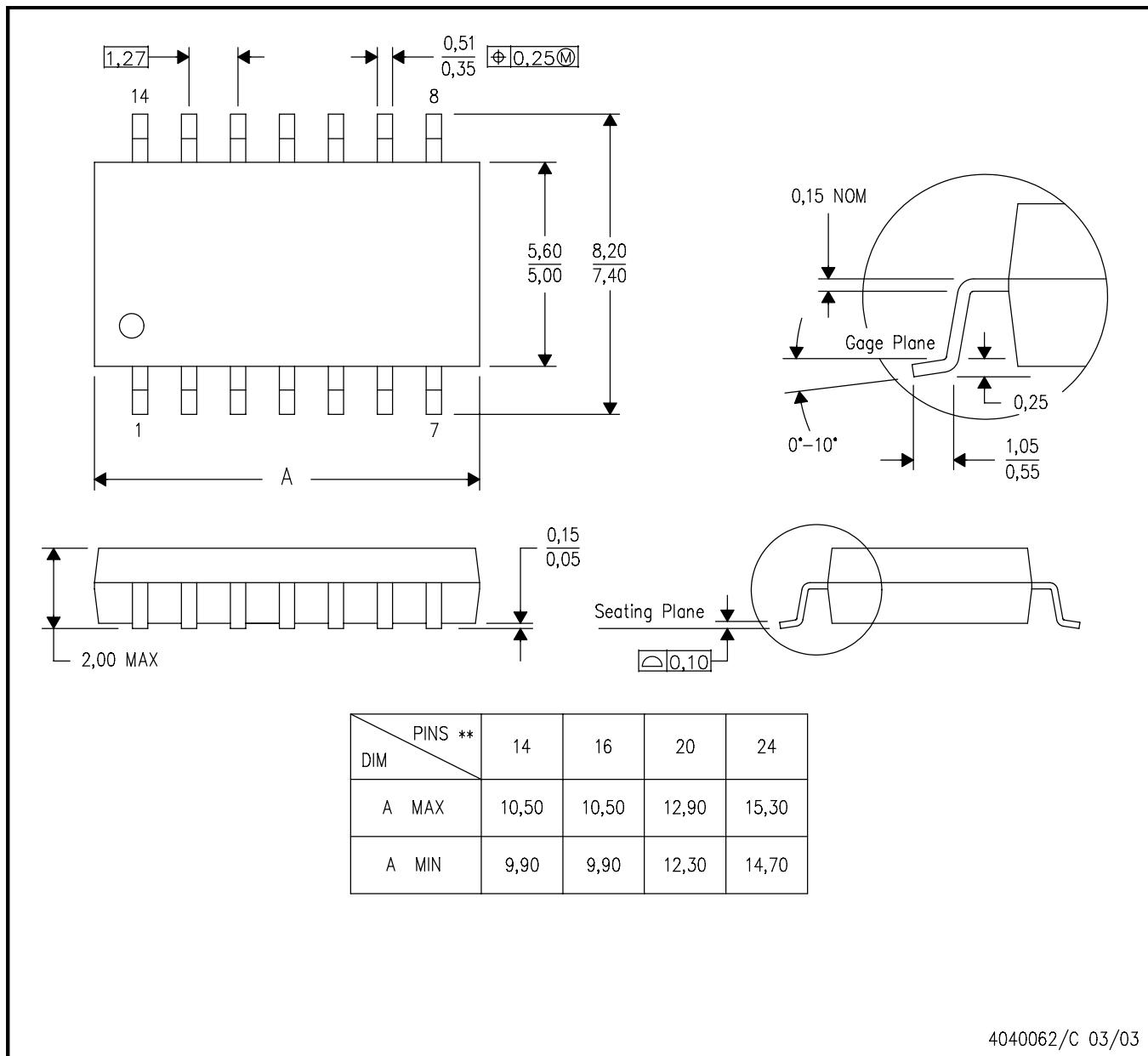
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
 D. Falls within JEDEC MS-013

MECHANICAL DATA

NS (R-PDSO-G)**

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

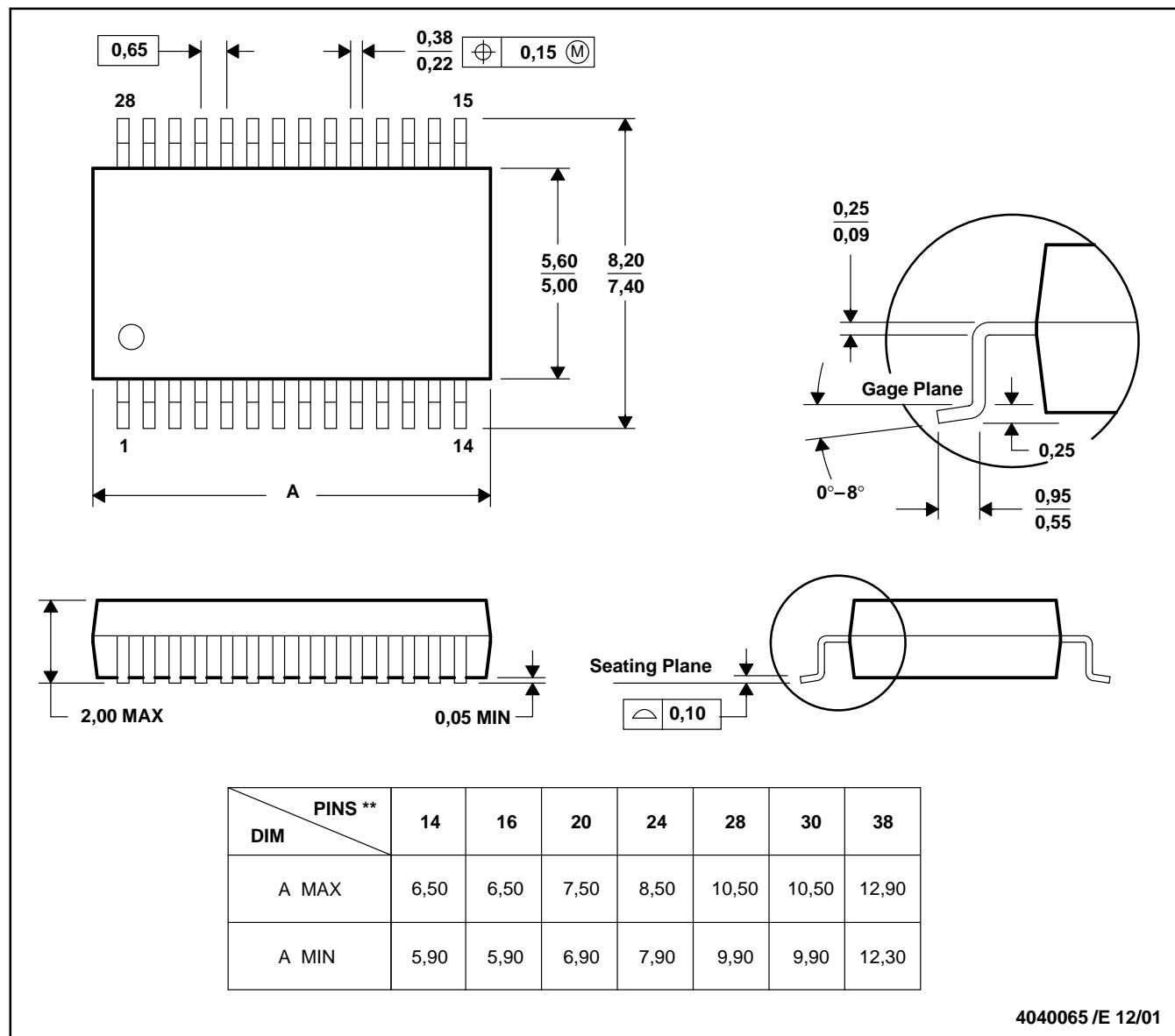


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

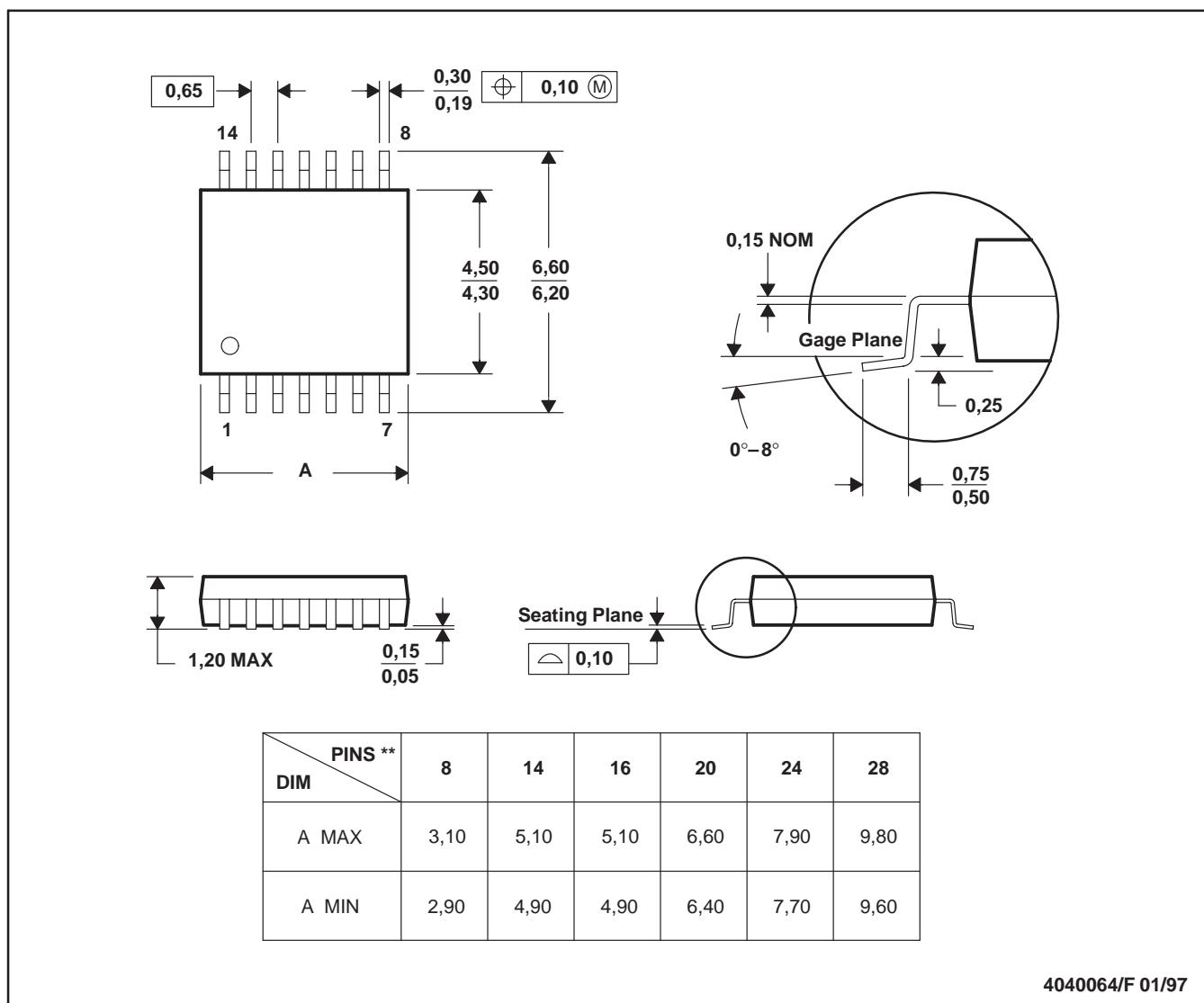


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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