- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**

- **Support Unregulated Battery Operation Down to 2.7 V**

- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**

- **I_{off} and Power-Up 3-State Support Hot Insertion**

- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**

- **Latch-Up Performance Exceeds 500 mA Per JESD 17**

- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
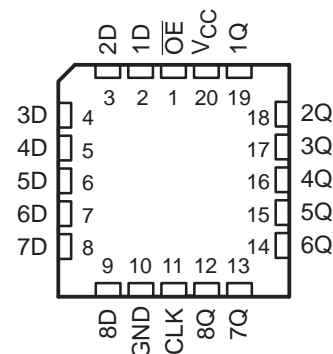 - **200-V Machine Model (A115-A)**

SN54LVTH574 . . . J OR W PACKAGE
SN74LVTH574 . . . DB, DW, NS, OR PW PACKAGE
(TOP VIEW)

$\overline{OE}$	1		20	V_{CC}
1D	2		19	1Q
2D	3		18	2Q
3D	4		17	3Q
4D	5		16	4Q
5D	6		15	5Q
6D	7		14	6Q
7D	8		13	7Q
8D	9		12	8Q
GND	10		11	CLK
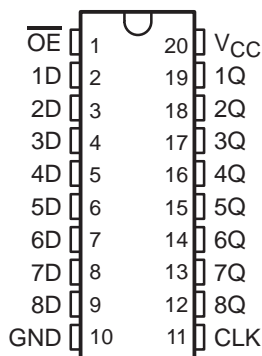
SN74LVTH574 . . . RGY PACKAGE
(TOP VIEW)

$\overline{OE}$ — 1, V_{CC} — 20

1D	2		19	1Q
2D	3		18	2Q
3D	4		17	3Q
4D	5		16	4Q
5D	6		15	5Q
6D	7		14	6Q
7D	8		13	7Q
8D	9		12	8Q

GND — 10, CLK — 11
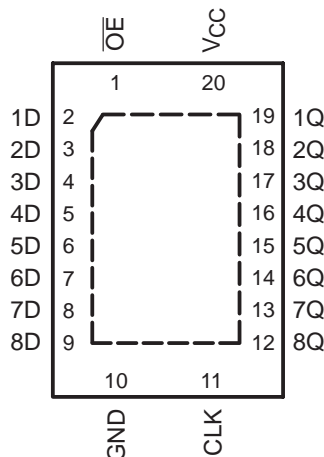
SN54LVTH574 . . . FK PACKAGE
(TOP VIEW)

Top pins: 2D (3), 1D (2), $\overline{OE}$ (1), V_{CC} (20), 1Q (19)

3D	4		18	2Q
4D	5		17	3Q
5D	6		16	4Q
6D	7		15	5Q
7D	8		14	6Q

Bottom pins: 8D (9), GND (10), CLK (11), 8Q (12), 7Q (13)

description/ordering information

These octal flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN – RGY	Tape and reel	SN74LVTH574RGYR	LXH574
	SOIC – DW	Tube	SN74LVTH574DW	LVTH574
		Tape and reel	SN74LVTH574DWR	
	SOP – NS	Tape and reel	SN74LVTH574NSR	LVTH574
	SSOP – DB	Tape and reel	SN74LVTH574DBR	LXH574
	TSSOP – PW	Tube	SN74LVTH574PW	LXH574
		Tape and reel	SN74LVTH574PWR	
	VFBGA – GQN	Tape and reel	SN74LVTH574GQNR	LXH574
	VFBGA – ZQN (Pb-free)		SN74LVTH574ZQNR	
−55°C to 125°C	CDIP – J	Tube	SNJ54LVTH574J	SNJ54LVTH574J
	CFP – W	Tube	SNJ54LVTH574W	SNJ54LVTH574W
	LCCC – FK	Tube	SNJ54LVTH574FK	SNJ54LVTH574FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

description/ordering information (continued)

The eight flip-flops of the 'LVTH574 devices are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

SN74LVTH574 . . . GQN OR ZQN PACKAGE
(TOP VIEW)
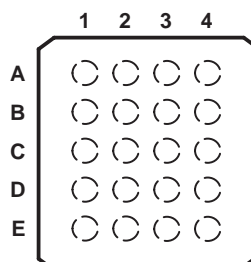
terminal assignments

	1	2	3	4
A	1D	$\overline{OE}$	V_{CC}	1Q
B	3D	3Q	2D	2Q
C	5D	4D	5Q	4Q
D	7D	7Q	6D	6Q
E	GND	8D	CLK	8Q

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic diagram (positive logic)

To Seven Other Channels
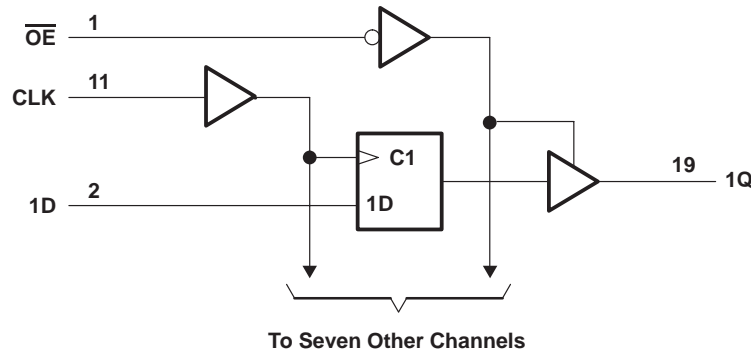
Pin numbers shown are for the DB, DW, FK, J, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} .... –0.5 V to 4.6 V

Input voltage range, V_I (see Note 1) .... –0.5 V to 7 V

Voltage range applied to any output in the high-impedance
or power-off state, V_O (see Note 1) .... –0.5 V to 7 V

Voltage range applied to any output in the high state, V_O (see Note 1) .... –0.5 V to V_{CC} + 0.5 V

Current into any output in the low state, I_O: SN54LVTH574 .... 96 mA

SN74LVTH574 .... 128 mA

Current into any output in the high state, I_O (see Note 2): SN54LVTH574 .... 48 mA

SN74LVTH574 .... 64 mA

Input clamp current, I_{IK} (V_I < 0) .... –50 mA

Output clamp current, I_{OK} (V_O < 0) .... –50 mA

Package thermal impedance, θ_{JA} (see Note 3): DB package .... 70°C/W

(see Note 3): DW package .... 58°C/W

(see Note 3): GQN/ZQN package .... 78°C/W

(see Note 3): NS package .... 60°C/W

(see Note 3): PW package .... 83°C/W

(see Note 4): RGY package .... 37°C/W

Storage temperature range, T_{stg} .... –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and V_O > V_{CC}.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

			SN54LVTH574		SN74LVTH574		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		µs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 5: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH574 MIN	TYP†	MAX	SN74LVTH574 MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 2.7$ V,	$I_I = -18$ mA			−1.2			−1.2	V
V_{OH}		$V_{CC} = 2.7$ V to 3.6 V,	$I_{OH} = -100$ µA	$V_{CC}-0.2$			$V_{CC}-0.2$			V
		$V_{CC} = 2.7$ V,	$I_{OH} = -8$ mA	2.4			2.4			
		$V_{CC} = 3$ V	$I_{OH} = -24$ mA	2						
			$I_{OH} = -32$ mA				2			
V_{OL}		$V_{CC} = 2.7$ V	$I_{OL} = 100$ µA			0.2			0.2	V
			$I_{OL} = 24$ mA			0.5			0.5	
		$V_{CC} = 3$ V	$I_{OL} = 16$ mA			0.4			0.4	
			$I_{OL} = 32$ mA			0.5			0.5	
			$I_{OL} = 48$ mA			0.55				
			$I_{OL} = 64$ mA						0.55	
I_I	Control inputs	$V_{CC} = 0$ or 3.6 V,	$V_I = 5.5$ V			10			10	µA
		$V_{CC} = 3.6$ V,	$V_I = V_{CC}$ or GND			±1			±1	
	Data inputs	$V_{CC} = 3.6$ V	$V_I = V_{CC}$			1			1	
			$V_I = 0$			−5			−5	
I_{off}		$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V						±100	µA
$I_{I(hold)}$	Data inputs	$V_{CC} = 3$ V	$V_I = 0.8$ V	75			75			µA
			$V_I = 2$ V	−75			−75			
		$V_{CC} = 3.6$ V‡,	$V_I = 0$ to 3.6 V						±500	
I_{OZH}		$V_{CC} = 3.6$ V,	$V_O = 3$ V			5			5	µA
I_{OZL}		$V_{CC} = 3.6$ V,	$V_O = 0.5$ V			−5			−5	µA
I_{OZPU}		$V_{CC} = 0$ to 1.5 V, $V_O = 0.5$ V to 3 V, $\overline{OE}$ = don't care				±100*			±100	µA
I_{OZPD}		$V_{CC} = 1.5$ V to 0, $V_O = 0.5$ V to 3 V, $\overline{OE}$ = don't care				±100*			±100	µA
I_{CC}		$V_{CC} = 3.6$ V, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high			0.19			0.19	mA
			Outputs low			5			5	
			Outputs disabled			0.19			0.19	
ΔI_{CC}§		$V_{CC} = 3$ V to 3.6 V, One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND				0.2			0.2	mA
C_i		$V_I = 3$ V or 0			3			3		pF
C_O		$V_O = 3$ V or 0			7			7		pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25°C$.
‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVTH574				SN74LVTH574				UNIT
		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		150		150		150		150	MHz
t_w	Pulse duration, CLK high or low	3.3		3.3		3.3		3.3		ns
t_{su}	Setup time, data before CLK↑	2		2.4		2		2.4		ns
t_h	Hold time, data after CLK↑	0.9		0.9		0.3		0		ns

switching characteristics over recommended free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH574				SN74LVTH574					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
f_{max}			150		150		150			150		MHz
t_{PLH}	CLK	Q	1.7	4.9		5.9	1.8	3	4.5		5.3	ns
t_{PHL}			1.7	4.9		5.5	1.8	3	4.5		5.3	
t_{PZH}	$\overline{OE}$	Q	1.4	5.1		6.5	1.5	3.2	4.8		5.9	ns
t_{PZL}			1.4	5.1		6.1	1.5	3.5	4.8		5.9	
t_{PHZ}	$\overline{OE}$	Q	1	5.9		6.4	2	3.5	4.8		5.1	ns
t_{PLZ}			0.8	4.8		5.3	2	3.2	4.4		4.4	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND
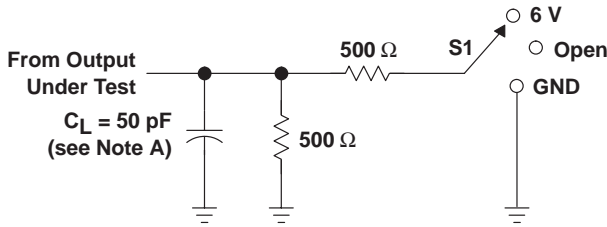
LOAD CIRCUIT
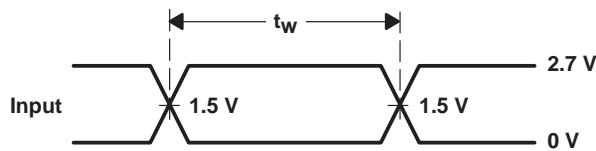
VOLTAGE WAVEFORMS
PULSE DURATION
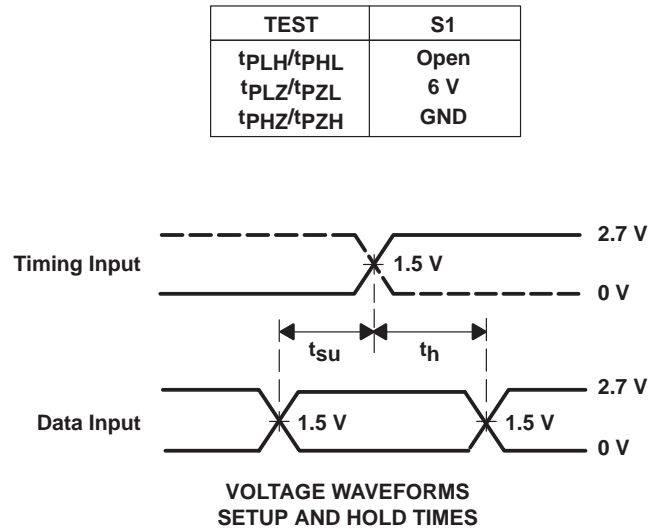
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
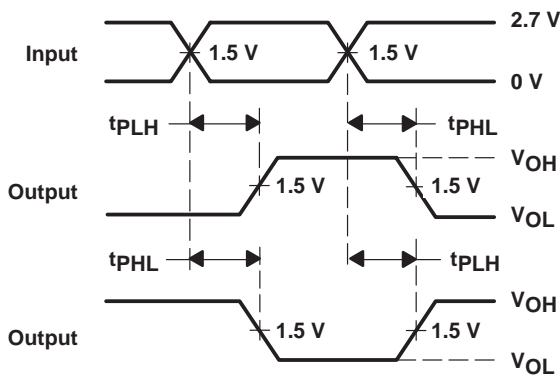
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS
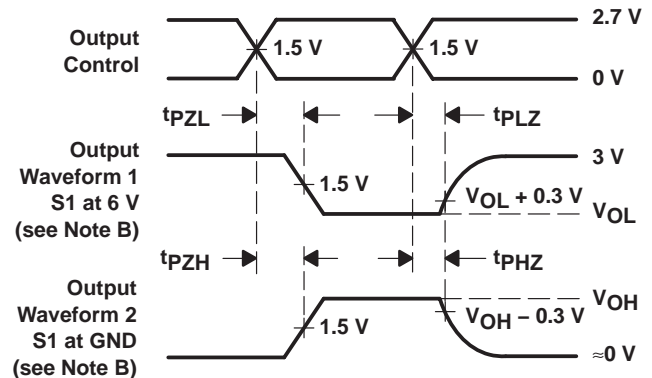
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
   D. The outputs are measured one at a time with one transition per measurement.
   E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

J (R−GDIP−T**)   CERAMIC DUAL IN−LINE PACKAGE
14 LEADS SHOWN

DIM PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

W (R-GDFP-F20)   **CERAMIC DUAL FLATPACK**

0.045 (1,14)
0.026 (0,66)

0.300 (7,62)
0.245 (6,22)

Base and Seating Plane

0.009 (0,23)
0.004 (0,10)

0.100 (2,54)
0.045 (1,14)

0.320 (8,13) MAX

0.022 (0,56)
0.015 (0,38)

1   20

0.540 (13,72)
MAX

0.050 (1,27)

0.005 (0,13) MIN
4 Places

10   11

0.370 (9,40)
0.250 (6,35)

0.370 (9,40)
0.250 (6,35)

4040180-4/D 07/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil-Std 1835 GDFP2-F20

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1

FK (S-CQCC-N**)   **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

0.020 (0,51) / 0.010 (0,25)

0.020 (0,51) / 0.010 (0,25)

0.080 (2,03) / 0.064 (1,63)

0.055 (1,40) / 0.045 (1,14)

0.045 (1,14) / 0.035 (0,89)

0.028 (0,71) / 0.022 (0,54)

0.045 (1,14) / 0.035 (0,89)

0.050 (1,27)
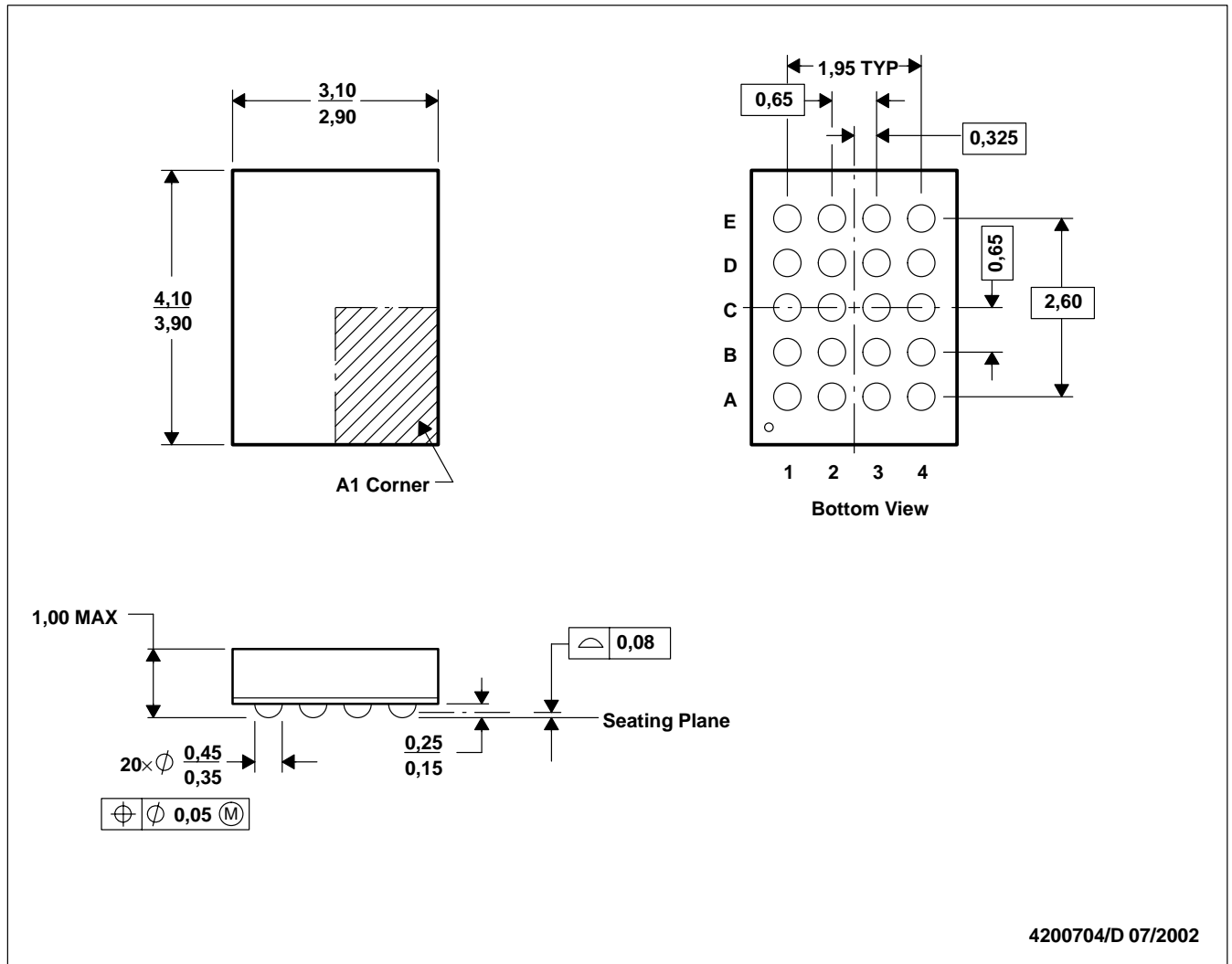
4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
             B. This drawing is subject to change without notice.
             C. This package can be hermetically sealed with a metal lid.
             D. The terminals are gold plated.
             E. Falls within JEDEC MS-004

1

GQN (R-PBGA-N20)   **PLASTIC BALL GRID ARRAY**

3,10
2,90

4,10
3,90

A1 Corner

1,95 TYP

0,65

0,325

E

D

C

B

A

0,65

2,60

1   2   3   4

Bottom View

1,00 MAX

◯ 0,08

Seating Plane

20× ⌀ 0,45
        0,35

0,25
0,15

⊕ ⌀ 0,05 Ⓜ
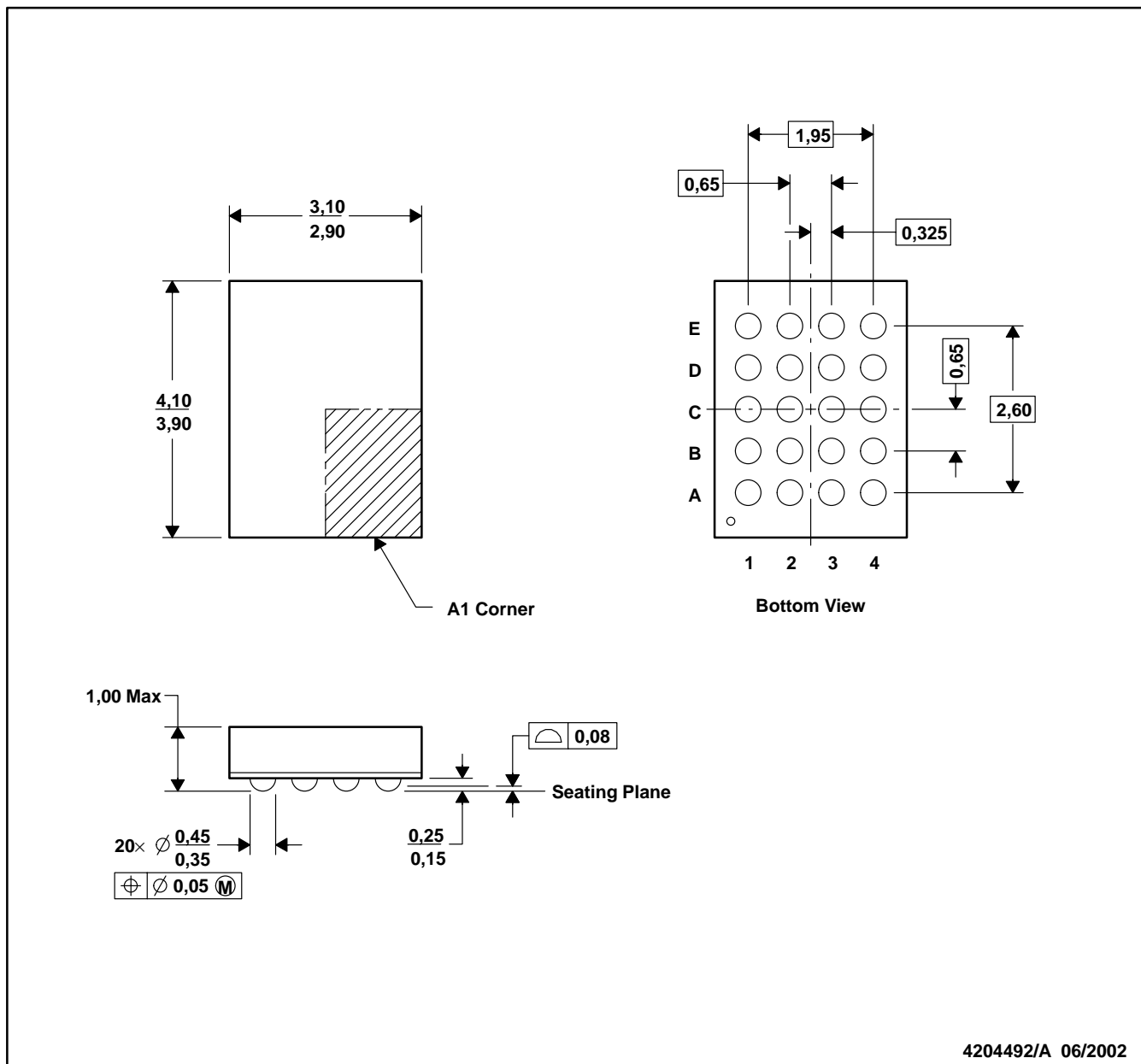
4200704/D 07/2002

NOTES: A. All linear dimensions are in millimeters.
      B. This drawing is subject to change without notice.
      C. MicroStar Junior™ configuration
      D. Falls within JEDEC MO-225 variation BC.
      E. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

MicroStar Junior is a trademark of Texas Instruments.

1

ZQN (R-PBGA-N20) PLASTIC BALL GRID ARRAY

3,10
2,90

4,10
3,90

A1 Corner

1,95

0,65

0,325

E
D
C
B
A

0,65

2,60

1   2   3   4

Bottom View

1,00 Max

0,08

Seating Plane

20× ⌀ 0,45
0,35

0,25
0,15

⊕ ⌀ 0,05 Ⓜ

4204492/A 06/2002
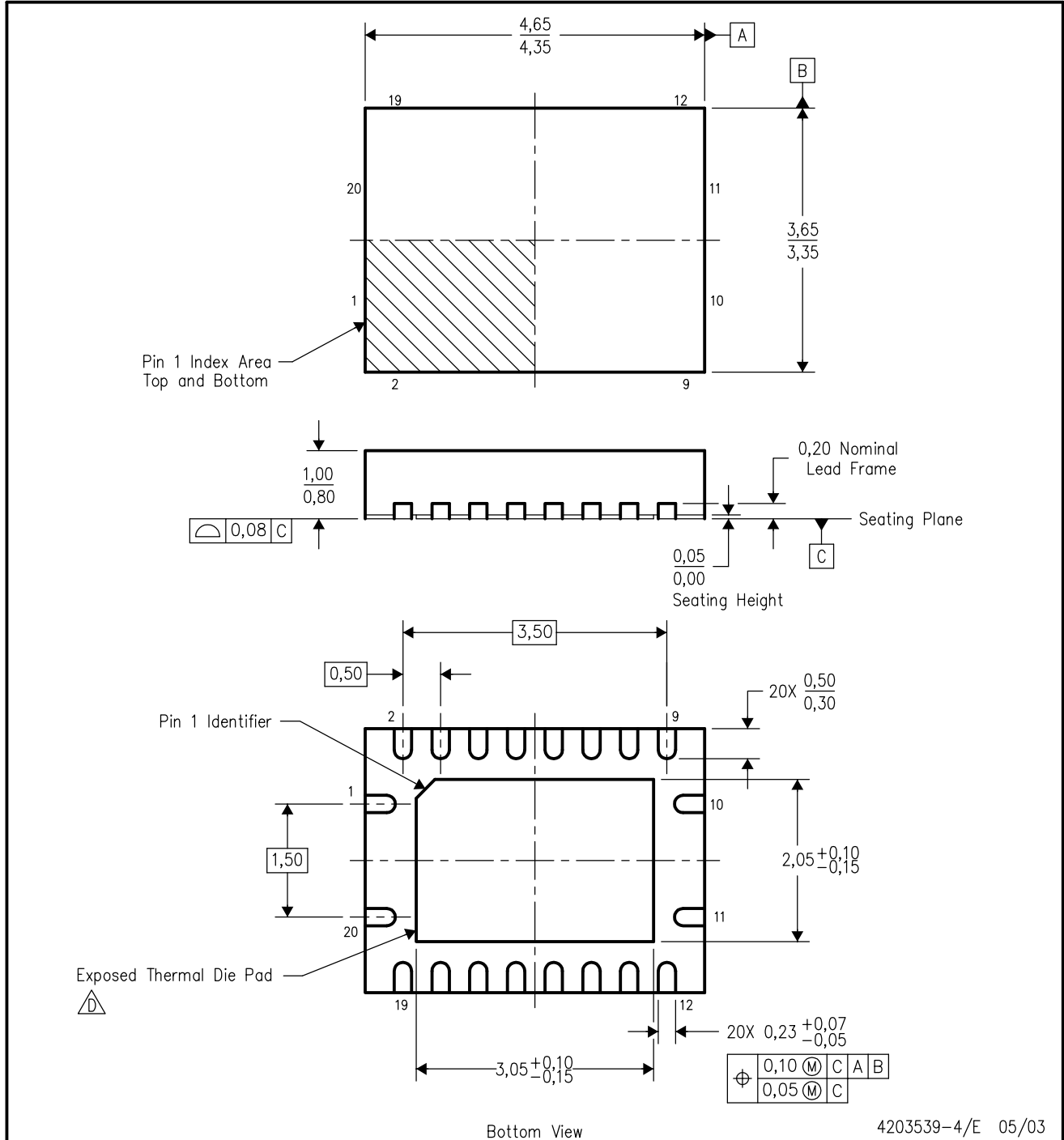
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ configuration.
D. Fall within JEDEC MO-225 variation BC.
E. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead)SnPb).

MicroStar Junior is a trademark of Texas Instruments.

TEXAS INSTRUMENTS

RGY (R—PQFP—N20) **PLASTIC QUAD FLATPACK**

Pin 1 Index Area
Top and Bottom

0,20 Nominal
Lead Frame

Seating Plane

Seating Height

Pin 1 Identifier

Exposed Thermal Die Pad

Bottom View
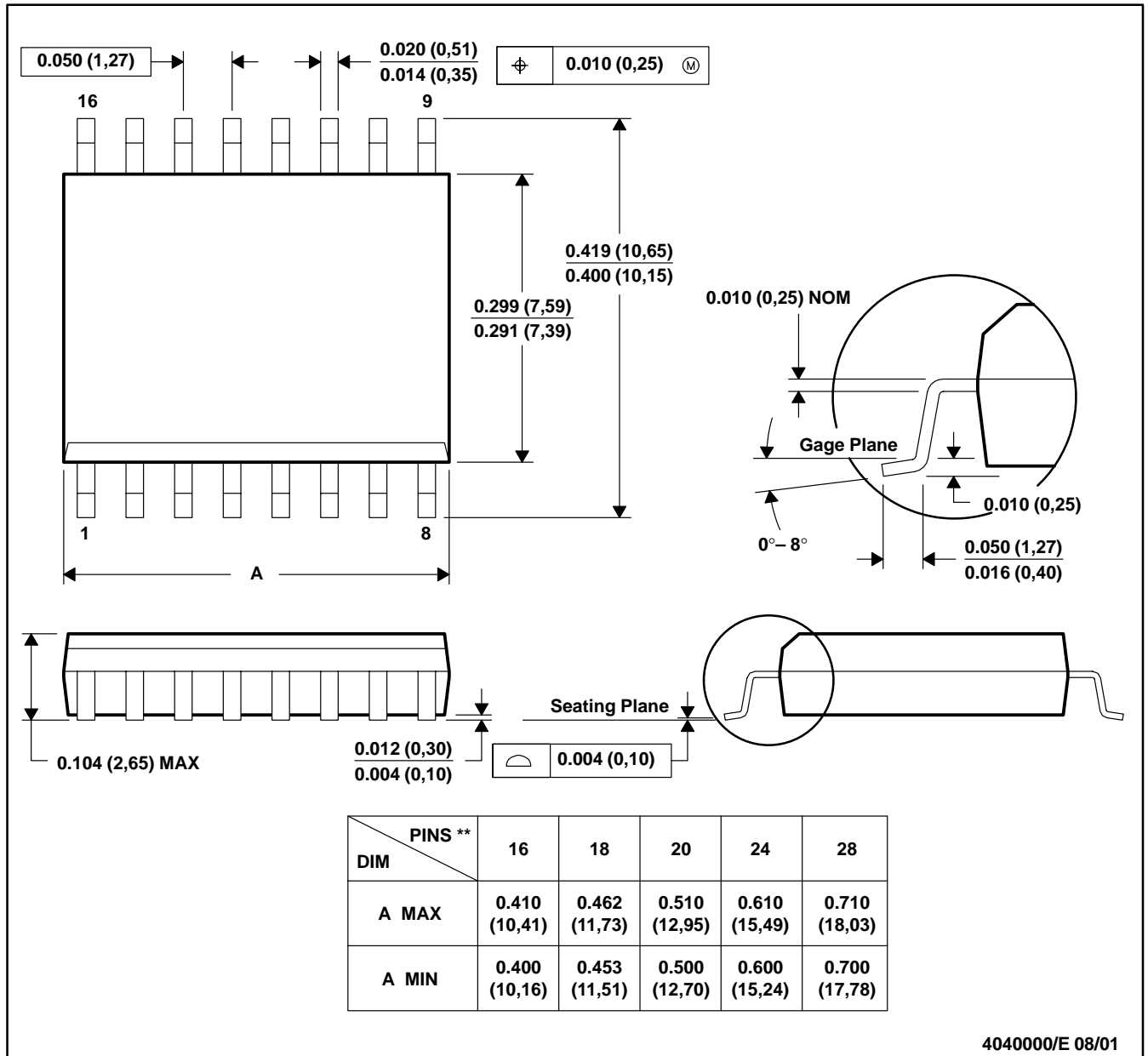
4203539—4/E 05/03

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. QFN (Quad Flatpack No—Lead) package configuration.

         D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane.
             This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.

         E. Package complies to JEDEC MO—241 variation BC.

TEXAS
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DW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN

0.050 (1,27)

0.020 (0,51)
0.014 (0,35)

0.010 (0,25) Ⓜ

16

9

0.419 (10,65)
0.400 (10,15)

0.299 (7,59)
0.291 (7,39)

0.010 (0,25) NOM

Gage Plane

0°– 8°

0.010 (0,25)

0.050 (1,27)
0.016 (0,40)

1

8

A

0.104 (2,65) MAX

Seating Plane

0.012 (0,30)
0.004 (0,10)

0.004 (0,10)

DIM \ PINS **	16	18	20	24	28
A MAX	0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/E 08/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

TEXAS INSTRUMENTS

1

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

	PINS **	14	16	20	24
DIM					
A	MAX	10,50	10,50	12,90	15,30
A	MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

0,65

0,38
0,22   ⊕ 0,15 Ⓜ

28   15

5,60   8,20
5,00   7,40

1   14

A

0,25
0,09

Gage Plane

0,25

0°–8°

0,95
0,55

2,00 MAX   0,05 MIN

Seating Plane

△ 0,10

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
            B. This drawing is subject to change without notice.
            C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
            D. Falls within JEDEC MO-153

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