- **Designed to Reduce Reflection Noise**
- **Repetitive Peak Forward Current to 200 mA**
- **16-Bit Array Structure Suited for Bus-Oriented Systems**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)

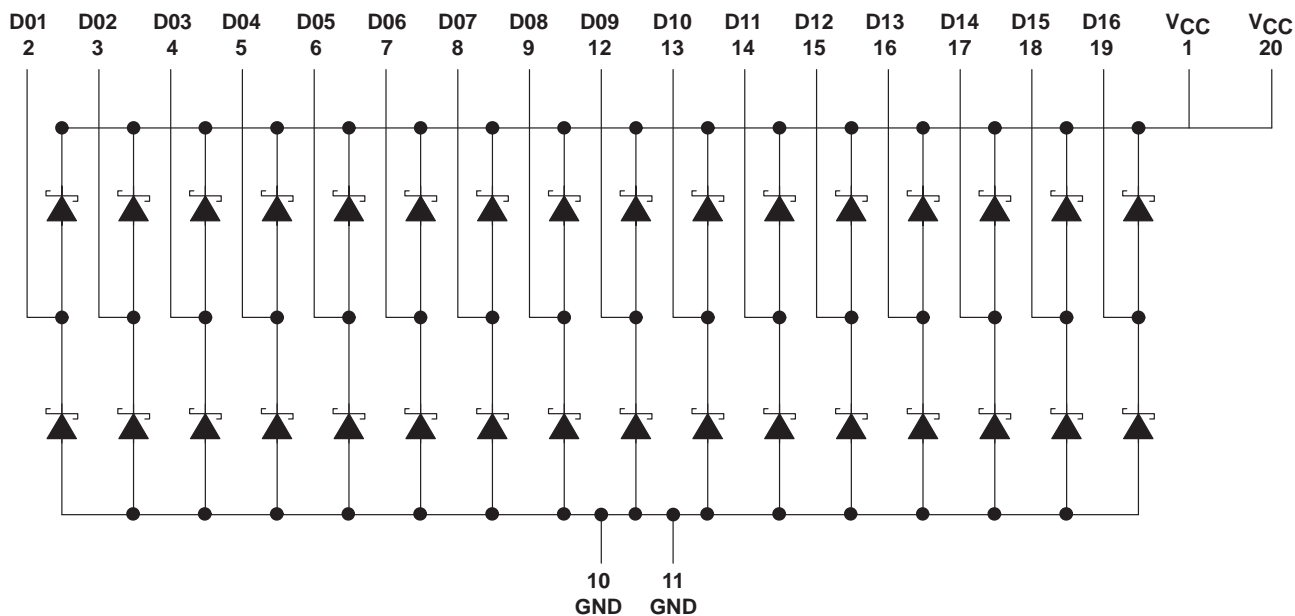|			
V_{CC}	1	20	V_{CC}
D01	2	19	D16
D02	3	18	D15
D03	4	17	D14
D04	5	16	D13
D05	6	15	D12
D06	7	14	D11
D07	8	13	D10
D08	9	12	D09
GND	10	11	GND
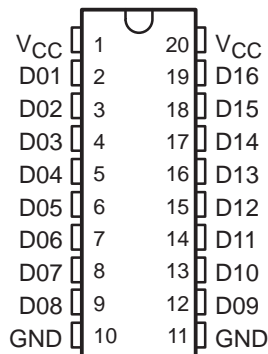
description

This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of a 16-bit high-speed Schottky diode array suitable for clamping to V_{CC} and/or GND.

The SN74S1053 is characterized for operation from 0°C to 70°C.

schematic diagrams

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady-state reverse voltage, V_R . . . . 7 V

Continuous forward current, I_F: Any D terminal from GND or to V_{CC} . . . . 50 mA

Total through all GND or V_{CC} terminals . . . . 170 mA

Repetitive peak forward current‡, I_{FRM}: Any D terminal from GND or V_{CC} . . . . 200 mA

Total through all GND or V_{CC} terminals . . . . 1.2 A

Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 1) . . . . 625 mW

Operating free-air temperature range . . . . 0°C to 70°C

Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ These values apply for $t_w \leq 100\ \mu s$, duty cycle ≤ 20%.

NOTE 1: For operation above 25°C free-air temperature, derate linearly at the rate of 5 m/W/°C.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 2)

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
V_F	Static forward voltage	To V_{CC}	$I_F = 18$ mA		0.85	1.05	V
			$I_F = 50$ mA		1.05	1.3	
		From GND	$I_F = 18$ mA		0.75	0.95	
			$I_F = 50$ mA		0.95	1.2	
V_{FM}	Peak forward voltage		$I_F = 200$ mA		1.45		V
I_R	Static reverse current	To V_{CC}	$V_R = 7$ V			5	μA
		From GND				5	
C_t	Total capacitance	$V_R = 0$ V,	f = 1 MHz		8	16	pF
		$V_R = 2$ V,	f = 1 MHz		4	8	

§ All typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.

NOTE 2: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

multiple-diode operation

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
I_X	Internal crosstalk current	Total I_F current = 1 A,	See Note 3		0.8	2	mA
		Total I_F current = 198 mA,	See Note 3		0.02	0.2	

§ All typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.

NOTE 3: I_X is measured under the following conditions with one diode static, and all others switching:
  Switching diodes: $t_w = 100\ \mu s$, duty cycle = 20%
  Static diode: $V_R = 5$ V
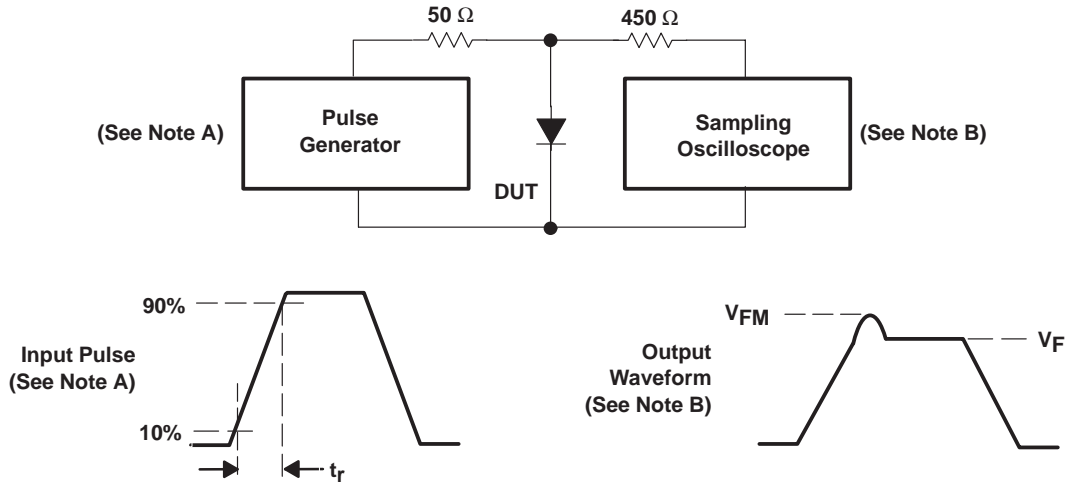 The static diode input current is the internal crosstalk current I_X.

switching characteristics, $T_A = 25$°C (see Figures 1 and 2)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
t_{rr}	Reverse recovery time	$I_F = 10$ mA,	$I_{RM(REC)} = 10$ mA,	$I_{R(REC)} = 1$ mA,	$R_L = 100\ \Omega$		8	16	ns

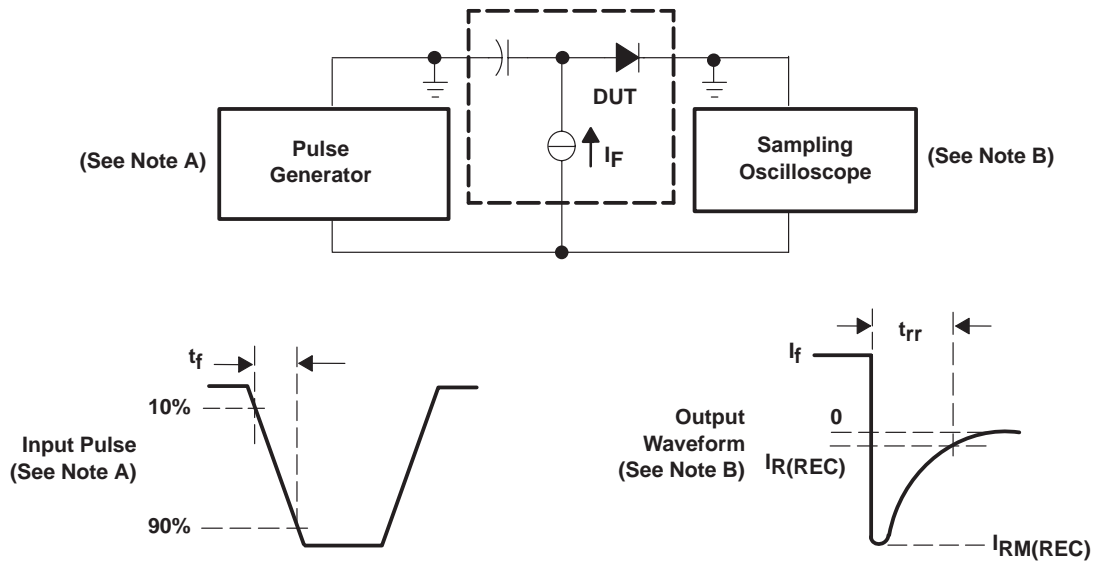## PARAMETER MEASUREMENT INFORMATION

NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: $t_r = 20$ ns, $Z_O = 50$ Ω, freq = 500 Hz, duty cycle = 1%.
B. The output waveform is monitored by an oscilloscope having the following characteristics: $t_r \leq 350$ ps, $R_i = 50$ Ω, $C_i \leq 5$ pF.

Figure 1. Forward Recovery Voltage

NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: $t_f = 0.5$ ns, $Z_O = 50$ Ω, $t_w \geq 50$ ns, duty cycle = 1%.
B. The output waveform is monitored by an oscilloscope having the following characteristics: $t_r \leq 350$ ps, $R_i = 50$ Ω, $C_i \leq 5$ pF.

Figure 2. Reverse Recovery Time

APPLICATION INFORMATION

Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.) or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74S1053 diode termination array helps suppress negative transients caused by transmission-line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver reduce negative transients, but they also can increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current when the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients is tracked by the current-voltage characteristic curve for that diode. Typical current versus voltage curves for the SN74S1053 are shown in Figures 3 and 4.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 5 was evaluated. The resulting waveforms with and without the diode are shown in Figure 6.

The maximum effectiveness of the diode arrays in suppressing negative transients occurs when the diode arrays are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes also can be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.
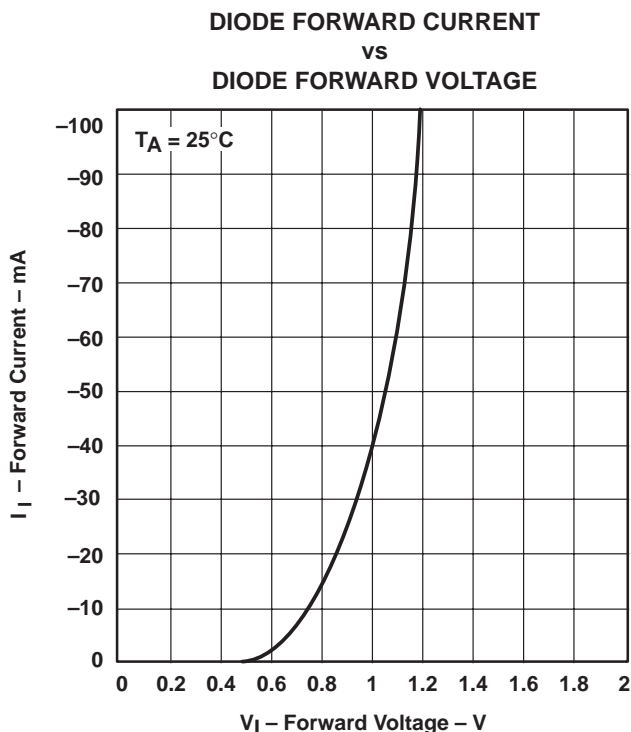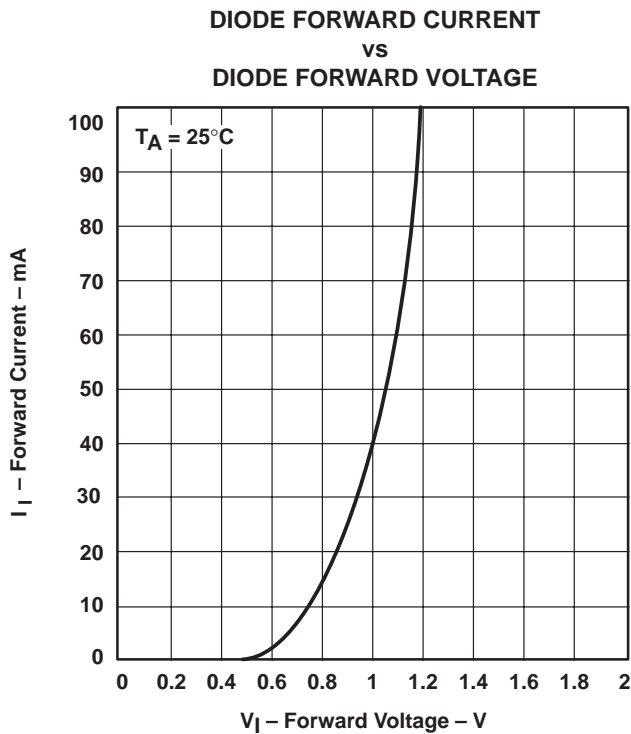
**DIODE FORWARD CURRENT
vs
DIODE FORWARD VOLTAGE**

**Figure 3. Typical Input Current vs Input Voltage
(Lower Diode)**

DIODE FORWARD CURRENT
vs
DIODE FORWARD VOLTAGE

Figure 4. Typical Input Current vs Input Voltage
(Upper Diode)

APPLICATION INFORMATION

Z_O = 50 Ω
Length = 36 in.
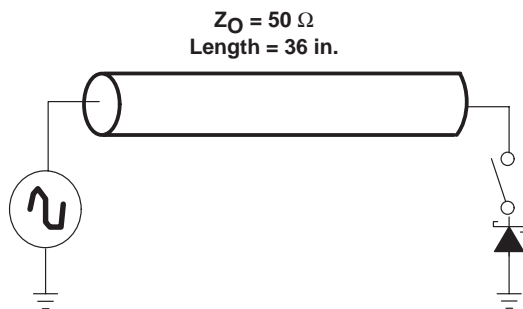
Figure 5. Diode Test Setup

31.500 ns   56.500 ns   81.500 ns

End-of-Line Without Diode

End-of-Line With Diode

Vmarker 1

Vmarker 2

Ch 2 = 1.880 V/div
Timebase = 5.00 ns/V
Memory 1 = 1.880 V/div
Vmarker 1 = −1.353 V
Vmarker 2 = −3.647 V

Offset = 0.000 V
Delay = 56.500 ns
Delta V = −2.293 V
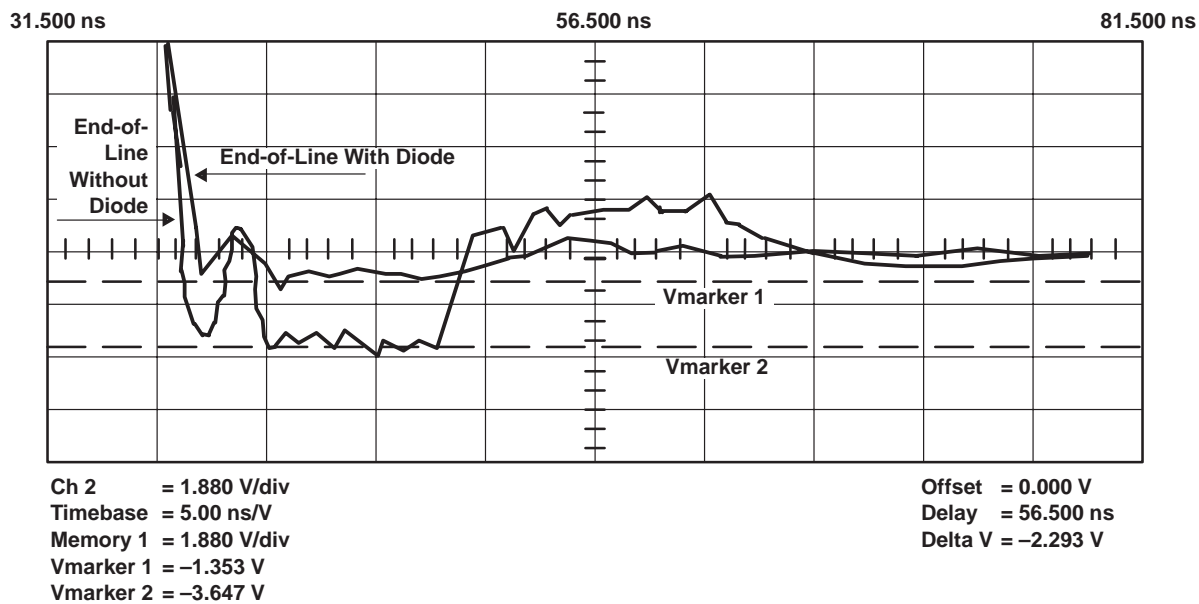
Figure 6. Oscilloscope Display

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74S1053DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S1053DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S1053DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S1053DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S1053DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S1053DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S1053DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S1053N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S1053NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S1053NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S1053NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S1053PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S1053PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S1053PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S1053PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S1053PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S1053PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame

retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

Cavity

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74S1053DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74S1053DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74S1053PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74S1053DBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74S1053DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74S1053PWR	TSSOP	PW	20	2000	346.0	346.0	33.0

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

NS (R-PDSO-G)**   PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DW (R−PDSO−G20)   PLASTIC SMALL−OUTLINE PACKAGE

0.512 (13,00)
0.496 (12,60)

20

11

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1

10

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−4/F 06/2004

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D. Falls within JEDEC MS−013 variation AC.

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N (R−PDIP−T**)
16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.