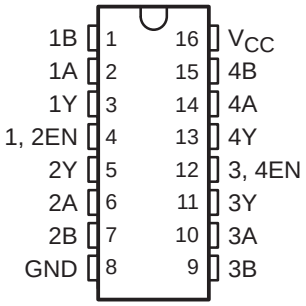
SLLS046C – JANUARY 1989 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ITU Recommendations V.10, V.11, X.26, and X.27**
- **Designed to Operate Up To 20 Mbaud**
- **–7 V to 7 V Common-Mode Input Voltage Range With 300-mV Sensitivity**
- **3-State TTL-Compatible Outputs**
- **High Input Impedance . . . 12 kΩ Min**
- **Input Hysteresis . . . 120 mV Typ**
- **Single 5-V Supply Operation**
- **Low Supply Current Requirement 35 mA Max**
- **Improved Speed and Power Consumption Compared to MC3486**

D OR N PACKAGE
(TOP VIEW)



description

The SN75ALS199 is a monolithic, quadruple line receiver with 3-state outputs designed using advanced, low-power, Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication, providing significantly less power consumption and permitting much higher data throughput than other designs. The device meets the specification of ITU Recommendations V.10, V.11, X.26, and X.27.

The SN75ALS199 features 3-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the ouptuts will always be high if the inputs are open. The device is optimized for balanced multipoint bus transmission at rates up to 20 megabits per second. The input features high-input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ±300 mV over a common-mode input voltage range of ±7 V. It also features an active-high enable function for each of two receiver pairs. The SN75ALS199 is designed for optimum performance when used with the SN75ALS194 quadruple, differential line driver.

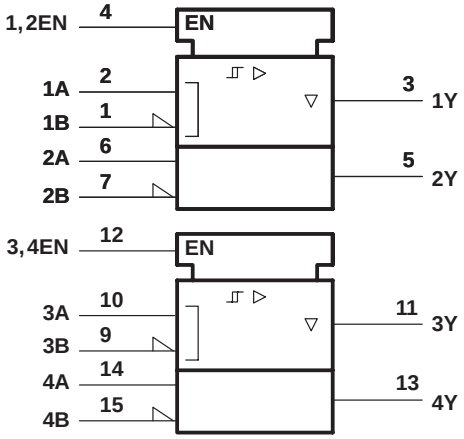
The SN75ALS199 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A – B	EN	OUTPUT Y
$V_{ID} \geq 0.3$ V	H	H
-0.3 V $< V_{ID} < 0.3$ V	H	?
$V_{ID} \leq -0.3$ V	H	L
X	L	Z
Open	H	H

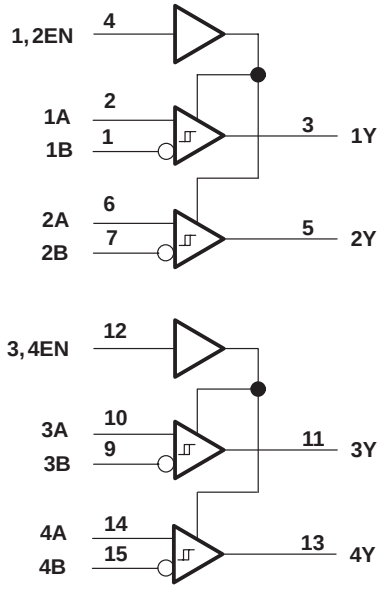
H = high level, L = low level, X = irrelevant,
? = indeterminate, Z = high impedance (off)

logic symbol†

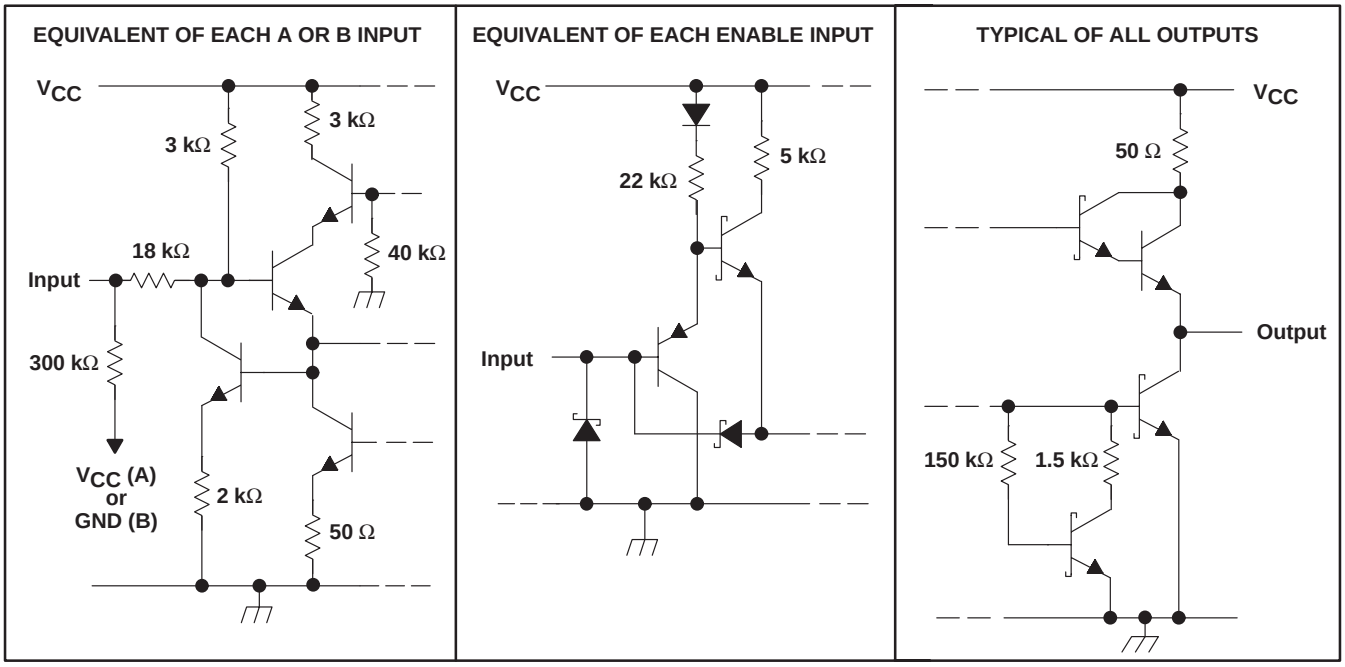


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I (A or B inputs) . . . . . ±15 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±15 V
Enable input voltage, V_I . . . . . 7 V
Low-level output current, I_{OL} . . . . . 50 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Differential input voltage, V_{ID}			±12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			– 400	µA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage					300	mV
V_{IT-}	Negative-going input threshold voltage			–300‡			mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				120		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 300 mV,	I_{OH} = – 400 μA	2.7	3.6		V
V_{OL}	Low-level output voltage	V_{ID} = – 300 mV	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_{IL} = 0.8 V, V_{ID} = – 3 V,	V_O = 2.7 V			20	μA
		V_{IL} = 0.8 V, V_{IO} = 3 V,	V_O = 0.5 V			–20	
I_I	Line input current	Other input at 0 V, See Note 3	V_I = 15 V		0.7	1.2	mA
			V_I = –15 V		–1	–1.7	
I_{IH}	High-level enable-input current		V_{IH} = 2.7 V			20	μA
			V_{IH} = 5.25 V			100	
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				–100	μA
	Input resistance			12	18		kΩ
I_{OS}	Short-circuit output current§	V_{ID} = 3 V,	V_O = 0	–15	–78	–130	mA
I_{CC}	Supply current	Outputs disabled			22	35	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 3: Refer to ITU Recommendations V.10 and V.11 for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = 0 V to 3 V, See Figure 2	C_L = 15 pF,		15	22	ns
t_{PHL}	Propagation delay time, high- to low-level output				15	22	
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PZL}	Output enable time to low level				11	25	
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PLZ}	Output disable time from low level				15	22	

PARAMETER MEASUREMENT INFORMATION

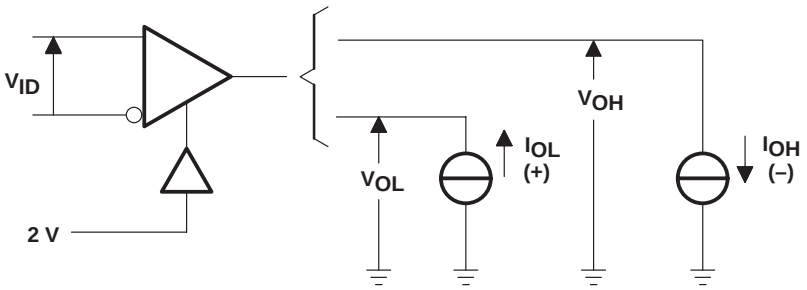
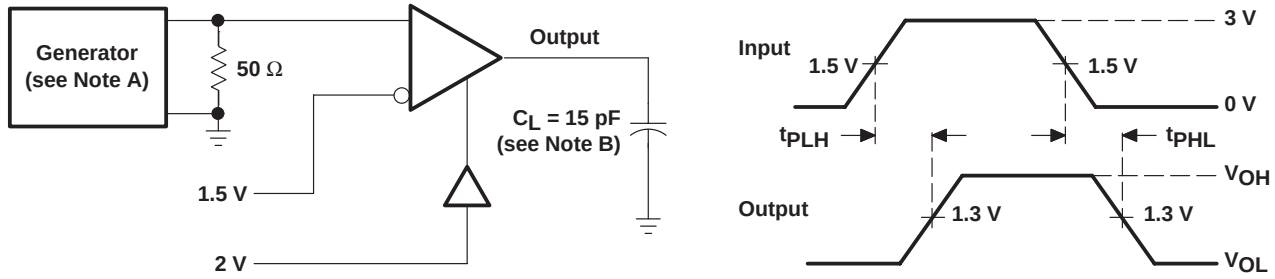


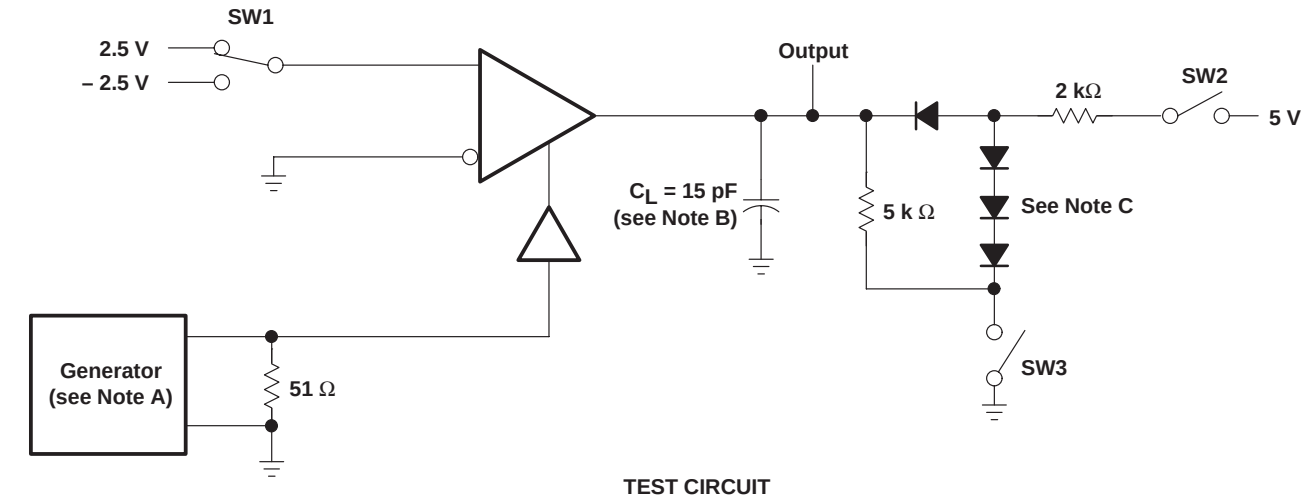
Figure 1. V_{OH} and V_{OL} Test Circuit



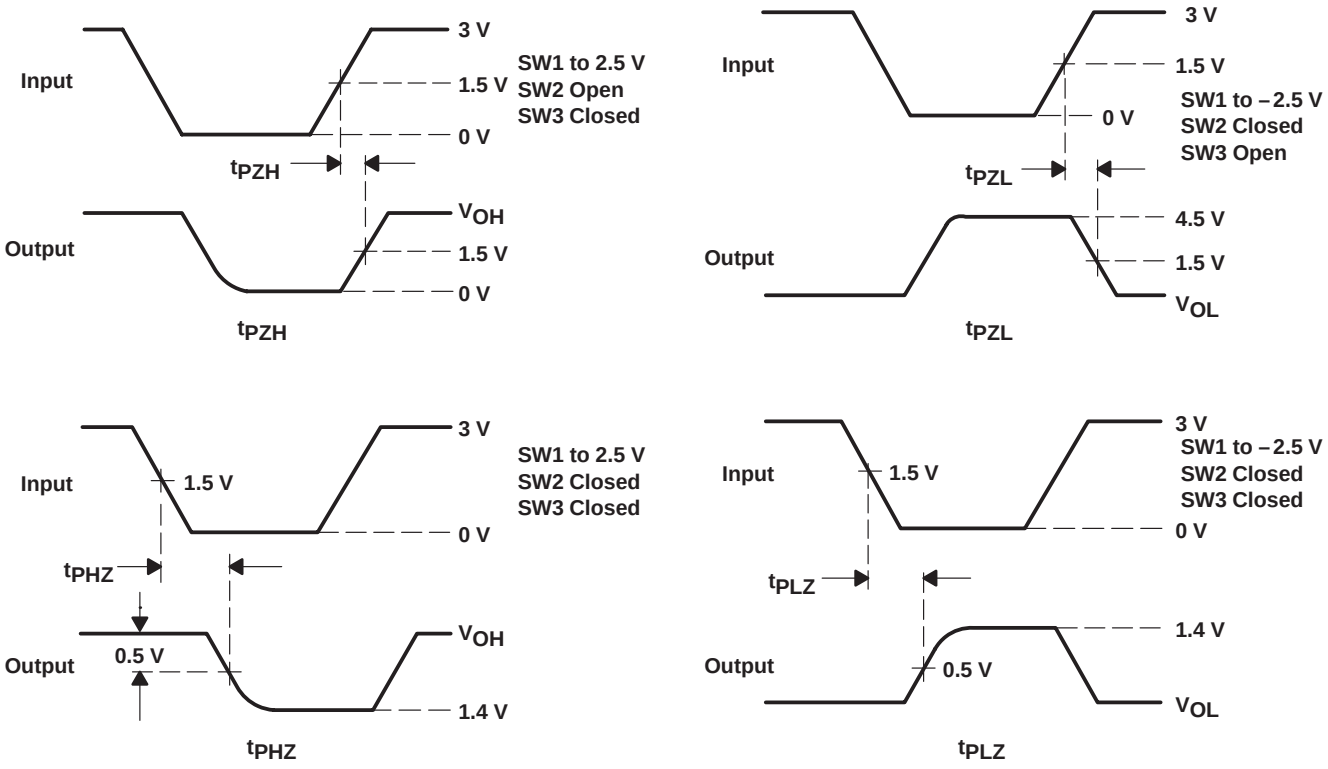
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

Figure 3. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

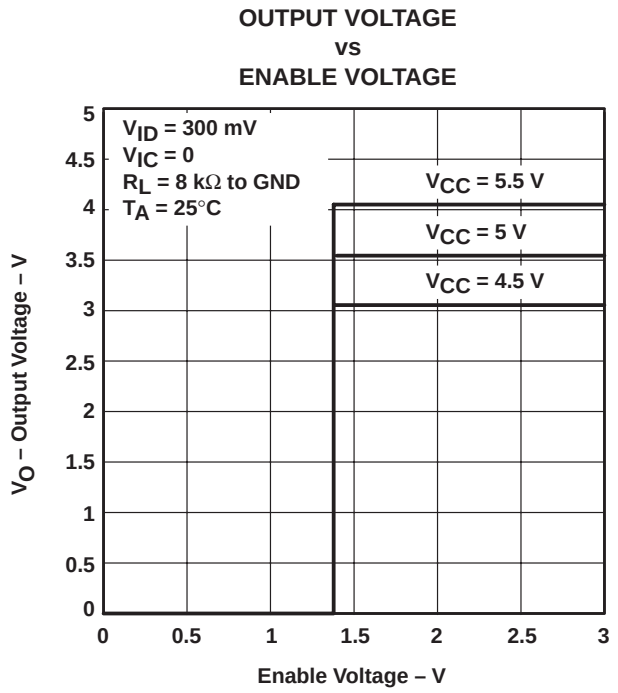


Figure 4

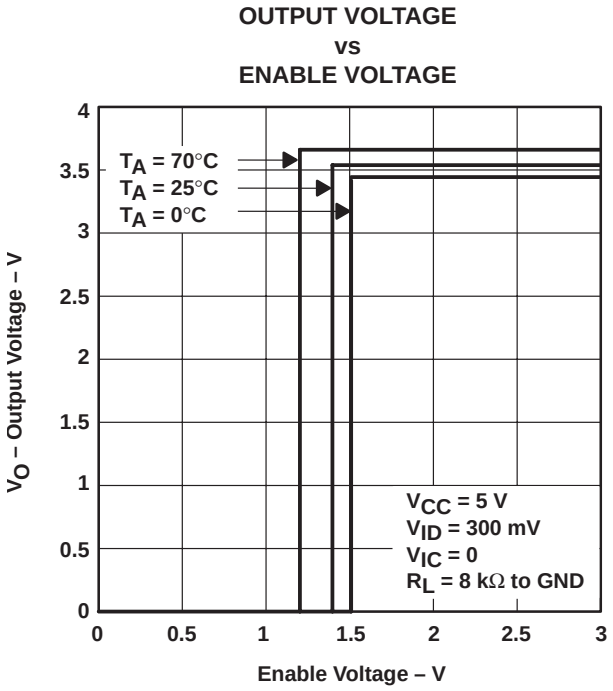


Figure 5

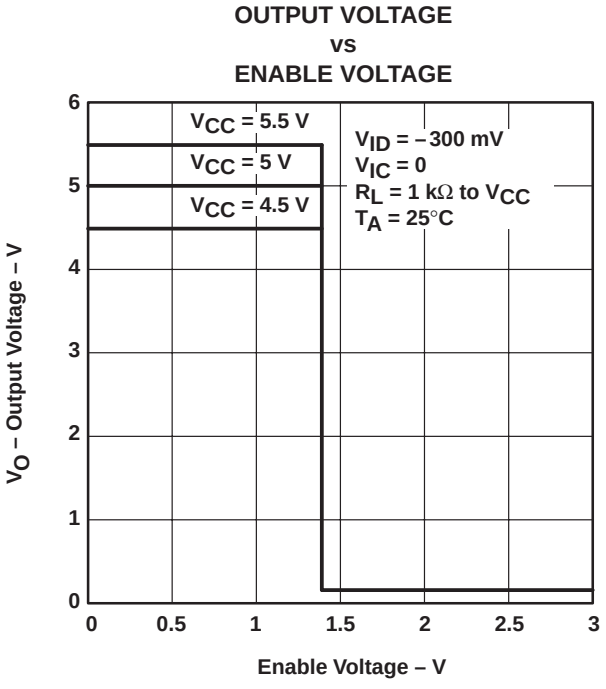


Figure 6

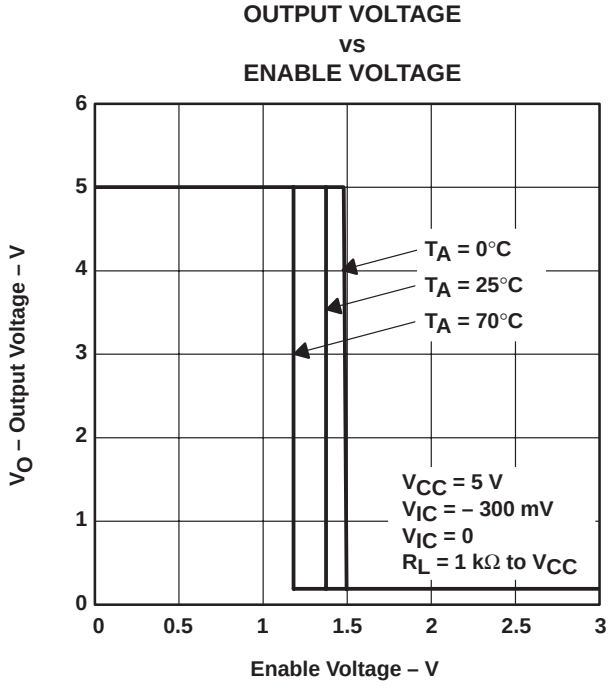


Figure 7

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

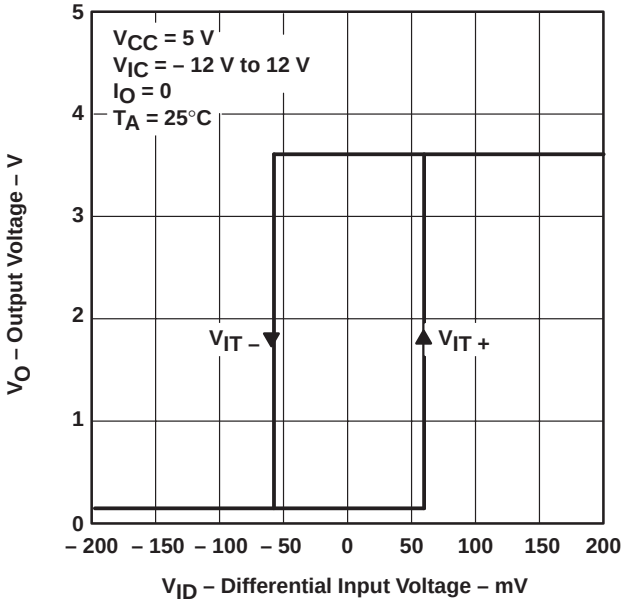


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

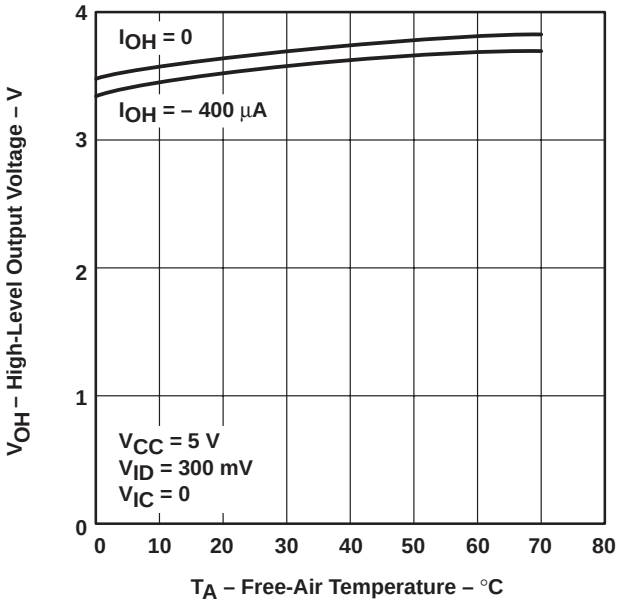


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

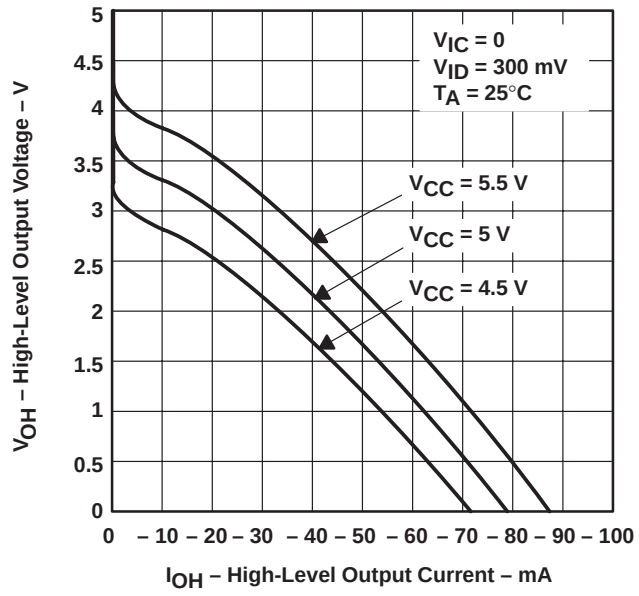


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

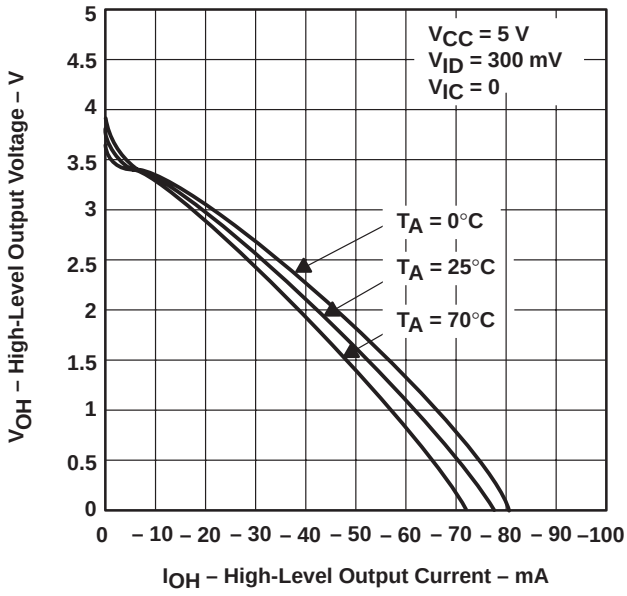


Figure 11

TYPICAL CHARACTERISTICS

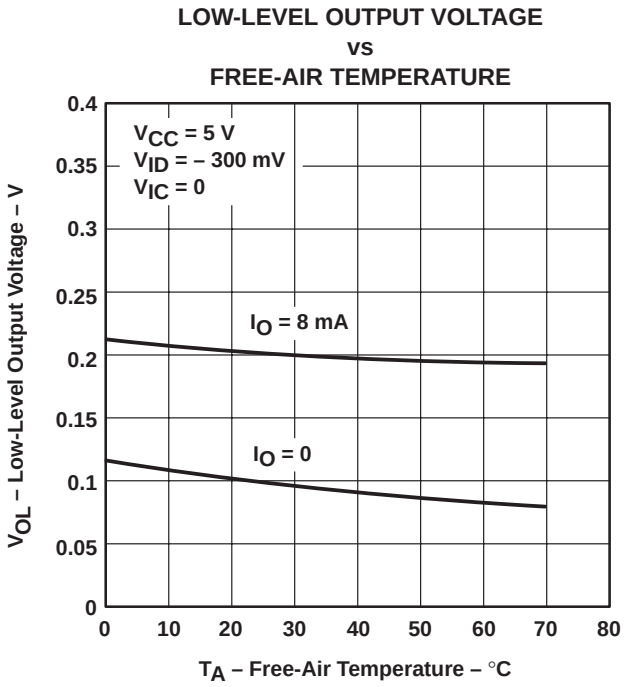


Figure 12

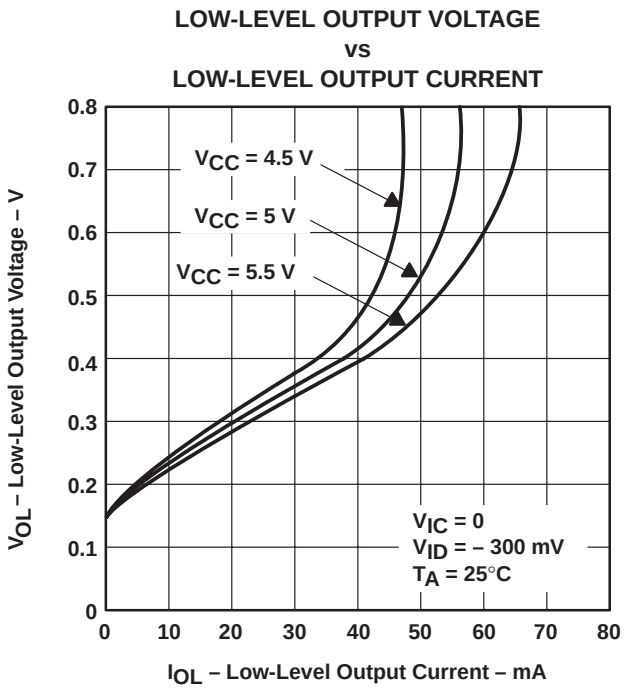


Figure 13

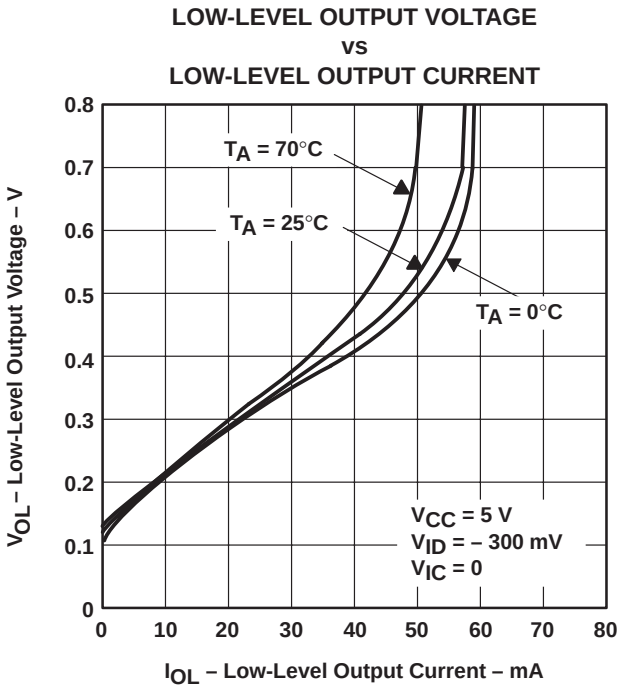


Figure 14

TYPICAL CHARACTERISTICS

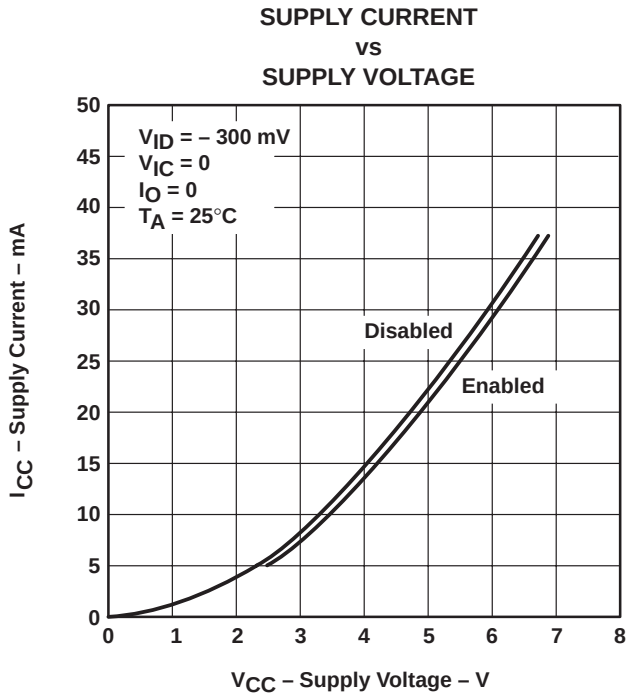


Figure 15

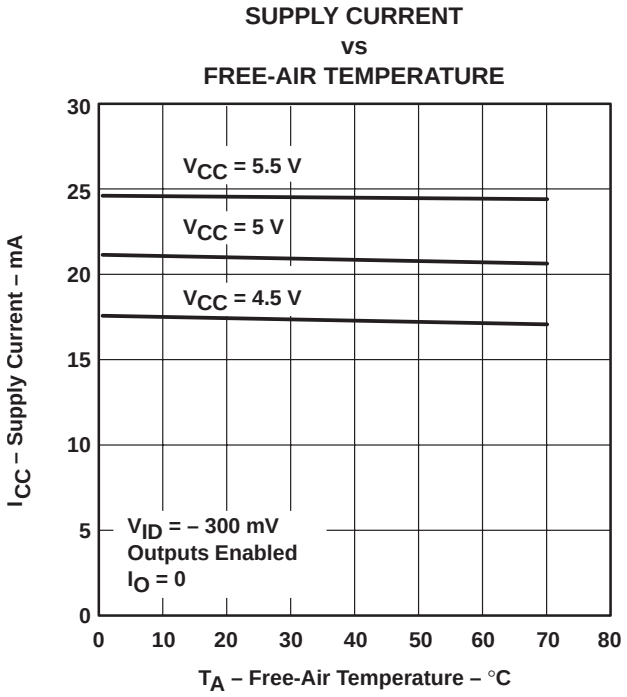


Figure 16

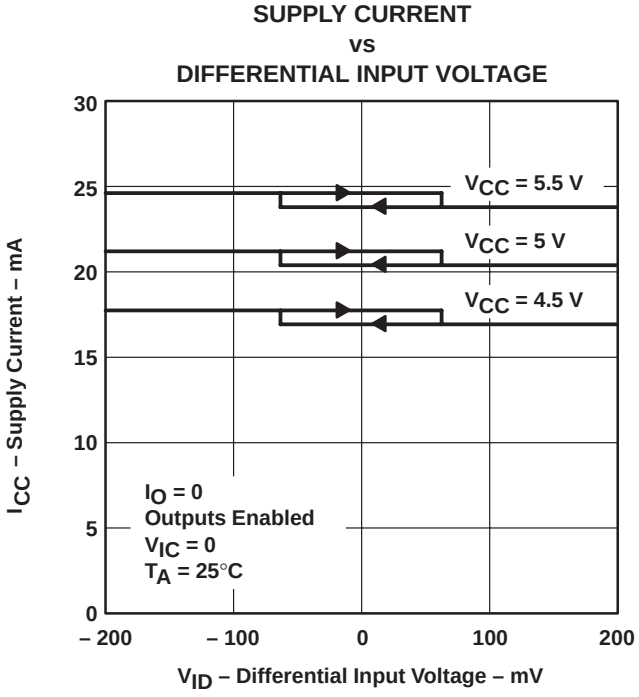


Figure 17

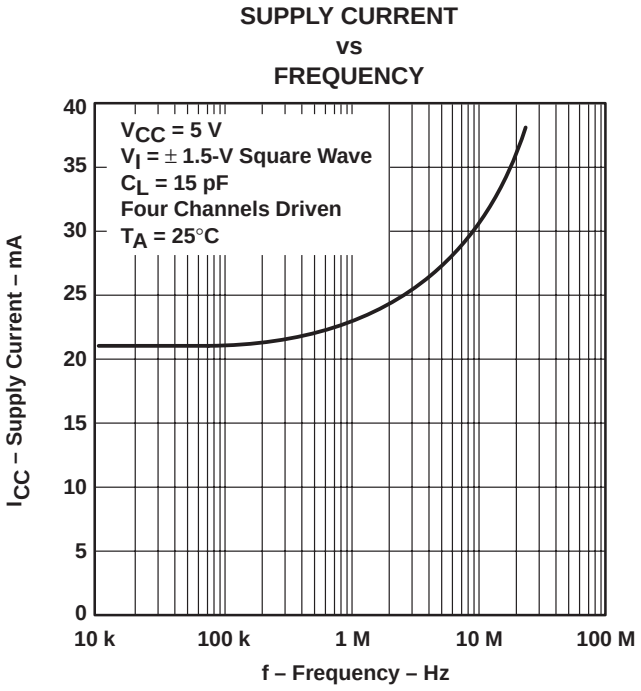


Figure 18

TYPICAL CHARACTERISTICS

INPUT RESISTANCE vs FREE-AIR TEMPERATURE

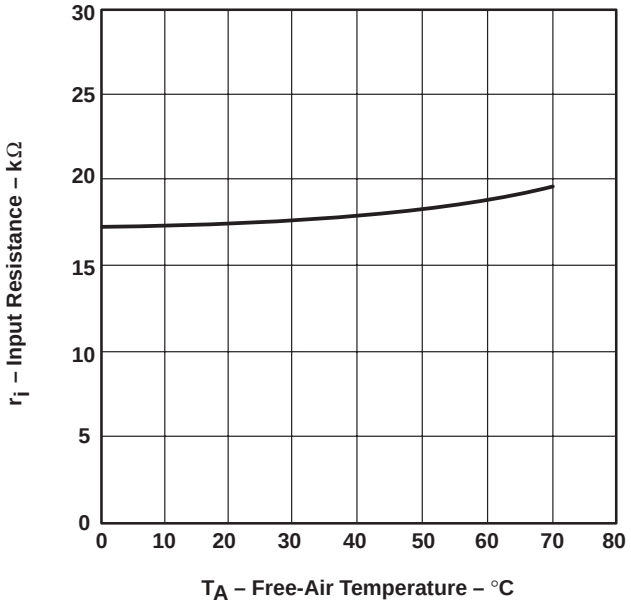


Figure 19

INPUT CURRENT vs INPUT VOLTAGE TO GND

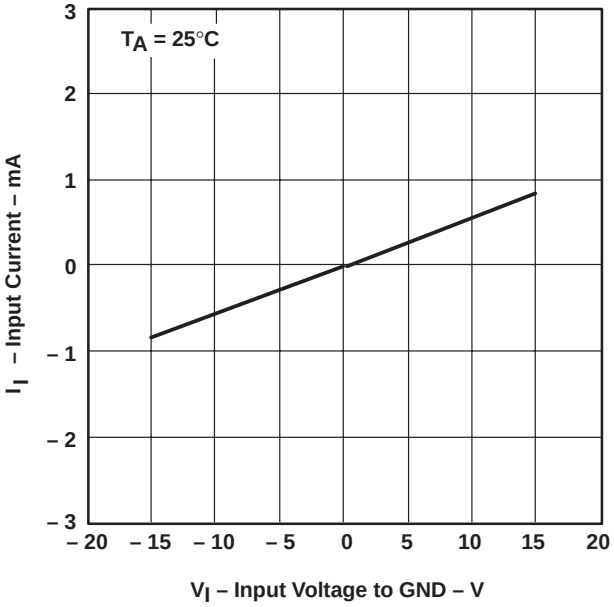


Figure 20

SWITCHING TIME vs FREE-AIR TEMPERATURE

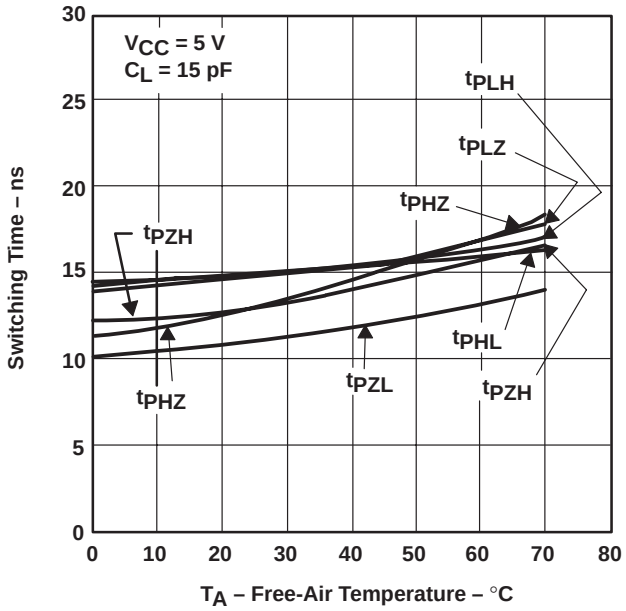


Figure 21

PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

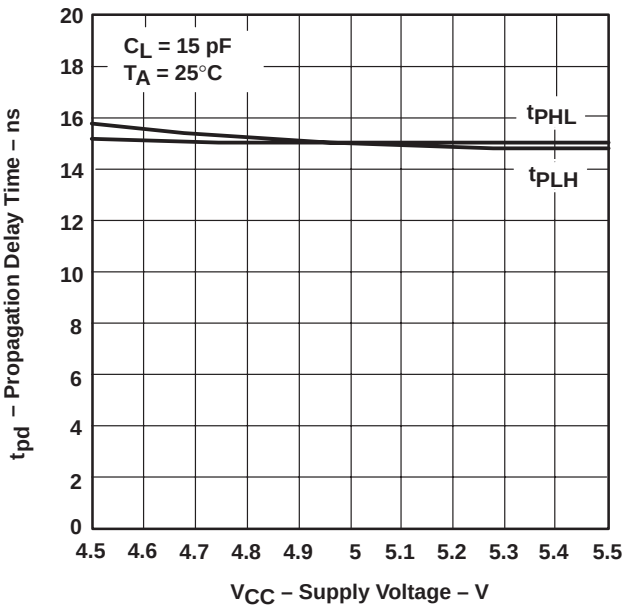


Figure 22

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN75ALS199D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS199DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS199DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS199DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS199N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75ALS199NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

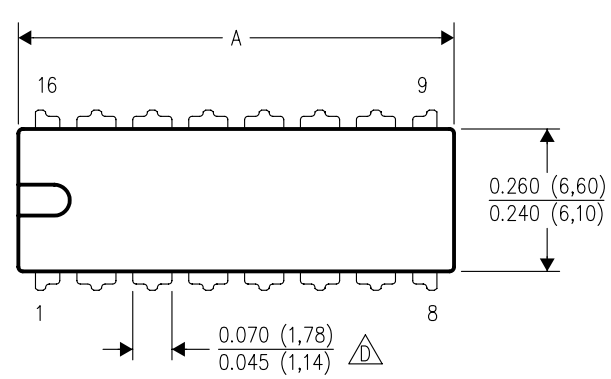
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

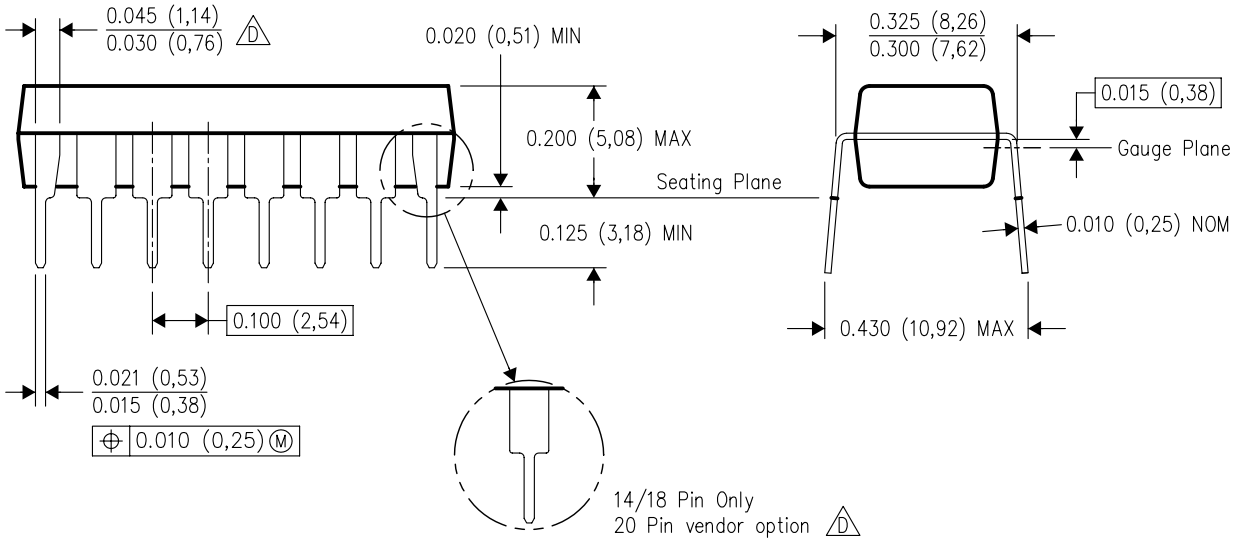
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



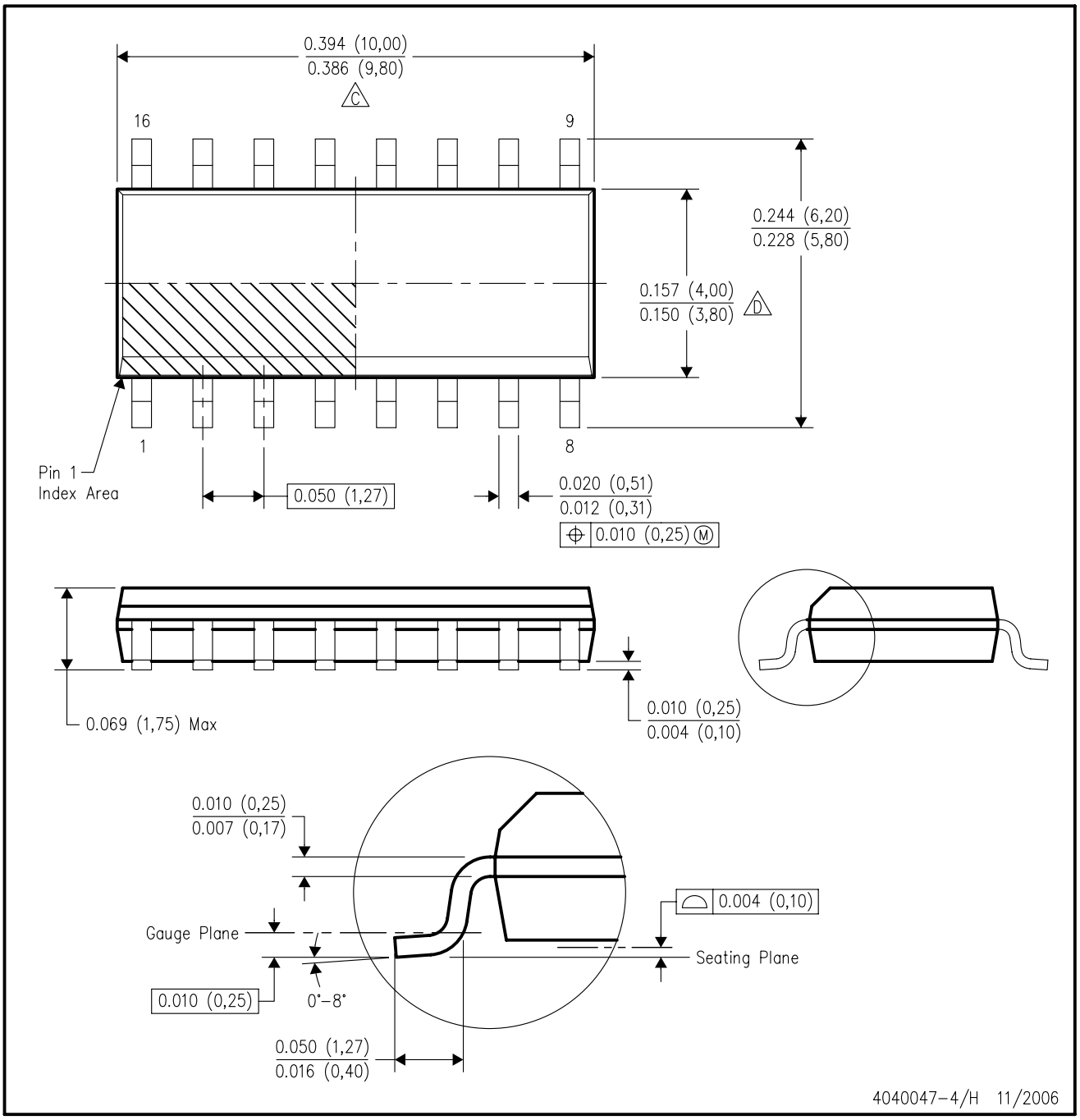
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

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