TMS320F240

DSP Controller

Silicon Errata

Silicon Revisions 1.1, 2.0, 3.1, 3.2, and 3.4

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Contents

1 Introduction

This document describes the known exceptions to the functional and emulation specifications for the TMS320F240†‡ DSP Controller. The exceptions to all released silicon revisions at the time of publication of this document are included. In addition, the changes made to each revision of silicon are summarized. In most cases, these changes are implemented to fix previously known exceptions. However, some of the changes are improvements or modifications that are not listed as exceptions to the functional or emulation specifications. The exceptions reported for a given revision are static, as of the release of the newest silicon revision. All exceptions reported thereafter will only be included in the section for that silicon release in which the exception was discovered. The reader is encouraged to review all sections of this document to obtain a complete understanding of all known exceptions.

1.1 Quality and Reliability Conditions

TMX Definition

Texas Instruments (TI) does not warranty either (1) electrical performance to specification, or (2) product reliability for products classified as “TMX.” By definition, the product has not completed data sheet verification or reliability performance qualification according to TI Quality Systems Specifications.

The mere fact that a “TMX” device is tested over a particular temperature and voltage ranges should not, in any way, be construed as a warranty of performance.

TMP Definition

TI does not warranty product reliability for products classified as “TMP.” By definition, the product has not completed reliability performance qualification according to TI Quality Systems Specifications; however, products are tested to a published electrical and mechanical specification.

TMS Definition

Fully-qualified production device.

Flash EEPROM

Reliability testing has been performed on other DSPs with flash which (by similarity of flash module) tends to suggest that both the TMP320F240PQ and the TMX320F240PQ should perform favorably to >10 cycles. However, flash write/erase endurance is not specified at this time.

Additionally, the TMS320F240 flash does not offer a “sector protection” feature. For further details, refer to the *Sector Protect Product Change Notice,* which is available at: **ftp://ftp.ti.com/pub/tms320bbs** on the DSP Internet BBS (Bulletin Board Service).

† Revisions 1.1, 2.0, and 3.1 are preproduction versions and will not be supported in production.
‡ See Section 5, *Silicon Revision List*, for a revision history of the TMS320F240PQ devices that have been released for sample and/or sale.

2 Summary of Changes Made Between Revisions

2.1 Improvements Made Between Revisions 1.1 and 2.0

The design changes made to the F240 from revision 1.1 to revision 2.0 focused on fixing known bugs. A summary of the bugs follows with a description of the corrected device behavior for revision 2.0 silicon.

SPISTE Pin Function

The SPI SPISTE pin will now force the SPISOMI output pin to the high-impedance state when the SPI is configured for slave mode and the SPISTE and SPISOMI pins are configured for use as serial port pins. This fixes the bug from revision 1.1, where the SPISTE pin had no effect on the SPISOMI pin.

Event Manager (EV) Capture FIFO

The Event Manager input capture units (CAP1 − CAP4) now perform correctly when the FIFO has two entries. Correct values can be read from the FIFO in this condition. (Note: a capture-status-bit-update bug remains in revision 2.0 silicon. See the advisory “EV CAPFIFO Status”, in Section 3, *Known Design Marginality/Exceptions to Functional Specifications*, for more details.)

XINT1 When V_{CCP} = 5 V

The External Interrupt 1 (XINT1) pin has been fixed so that it now recognizes external interrupt stimulus when V_{CCP} = 5 V.

Flash Inverse Erase

The Inverse Erase function of the flash EEPROM has been fixed. The Inverse Erase function can now be used on revision 2.0 silicon (and revision 2.0 of the flash programming utility) to identify and recover depleted bits.

EV Address Decode

The address decode problem for the event manager has been corrected. The event manager will decode addresses at 7400h−7434h, as defined. The data address ranges at F400h−F434h, F600h−F63Fh, FC00h−FC3Fh, and FE00h−FE3Fh are no longer decoded as valid event manager addresses.

EV Asymmetric PWM With Dead-Band

The dead-band generation for asymmetric PWM mode has been fixed to work correctly when the active PWM output pulse duration is less than the dead-band time. This feature now works as specified.

EV Forced PWM Function

The Event Manager PWM function has been corrected to allow the changing of PWM outputs from any forced condition (forced low or forced high) to active-low condition. This feature now works as specified.

Analog-to-Digital Converter (ADC) Control Register Bits, ADC2EN and ADC1EN

The ADC control register 1, ADCTRL1 at 0x07032, will no longer read incorrect values for bits 11 and 12, ADC2EN and ADC1EN, respectively. The bit positions have been corrected. These register bits now function as specified.

EV Scan Clocks

The Event Manager scan-based emulation clocks are now connected correctly. The Event Manager functions in emulation mode as specified.

ADC External Start of Convert Pin, ADCSOC

The external start of ADC conversion pin, ADCSOC, has been changed to detect rising edge transitions. A rising edge on ADCSOC will initiate an ADC start-of-conversion request.

CLKOUT/IOPC1 Power-On Reset State

The power-on reset condition of the CLKOUT/IOPC1 pin was changed from being an input to CPUCLK output. The state of the CLKSRC[1:0] bits in the system control register (SYSCR @ 0x7018) is now 11b.

EV GP Timer—Directional Up/Down and QEP Modes

The function of GP Timer 2 in directional-up/down mode, and GP Timers 2 and 3 in QEP mode, has been changed. The change has been incorporated in the new *TMS320C24x DSP Controllers Reference Set* (see Section 7, *Documentation Support*). The following is a summary of the change.

Before the change, for every GP Timer in directional-up/down and QEP modes:

1. The GP Timer will stop and hold at 0 when it counts down to 0 as long as the direction input is 0.
2. The GP Timer will stop and hold at 0ffffh when it counts up to 0ffffh as long as the direction input is 1.

After the change, for GP Timer 2 when it is in directional-up/down mode and for every GP Timer in QEP mode:

1. The GP Timer will roll over to 0ffffh and continue the count downward when it counts down to 0 as long as the direction input is 0.
2. The GP Timer will roll over to 0 and continue the count upward when it counts up to 0ffffh as long as the direction input is 1.

2.2 Improvements Made Between Revisions 2.0 and 3.1

The design changes made to the F240 from revision 2.0 to revision 3.1 focused on fixing known bugs. A summary of the bugs follows with a description of the corrected device performance for revision 3.1 silicon.

XINT2/3 Interrupt Enable

The XINT2 and XINT3 interrupt-enable circuitry can be overridden by setting the data direction bit (bit 4) in their respective control registers (XINT2CR at address 7078h and XINT3CR at address 707Ah). Setting this bit enables the digital output function of the pin and prevents the interrupt from occurring.

On revision 3.1 silicon, when the XINT2/3 inputs are enabled as interrupts, the interrupt path will be automatically enabled, regardless of the state of the direction (DIR) bit.

EV Forced PWM With Dead-Band Function

When the action register is changed from the FORCED HIGH or FORCED LOW state to either ACTIVE LOW or ACTIVE HIGH, AND the dead-band function is enabled, the PWM outputs do not come back on in the correct state.

On revision 3.1 silicon, the logic is modified so that the PWM outputs may be FORCED LOW or FORCED HIGH and then re-enabled for ACTIVE HIGH or ACTIVE LOW in the correct state.

EV CAPFIFO Status

The Event Manager Capture FIFO status bits (CAPxFIFO bits in CAPFIFO register) update incorrectly when a capture is generated at the same time a FIFO read is performed AND the CAPxFIFO status is 11b. The CAPxFIFO bits change from 11b to 01b, resulting in the loss of the second capture value.

On revision 3.1 silicon, the CAPxFIFO status will update to the correct value of 10b.

EV GP Timer 1 Synchronization With GP Timers 2/3

When the prescale value and the timer-enable bit are changed in the same cycle (T1CON), Timer 2 and Timer 3 will no longer begin counting one cycle ahead of Timer 1, when Timer 1 enables Timer 2 and Timer 3. The timer synchronization feature now works as specified.

SYSIVR Writes

Writing to the system interrupt vector register, SYSIVR, will no longer cause the internal ready signal to stay low, halting all processor activity (until a reset occurs). Writes to this register have no effect on the contents, and the processor will not be halted. Writes to this register now work as specified.

2.3 Improvements Made Between Revisions 3.1 and 3.2

Input V_{IH}/V_{IL} Levels

The input levels for the input pins meet the specifications for V_{IH} and V_{IL}.

EV Interrupt—Multiple Interrupts in One Group

Multiple interrupts in single Event Manager interrupt group (A, B, or C) now work as specified. The one-cycle condition where a read of the vector register and a higher priority interrupt event coinciding in the same cycle has been fixed.

NOTE: Revisions 3.2 and 3.4 are identical from a user perspective. There is no revision 3.3 silicon for F240.

3 Known Design Marginality/Exceptions to Functional Specifications

Table 1. Summary of Exceptions

Description	Revision(s) Affected	Page
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The first available silicon for F240 was revision 1.1. No previous revisions were released.

Advisory *SPISTE Pin Function*

Revision(s) Affected: 1.1

Details: The SPI SPISTE pin does not put the SPISOMI pin in the high-impedance state when the SPI is configured in slave mode. The state of the SPISTE pin has no effect on the SPISOMI pin.

Workaround: In slave mode, the SPI SPISOMI pin can be put into the high-impedance state in one of two ways. The first is to configure the SPISOMI pin as a digital input. This is done by clearing the SPISOMI function and DATA DIR bits (SPIPC2 register, bits 1 and 0). The second way to put the SPISOMI pin into the high-impedance state is by clearing the TALK bit (SPICTL register, bit 1).

A hardware workaround is to add a buffer to the SPISOMI output. The buffer should be enabled by the master SPI's slave select signal.

This will be fixed in rev 2.0.

Advisory *EV Capture FIFO*

Revision(s) Affected: 1.1

Details: The Event Manager input-capture units (CAP1 − CAP4) do not behave correctly when the FIFO has two entries. In this condition, incorrect values are read from the FIFO. The capture units will function correctly if only one value is allowed to reside in the FIFO.

Workaround: The capture FIFO must be read each time a value is captured. Either the capture status bits [CAP1FIFO, CAP2FIFO, CAP3FIFO, or CAP4FIFO (bits 8−9, 10−11, 12−13, and 14−15, respectively) in the Capture FIFO Status Register, CAPFIFO, at 7422h] or the capture interrupt flag bits [CAP1INT, CAP2INT, CAP3INT, or CAP4INT (bits 0, 1, 2, or 3, respectively) in the EV Interrupt Flag Register C, EVIFRC, at 7431h] can be read to determine when a capture event has occurred.

This will be fixed in rev 2.0.

Advisory *CLKOUT/IOPC1—SYSCLK Not Output*

Revision(s) Affected: 1.1

Details: The CLKOUT/IOPC1 pin does not output the SYSCLK as stated in the *TMS320C24x DSP Controller Reference Set* (see Section 7, *Documentation Support*). A 1-MHz clock is output when the CLKSRC[1:0] bits are set to 10b (SYSCR register, bits 6 and 7).

Workaround: This will be fixed in rev 2.0.

Advisory *XINT1 When V_{CCP} = 5 V*

Revision(s) Affected: 1.1

Details: External Interrupt 1 (XINT1) pin does not respond to external interrupt stimulus when V_{CCP} = 5 V.

Workaround: External interrupts 2 and 3 are the same as XINT1 with the addition that XINT2 and XINT3 are also capable of being configured as digital I/Os. These external interrupts should be used instead of XINT1 when V_{CCP} = 5 V. When V_{CCP} = 0 V, XINT1 functions normally.

This will be fixed in rev 2.0.

Advisory *Flash Inverse Erase*

Revision(s) Affected: 1.1

Details: The Inverse Erase function does not work. The Inverse Erase function is used to identify and recover depleted bits. This may result in unreliable Erase/Clear sequences after a device is cycled through a few (1−3) Clear/Erase/Program sequences.

Workaround: None at present.

This will be fixed in rev 2.0.

Advisory *EV Address Decode*

Revision(s) Affected: 1.1

Details: The address decode for the event manager is implemented incorrectly. The event manager will decode addresses at 7400h−7434h, as designed, but will also decode addresses at F400h−F434h, F600h−F63Fh, FC00h−FC3Fh, and FE00h−FE3Fh as valid event manager addresses.

Workaround: The workaround is to avoid external data space accesses in these ranges. No other workaround is available.

This will be fixed in rev 2.0.

Advisory *EV Asymmetric PWM With Dead-Band*

Revision(s) Affected: 1.1

Details: The dead-band generation for asymmetric PWM mode does not work correctly when the active PWM output pulse duration is less than the dead-band time.

Workaround: If this mode must be used, the user will have to make the active PWM output pulse duration zero by setting the compare register greater than the period register when the active PWM output pulse duration is less than the dead-band time.

This will be fixed in rev 2.0.

Advisory *ADC Control Register Bits, ADC2EN and ADC1EN*

Revision(s) Affected: 1.1

Details: The ADC control register 1, ADCTRL1 at 0x07032, will read incorrect values for bits 11 and 12 (ADC2EN and ADC1EN, respectively). The value will be incorrect in that bit 11 is read out as bit 12, and bit 12 is read as bit 11. This problem does not affect correct operation of either conversion.

Workaround: One possible workaround is to define separate bit masks for reads and writes to ADC control register 1.

```
ADCTRL1         .set    7032h           ;Address for ADC control register 1
ADC2EN_TST      .set    0003h           ;Bit Code for testing bit 12, ADC2EN
ADC1EN_TST      .set    0004h           ;Bit Code for testing bit 11, ADC1EN
ADC1EN_MSK      .set    1000h           ;Bit Mask for setting bit 12, ADC1EN
ADC2EN_MSK      .set    0800h           ;Bit Mask for setting bit 11, ADC2EN
                :
                :
LDP             #(ADCTRL1/80h)          ;change data page pointer to correct page
LACL            ADCTRL1                 ;read ADC control register 1
OR              #ADC1EN_MSK             ;enable ADC1
SACL            ADCTRL1                 ;store new value to ADC control register 1
                :
                :
LDP             #(ADCTRL1/80h)          ;change data page pointer to correct page
BIT             ADCTRL1,ADC1EN_TST      ;test for ADC1EN bit set
                :
                :
```

This will be fixed in rev 2.0.

Advisory *XINT2/3 Interrupt Enable*

Revision(s) Affected: 1.1, 2.0

Details: The XINT2 and XINT3 interrupt-enable circuitry can be overridden by setting the data direction bit (bit 4) in their respective control registers (XINT2CR at address 7078h and XINT3CR at address 707Ah). Setting this bit enables the digital output function of the pin and prevents the interrupt from occurring.

Workaround: The workaround is to clear the data direction bit at the same time the interrupt-enable bit is set.

This will be fixed in rev 3.1.

Advisory *EV CAPFIFO Status*

Revision(s) Affected: 1.1, 2.0

Details: The Event Manager capture FIFO status bits (CAPxFIFO bits in CAPFIFO register) update incorrectly when a capture is generated at the same time a FIFO read is performed AND the CAPxFIFO status is 11b. The CAPxFIFO bits change from 11b to 01b, resulting in the loss of the second capture value.

Workaround: The capture FIFO must be read each time a value is captured. Either the capture status bits [CAP1FIFO, CAP2FIFO, CAP3FIFO, or CAP4FIFO (bits 8−9, 10−11, 12−13, and 14−15, respectively) in the Capture FIFO Status Register, CAPFIFO, at 7422h] or the capture interrupt flag bits [CAP1INT, CAP2INT, CAP3INT, or CAP4INT (bits 0, 1, 2, or 3, respectively) in the EV Interrupt Flag Register C, EVIFRC, at 7431h] can be read to determine when a capture event has occurred.

This will be fixed in rev 3.1.

Advisory *Input V_{IH}/V_{IL} Levels*

Revision(s) Affected: 1.1, 2.0, 3.1

Details: The input levels for the input pins do not meet the specification for V_{IH} and V_{IL}.

Workaround: The device functions correctly when the input levels are relaxed. For revision 3.1 silicon, the correct levels are as follows:

V_{IH} min: 2.8 V
V_{IL} max: 1.25 V

This will be fixed in rev 3.2.

Advisory *EV Interrupt—Multiple Interrupts in One Group*

Revision(s) Affected: 1.1, 2.0, 3.1

Details:

This bug is in all silicon revisions prior to and including revision 3.1. A hardware design modification has been identified. This design modification will be included in the production release of the F240 − most likely, revision 3.2. This version is planned for availability in June 1998.

Reading the vector register, except in response to an interrupt event, can cause a future interrupt event to be missed. The user must not read the vector register except in response to an interrupt. The future interrupt event will only be missed if the event and the vector register read occur in the same cycle AND no flags are set in the interrupt flag register.

The bug description is as follows:

The higher-priority EVIFRx bit will be cleared when the higher-priority event occurs in the same cycle that the EVIVRx register is read for a previously received lower-priority event. When this vector is used as part of the ISR branch address, the wrong vector will be used as the offset into the peripheral interrupt vector branch table. The result is that the higher-priority interrupt will NOT be serviced and the lower-priority interrupt will be serviced twice.

This occurs because the vector read automatically clears the highest-priority flag, but there is a one-cycle delay between the flag being set and the register updated with the new vector. This one cycle happens when a higher-priority event occurs in the same cycle as the vector read.

However, skipping the vector read does not avoid the problem, since the vector must be read before any additional pending interrupt requests are sent to the CPU.

Workaround:

Case 1. Only one interrupt is enabled in a single EV group (e.g., TCINT1 in EV group A). The bug condition cannot happen in this case, no workaround is required.

Case 2. Only two interrupts are enabled in a single EV group (e.g., TCINT2 and TCINT3 in EV group B).

The software workaround is as follows:

1. Read the vector register and save.
2. Read the flag register and save.
3. Branch to the ISR corresponding to the vector saved in step 1. Branch table must check for lower-priority vector first.
4. In lower-priority ISR, check if the flag bit (saved in step 2) is set. (In normal operation, the flag bit corresponding to the vector read is cleared). If set, skip lower-priority ISR and branch to higher-priority ISR. If cleared, service lower priority as normal.
5. In higher-priority ISR, no checking of the flag is necessary. Either its vector was read correctly and the code branched here directly, −OR− its flag was cleared in error as a result of the bug, and the lower-priority ISR code caught the error and branched here.

A code example for EV group B interrupt service routine with Timer 2 and Timer 3 compare interrupts enabled follows:

```
GISR2       ; put context save code here, before changing any machine state.
            ; Software workaround
            LDP     #DP_EV      ; change dp for EV control regs
RDVEC       LACL    EVIVRB      ; read IVRB to clear one flag (any flag)
            LDP     #0          ; change data page for B2 DARAM
            SACL    IVRB_TEMP   ; save valid flags to B2 DARAM
            LDP     #DP_EV      ; change dp for EV control regs
            LACL    EVIFRB      ;read IFRB, one flag should have been cleared
            LDP     #0          ; change data page for B2 DARAM
            SACL    IFRB_TEMP   ; save valid flag to B2 DARAM
CHK_VEC     ; Now compare the vector and branch to ISR
                    ; In this case, only T2 and T3 Compare interrupts are enabled
                    ; so the vector testing and branch is optimized for this case.
            LACL    IVRB_TEMP   ; ACC = vector
            XOR     #TCINT3_VEC
            BCND    TCINT3_ISR,EQ
            B       TCINT2_ISR
TCINT3_ISR:
            LACL    IFRB_TEMP
            XOR     #TCINT3_FLAG
            BCND    TCINT2_ISR,EQ
            ; continue with TCINT3 ISR if flag cleared.
            ; Don't forget to restore context and re-enable interrupts before returning.
```

Case 3. Three or more asynchronous interrupts are enabled in a single EV group (e.g., TCINT1, CMP1INT, and PDPINT in EV group A).

With three interrupts enabled, there is no way to detect which higher-priority interrupt flag bit gets cleared in error, IF that higher-priority interrupt happens to coincide with a vector read for the lowest-priority interrupt service. In this case, the lower-priority vector will be read, and the lower-priority flag bit will be set. In the worst case, only one of the higher-priority interrupts occurred in the same cycle as the vector read and the other higher-priority interrupt is inactive during this time. In this case, only the lowest-priority bit is set and the higher-priority event is lost.

A workaround for this case is only applicable if the two lowest-priority interrupts (TCINT1 and CMP1INT) are programmed such that one never coincides with the read of the other. In this case, the workaround for Case 2 is applicable, with minor modifications.

Advisory *EV Forced PWM With Dead-Band Function*

Revision(s) Affected: 1.1, 2.0, 3.1, 3.2, 3.4

Details: Event Manager (EV) of the TMS320F240 does not allow changes to the PWM outputs from any forced condition (forced low or forced high) to active-low condition. All outputs come back to active-high condition regardless of the action control register (ACTR) setting. This problem exists only when the dead-band function is activated. Without dead-band, the ACTR register controls the PWM output signal polarity as defined in the user's guide (see Section 7, *Documentation Support*).

An example of the error condition is as follows:

If the user forces PMW1 and PWM2 to a forced-low condition by writing to the ACTR register and then wants to come back to the active-high condition for PWM1 and the active-low condition for PWM2 with appropriate dead-band, F240 will bring both PWMs to the active-high condition, and the user will not have the desired complementary PWM signals.

Workaround: One possible workaround is to shut off all compare functions and then restart the PWM function. This will reset all internal circuits and the F240 will restart PWM operation as a new command. However, before restarting the PWM function, all PWM outputs have to be forced low. This is needed to avoid any shoot-through (no dead-band between complementary PWM signals) fault.

```
LDP     #DP_EV
SPLK    #1100101101010111b,  COMCO      ; COMCON for immediate load of ACTR
SPLK    #0000000000000000b,  ACTR       ; Forces all PWM channels to zero.
SPLK    #1100001101010111b,  COMCON     ; Configures COMCON loading in UF
SPLK    #0000011001100000b,  ACTR       ; Configures ACTR for proper polarities
SPLK    #0100001101010111b,  COMCON     ; Reload COMCON
SPLK    #1100001101010111b,  COMCON
```

Advisory *Clock-In Frequency Bits (CKINF), CKINF[3:0] in CKCR1, Stay at 1111b Until Power-On Reset*

Revision(s) Affected: 1.1, 2.0, 3.1, 3.2, 3.4

Details: The clock input frequency bits, when set to 1111b, may not be modified by software and are reset only by a power-on reset. All other bit combinations are reconfigurable by user software.

Workaround: Once written to 1111b state, the CKINF[3:0] bits can only be changed by a power-on reset, which clears the CKINF[3:0] bits to 0000b. The CKINF bits are used to indicate the frequency of the clock signal applied at the CLKIN/XTAL1 pin. This value should be constant for a given system. Under normal use conditions, the user should not change the state of the CKINF bits.

No fix is currently planned since changing the status of the CKINF bits in not recommended.

Advisory *SCI Address Mode*

Revision(s) Affected: 1.1, 2.0, 3.1, 3.2, 3.4

Details: The TXWAKE bit is not shadowed correctly by the WUT bit as described in the SCI chapter of the C240 reference set (section Address-Bit Multiprocessor Mode). When the SCI is configured in Address-Bit mode, any write to the SCITXBUF causes the TXWAKE bit to be transferred to the WUT bit. The incorrect value for the address bit will be transmitted under the following conditions:

1. A data-byte transmission is in progress (TXWAKE=0 and SCITXBUF="data value").
2. An address byte is queued (TXRDY=1, TXEMPTY=0, and the user writes TXWAKE=1, then SCITXBUF="address value").

In this case, the address bit in the data-byte transmission sequence will be set to 1. The correct value is 0.

Workaround: The user software should poll the TXEMPTY bit before setting up an address-byte transmission sequence. This will indicate the previous data-byte transmission is completed, and therefore, setting TXWAKE=1 will not cause the address bit to be set in the data byte-transmission sequence.

No fix is currently planned.

4 Known Exceptions to Emulation Specifications

4.1 Silicon Revision 1.1

Advisory	*EV Scan Clocks*

Revision(s) Affected: 1.1

Details: The Event Manager scan clocks are not connected correctly. This results in the Event Manager registers not being set to zero on power up or reset by the debugger. Any update by the debugger to these registers will corrupt the value in these registers.

Workaround(s):

1. Do not view any of the Event Manager registers using the debugger. Windows to avoid are the Watch and Memory windows.
2. Use the “runf” command instead of the “run” command. The “runf” command disconnects the emulator and allows the device to run under functional clocks.
3. Execute the following code to initialize the Event Manager registers when using the debugger:

```
* Initialize key EV registers to their reset state of zero.
        LDP  #232               ; DP = 7400/80h = 232
        ZAC
        SACL GPTCON
        SACL T1CNT
        SACL T1CON
        SACL T2CNT
        SACL T2CON
        SACL T3CNT
        SACL T3CON
        SACL COMCON
        SACL ACTR
        SACL SACTR
        SACL DBTCON
        SACL CAPCON
        SACL CAPFIFO
        SACL IMRA
        SACL IMRB
        SACL IMRC
        LACC #0FFFFh            ; write ones to IFR regs to clear
        SACL IFRA
        SACL IFRB
        SACL IFRC
```

This will be fixed in rev 2.0.

4.2 TMS320C2xx Debugger v1.00.01

Advisory *Watchdog Counter Clock in STEP or RUN/BREAK Mode*

Details: Watchdog counter clocks are not halted by the debugger during STEP mode. During debugger update periods, the watchdog clock continues to run, causing watchdog resets.

Workaround: The watchdog timer should be disabled when using the emulator. The watchdog counter is disabled by setting the V_{CCP} pin high, and executing the following code immediately after reset. This will disable the watchdog timer counter. Program breakpoints should be set after the following code has executed.

```
* Set Data Page pointer to page 1 of the peripheral frame
        LDP     #DP_PF1             ; Page DP_PF1 includes WET through
                                    ; EINT frames
* initialize WDT registers
        SPLK    #06Fh, WDTCR        ; clear WDFLAG, Disable WDT, set WDT for 1
*                                   ; second overflow.
```

This will be fixed in a future release of the C2xx C-Source Debugger.

Advisory *Memory Add Command—"RAM" Keyword*

Details: The use of the "RAM" keyword in a "memory add debugger" command will result in illegal address resets when issuing a "run" command after a break point. The use of the "RAM" keyword is only a problem when defining peripheral registers in data space. The illegal address reset condition occurs when a peripheral register has been added to the "Watch" window.

Workaround: Change the "memory add" keyword from type "RAM" to type "IOPORT". This fixes the illegal reset condition. The exact syntax to use is as follows:

```
good:  ma 0x07090,1,0x0010,ioport     ;Peripheral − Digital I/O
 bad:  ma 0x07090,1,0x0010,ram        ;Peripheral − Digital I/O
```

This will be fixed in a future release of the C2xx C-Source Debugger.

Advisory	*Watch/Memory Window Updates Can Clear Flag Bits*

Details: This section describes a feature of the debugger that users need to be aware of when debugging code on the C240/F240. Normal operation of the debugger can modify the state of some peripheral registers. This occurs when the debugger updates the contents of peripheral registers that are displayed in either the watch or memory window. These debugger “reads” will cause certain registers and status/flag bits to be reset. Specifically, the four interrupt vector registers (SYSIVR, EVIVRA, EVIVRB, and EVIVRC) and the ADC and EV Capture FIFO registers (ADCFIFO1, ADCFIFO2, CAP1FIFO, CAP2FIFO, CAP3FIFO, and CAP4FIFO) will be cleared by debugger reads. In addition, the status/flag bits associated with these registers will also be modified accordingly. This condition will occur when the debugger is used in the RUN/STOP mode by single stepping through code or hitting a breakpoint. If the stop action, and therefore the memory/watch window update, happens between a key event, such as an interrupt or data loaded into one of the FIFO registers, the debugger read will cause the state of these registers and their respective status/flag bits to be changed per normal operation.

Workaround: The solution is to refrain from viewing the register addresses in either the watch or memory windows. The value contained in the register should be read by user code while the processor is running, then saved to a location in RAM which can then be viewed using either the watch or the memory window.

5 Silicon Revision List

The following table lists the revision history of the TMS320F240PQ devices that have been released for sample and/or sale.

Revision	Class
1.1	TMX
2.0	TMX or TMP
3.1	TMP
3.2	TMP or TMS
3.4	TMS

6 Programming Considerations for the F240

6.1 Cascaded Timer Operation

When timers 2 and 3 are used as a 32-bit cascaded timer, the following facts should be considered:

- On reaching the 32-bit period value, the cascaded timer stops counting (i.e., saturates), and can only be restarted by changing the state of the TMRDIR pin. The timer then counts in the other direction. When counting down, the 32-bit counter counts down to zero, where it stops again until the TMRDIR pin is toggled again.
- The timer counter registers are not shadowed. For this reason, it is not possible to read the 32-bit counter value at a given instant of time (since the counters are always running, the content of one counter changes when the other counter is being read). The timers have to be stopped in order to read the counter values.

These limitations of the cascaded timer feature must be considered in user applications.

7 Documentation Support

For device-specific data sheets and related documentation, visit the TI web site at: **http://www.ti.com**

To access documentation on the web site:

1. Go to **http://www.ti.com**
2. Open the "**Products**" dialog box and select "**Digital Signal Processors**"
3. Scroll to **"C24X™ DSP Generation"** and click on **DEVICE INFORMATION**
4. Click on a device name and then click on the documentation type you prefer.

For further information regarding the TMS320F240PQ, please refer to the following publications:

- *TMS320F/C24x DSP Controllers Reference Guide: CPU and Instruction Set,* literature number SPRU160
- *TMS320F/C24x DSP Controllers Reference Guide: Peripheral Library and Specific Devices,* literature number SPRU161

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