LOW INPUT VOLTAGE, DUAL LOAD SWITCH WITH CONTROLLED TURN-ON

Check for Samples: TPS22960

FEATURES

- **Integrated Dual Load Switch**
- **Input Voltage Range: 1.62 V to 5.5 V**
- **Low ON-State Resistance**
  - **r_{ON} = 342 mΩ at V_{IN} = 5.5 V**
  - **r_{ON} = 435 mΩ at V_{IN} = 3.3 V**
  - **r_{ON} = 523 mΩ at V_{IN} = 2.5 V**
  - **r_{ON} = 737 mΩ at V_{IN} = 1.8 V**
- **500-mA Maximum Continuous Switch Current**
- **Low Quiescent Current and Shutdown Current**
- **Controlled Switch Output Rise Time: 75 µs or 660 µs**
- **Integrated Quick Output Discharge Transistor**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **8-Pin SOT (DCN) Package: 3 mm × 3 mm**
- **8-Pin µQFN (RSE) Package: 1.5 mm × 1.5 mm**

APPLICATIONS

- **GPS Devices**
- **Cell Phones/PDAs**
- **MP3 Players**
- **Digital Cameras**

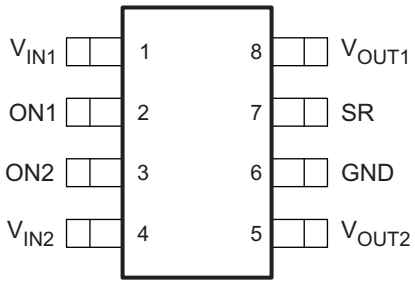
DESCRIPTION

The TPS22960 is a small low-r_{ON} dual load switch with controlled turn on. The devices contain two P-channel MOSFETs that can operate over an input voltage range of 1.62 V to 5.5 V. Each switch is controlled by an on/off input (ON1 and ON2), which is capable of interfacing directly with low-voltage control signals. In TPS22960 a 85-Ω on-chip load resistor is added for output quick discharge when switch is turned off.

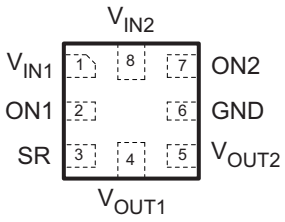
The rise time (slew-rate) of the device is internally controlled in order to avoid inrush current and can be slowed down if needed using the SR pin: TPS22960 features a 75 µs rise time with the SR pin tied to ground and 660 µs with the SR pin tied to high.

The TPS22960 is available in a space-saving 8-pin µQFN package and in an 8-pin SOT package. It is characterized for operation over the free-air temperature range of –40°C to 85°C.

DCN PACKAGE
(TOP VIEW)



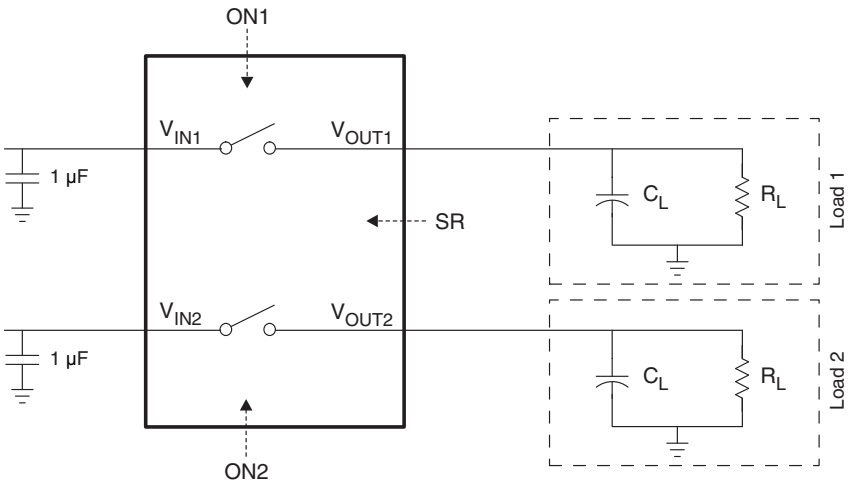
RSE PACKAGE
(TOP VIEW)



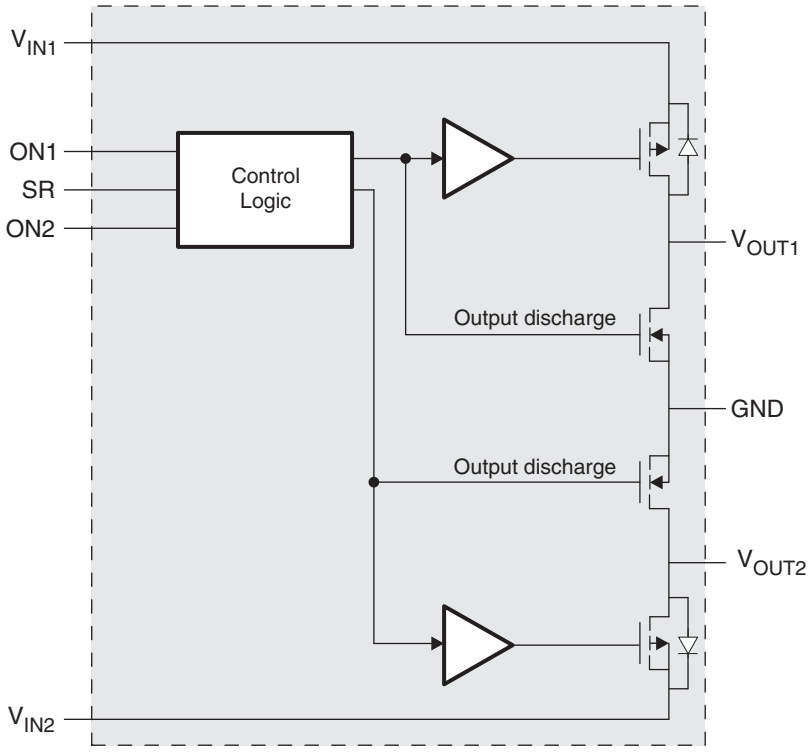
DEVICE	r_{ON} AT 3.3 V (TYP)	SLEW RATE AT 3.3 V (TYP)	QUICK OUTPUT DISCHARGE(1)	MAX OUTPUT CURRENT	ENABLE
TPS22960	435 mΩ	75 µs with SR = low 660 µs with SR = high	Yes	500 mA	Active High

(1) This feature discharges the output of the switch to ground through a 85-Ω resistor, preventing the output from floating.

TYPICAL APPLICATION



APPLICATION BLOCK DIAGRAM



CONFIGURABLE LOGIC FUNCTION TABLE

ONx	V_{INx} TO V_{OUTx}	V_{OUTx} TO GND
L	OFF	ON
H	ON	OFF

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
DCN PIN NO.	RSE PIN NO.	NAME	
1	1	V_{IN1}	Switch 1 input; bypass this input with a ceramic capacitor to GND
2	2	ON1	Switch 1 control input, active high. Do not leave floating.
3	7	ON2	Switch 2 control input, active high. Do not leave floating.
4	8	V_{IN2}	Switch 2 input; bypass this input with a ceramic capacitor to GND
5	5	V_{OUT2}	Switch 2 output
6	6	GND	Ground
7	3	SR	Slew rate control pin. SR = GND translates into a 75-µs rise time; SR = high translates into a 660-µs rise time
8	4	V_{OUT1}	Switch 1 output

ABSOLUTE MAXIMUM RATINGS(1)

			MIN	MAX	UNIT
V_{IN}	Input voltage range		–0.3	6	V
V_{OUT}	Output voltage range			V_{IN} + 0.3	V
V_{ON}	Input voltage range		–0.3	6	V
I_{MAX}	Maximum continuous switch current			0.5	A
T_A	Operating free-air temperature range		–40	85	°C
T_J	Maximum junction temperature			125	°C
T_{stg}	Storage temperature range		–65	150	°C
ESD	Electrostatic discharge protection	Human-Body Model (HBM)		2000	V
		Charged-Device Model (CDM)		1000	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

BOARD	PACKAGE	RθJC	RθJA	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le 25°C$	T_A = 70°C	T_A = 85°C
High-K(1)	DCN	123°C/W	220°C/W	-4.545 mW/°C	454.5 mW	250 mW	181.1 mW
High-K(1)	RSE	60°C/W	116°C/W	-8.621 mW/°C	862.1 mW	474.1 mW	344.8 mW

(1) The JEDEC High-K (2s2p) board used to derive this data was a 3 × 3 inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{IN}	Input voltage range		1.62	5.5	V
V_{OUT}	Output voltage range			V_{IN}	V
V_{IH}	High-level input voltage: ON1, ON2, SR	V_{INx} = 3.0 V to 5.5 V	1.5	5.5	V
		V_{INx} = 1.62 V to 3.0 V	1.4	5.5	
V_{IL}	Low-level input voltage: ON1, ON2, SR	V_{INx} = 3.0 V to 5.5 V		0.5	V
		V_{INx} = 1.62 V to 3.0 V		0.4	
C_{IN}	Input capacitor		1(1)		µF

(1) See Application Information

ELECTRICAL CHARACTERISTICS

V_{IN} = 1.62 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP(1)	MAX	UNIT
I_{IN}	Quiescent current (each switch)	I_{OUTx} = 0, V_{INx} = V_{ON}	V_{INx} = 5.5 V	Full		0.64	2	µA
			V_{INx} = 3.3 V	Full		0.35	1.2	
			V_{INx} = 2.5 V	Full		0.24	0.8	
			V_{INx} = 1.8 V	Full		0.15	0.5	
$I_{IN(OFF)}$	OFF-state supply current (each switch)	V_{ON} = GND, V_{OUTx} = Open	V_{INx} = 5.5 V	Full		0.47	3.6	µA
			V_{INx} = 3.3 V	Full		0.25	1.8	
			V_{INx} = 2.5 V	Full		0.18	1.3	
			V_{INx} = 1.8 V	Full		0.11	0.9	
r_{ON}	ON-state resistance (each switch)	I_{OUT} = –200 mA	V_{INx} = 5.5 V	25°C		342	400	mΩ
				Full			465	
			V_{INx} = 3.3 V	25°C		435	500	
				Full			595	
			V_{INx} = 2.5 V	25°C		523	620	
				Full			720	
			V_{INx} = 1.8 V	25°C		737	1100	
				Full			1300	
			V_{INx} = 1.62 V	25°C		848	1300	
				Full			1500	
r_{PD}	Output pulldown resistance	V_{IN} = 3.3 V, V_{ON} = 0, I_{OUT} = 30 mA		25°C		85	120	Ω
I_{ON}	ON-state input leakage current	V_{ON} = 1.62 V to 5.5 V or GND		Full			0.25	µA

(1) Typical values are at T_A = 25°C.

SWITCHING CHARACTERISTICS

V_{IN} = 3.3 V, T_A = 25°C, RL_CHIP = 85 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{ON}	Turn-ON time	R_L = 33 Ω, C_L = 0.1 µF	SR = V_{IN}		635		µs
			SR = GND		67		
t_{OFF}	Turn-OFF time	R_L = 33 Ω, C_L = 0.1 µF	SR = V_{IN}		4.5		µs
			SR = GND		4.2		
t_r	V_{OUT} rise time	R_L = 33 Ω, C_L = 0.1 µF	SR = V_{IN}		660		µs
			SR = GND		75		
t_f	V_{OUT} fall time	R_L = 33 Ω, C_L = 0.1 µF	SR = V_{IN}		4.5		µs
			SR = GND		4.5		

(1) Typical values are at the specified V_{IN} = 3.3 V and T_A = 25°C

TYPICAL CHARACTERISTICS

ON RESISTANCE
vs
INPUT VOLTAGE

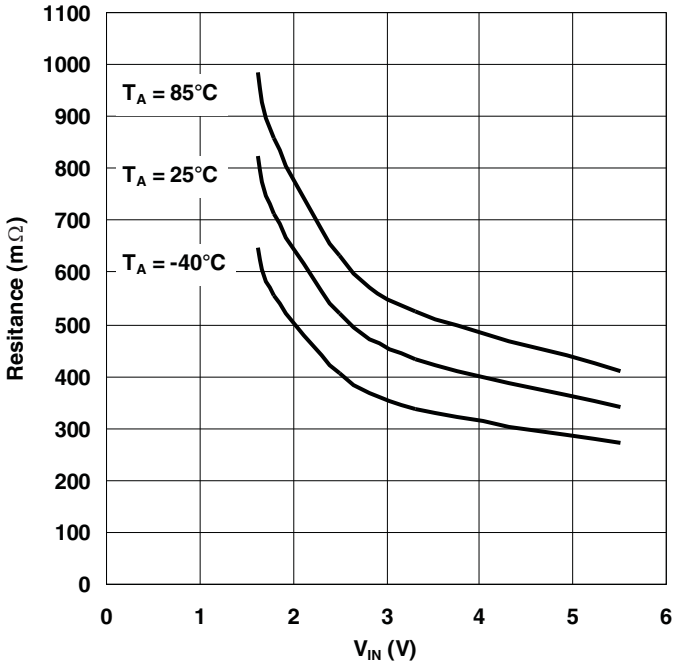


Figure 1.

ON RESISTANCE
vs
TEMPERATURE

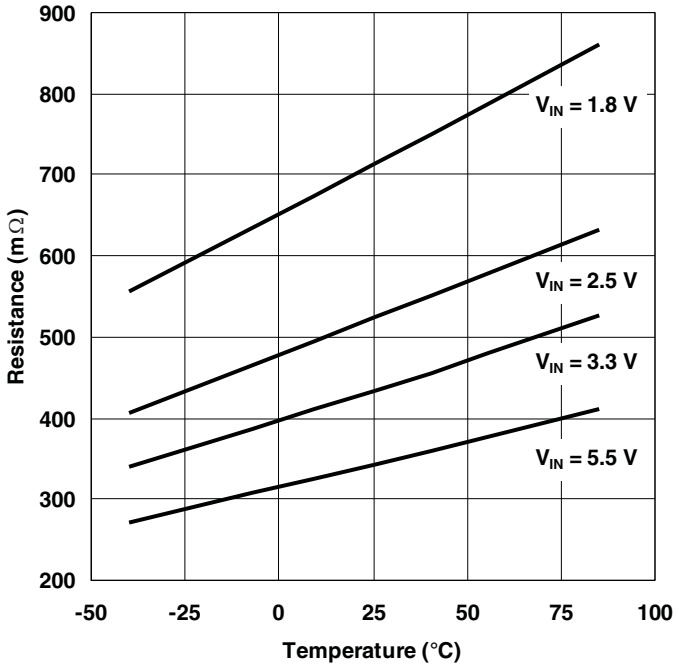


Figure 2.

QUIESCENT CURRENT
vs
TEMPERATURE

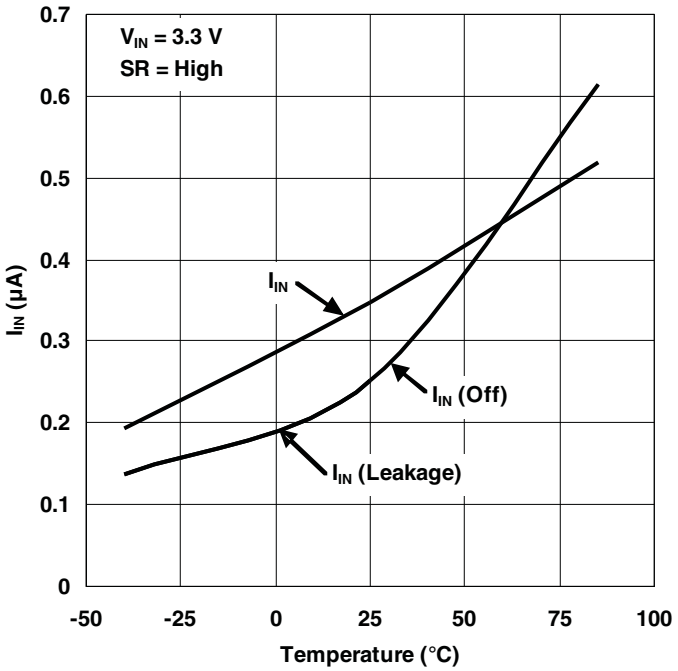


Figure 3.

QUIESCENT CURRENT
vs
INPUT VOLTAGE

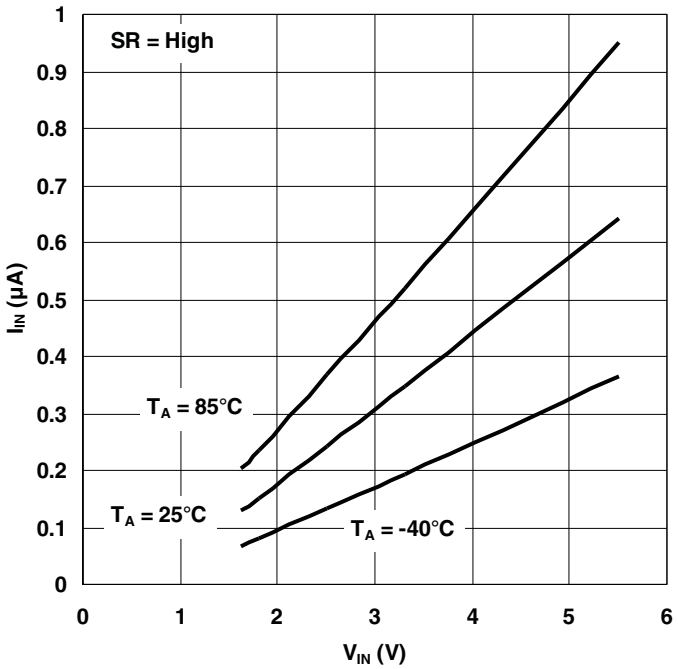


Figure 4.

TYPICAL CHARACTERISTICS (continued)

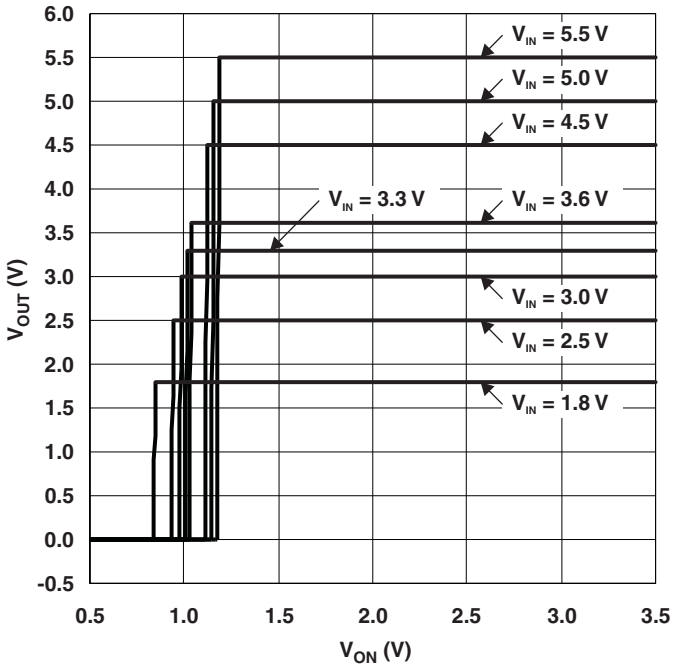
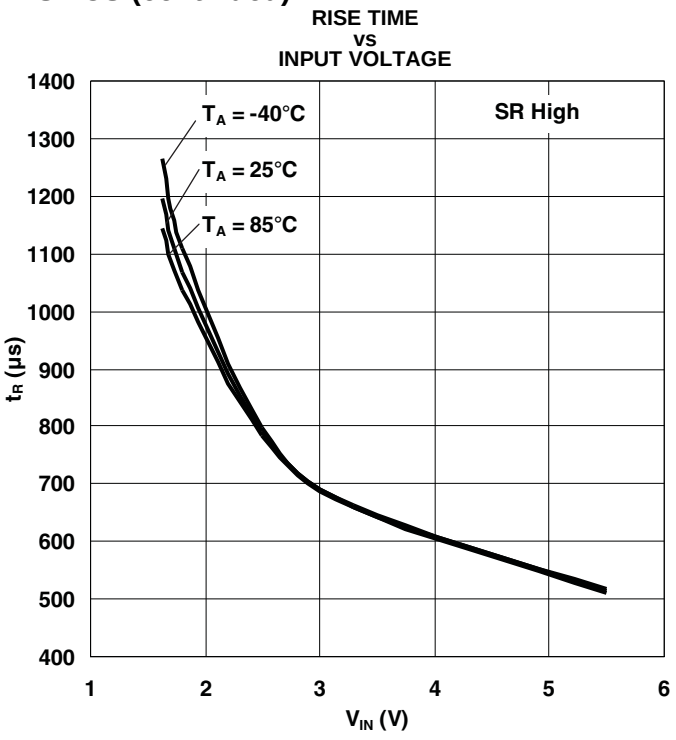


Figure 5.



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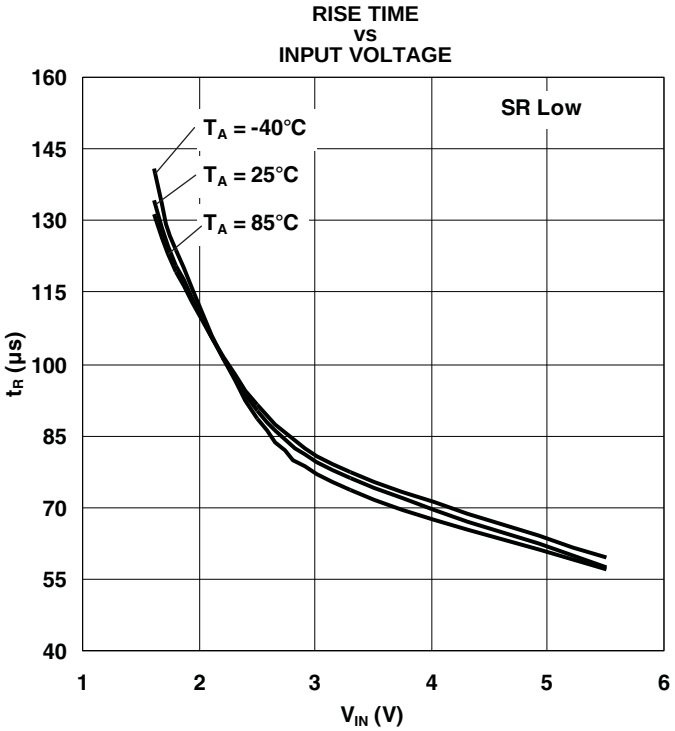

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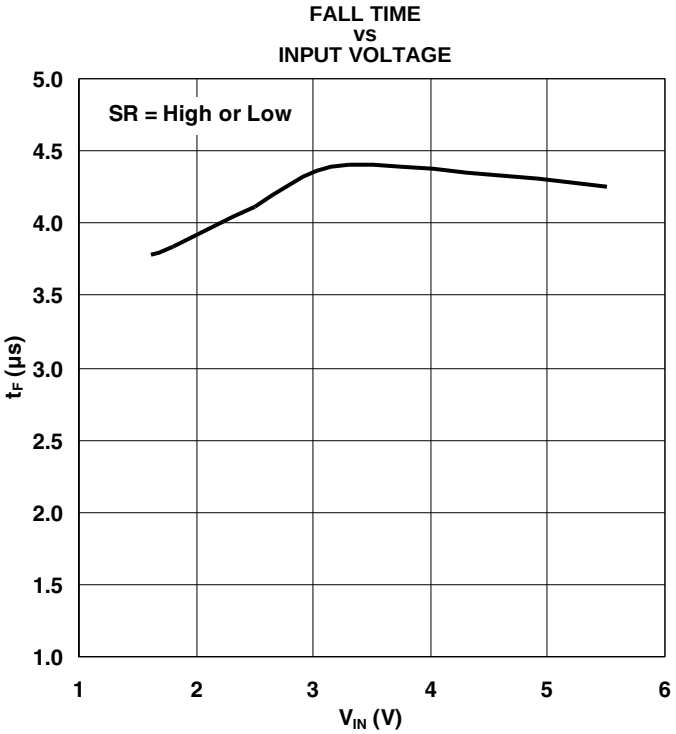


Figure 8.

TYPICAL CHARACTERISTICS (continued)

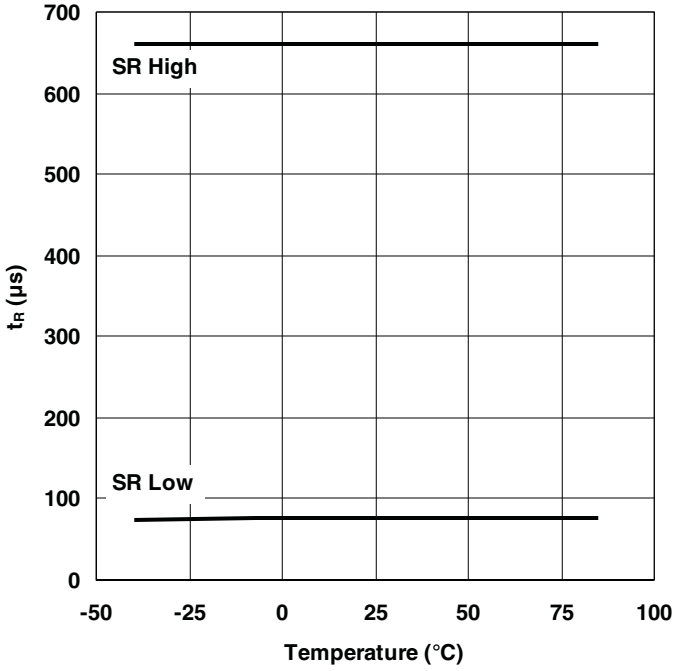


Figure 9.

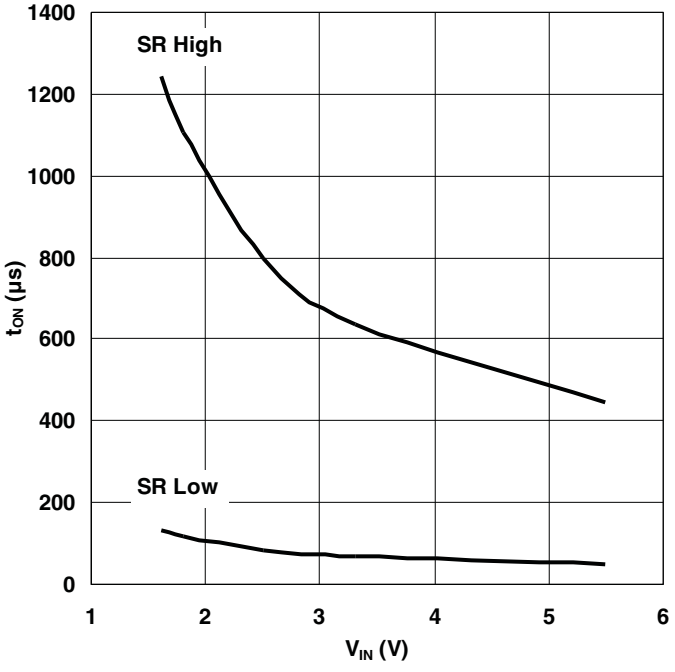


Figure 10.

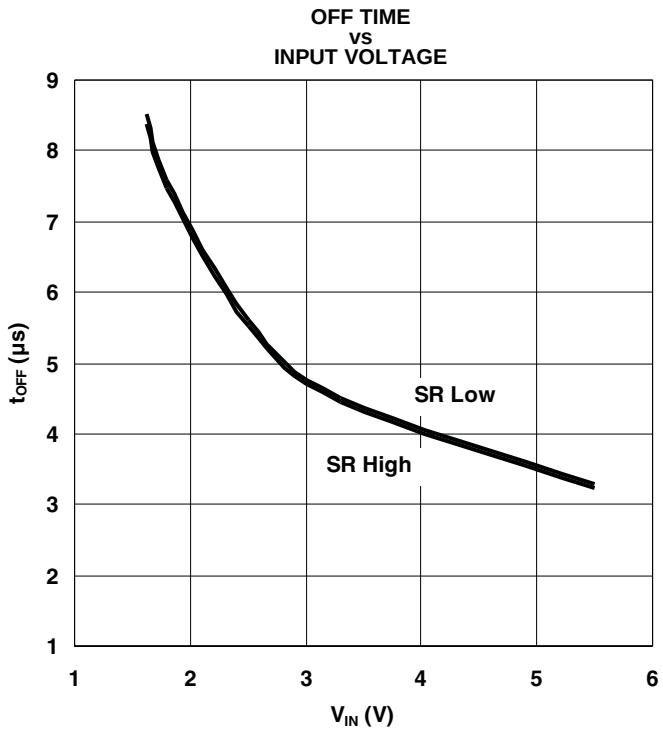


Figure 11.

TYPICAL CHARACTERISTICS (continued)

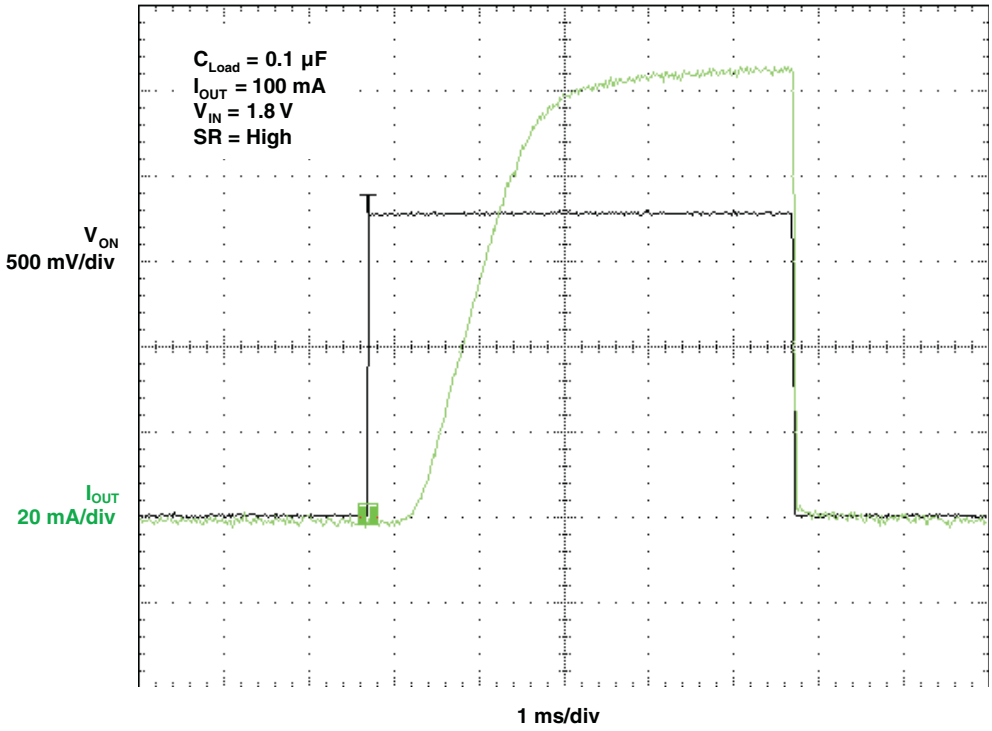


Figure 12. t_{ON} Response

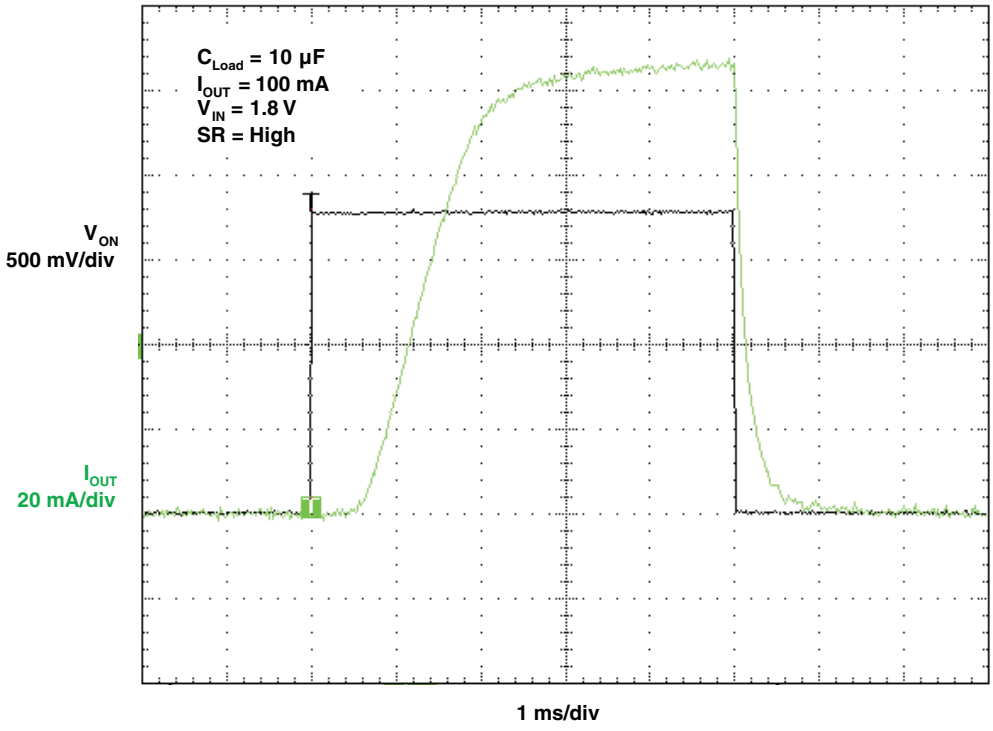


Figure 13. t_{ON} Response

TYPICAL CHARACTERISTICS (continued)

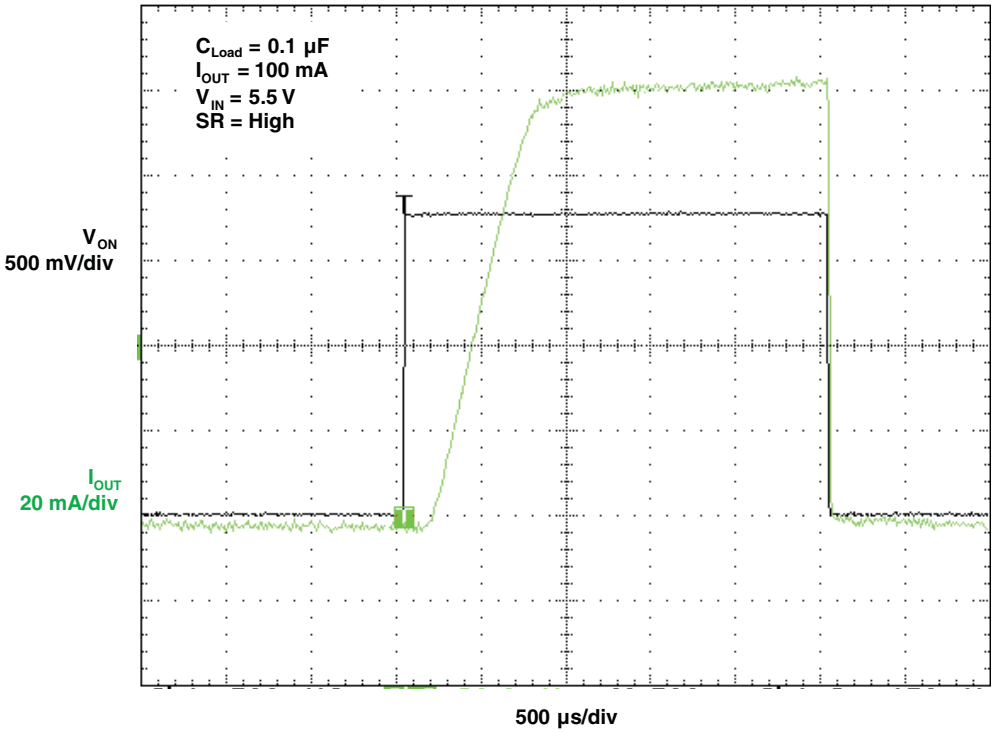


Figure 14. t_{ON} Response

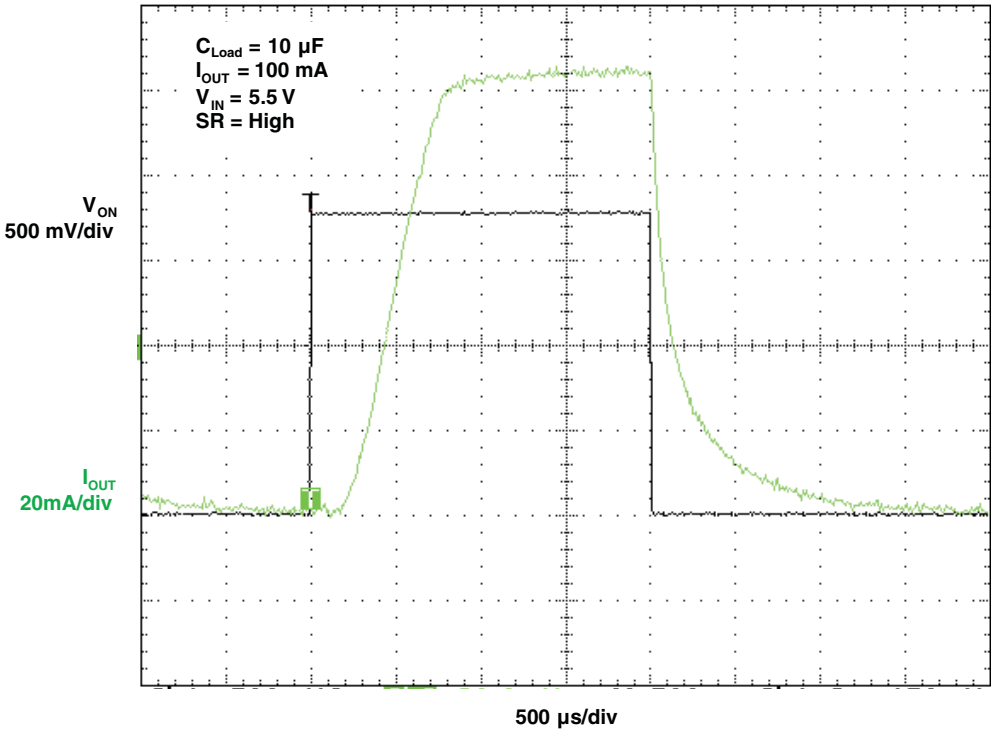


Figure 15. t_{ON} Response

TYPICAL CHARACTERISTICS (continued)

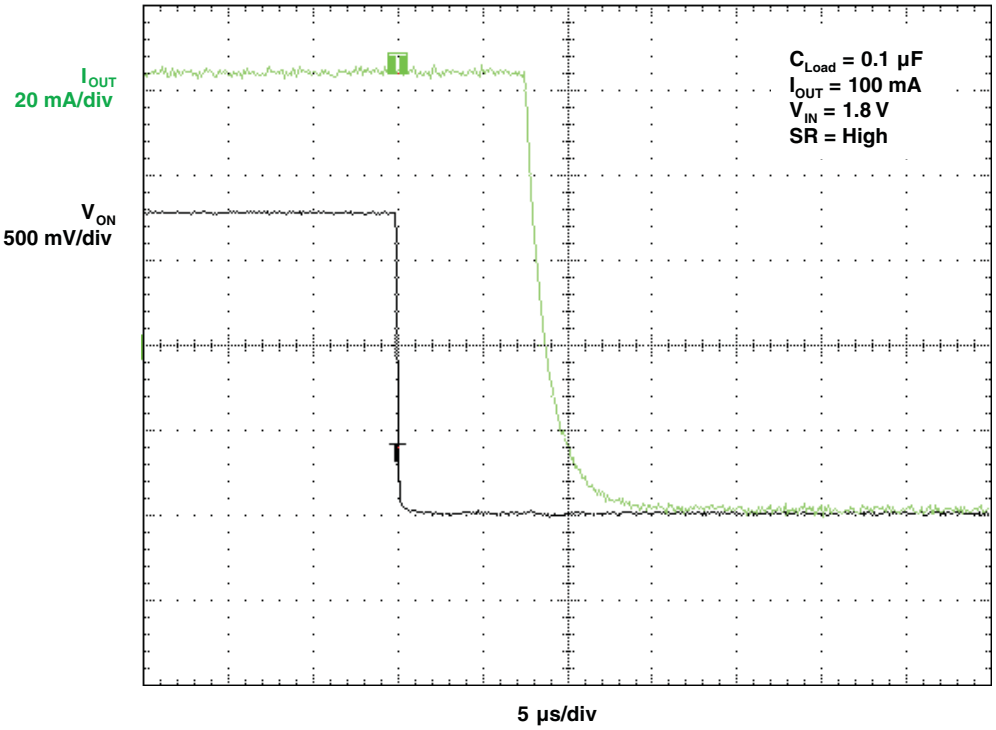


Figure 16. t_{OFF} Response

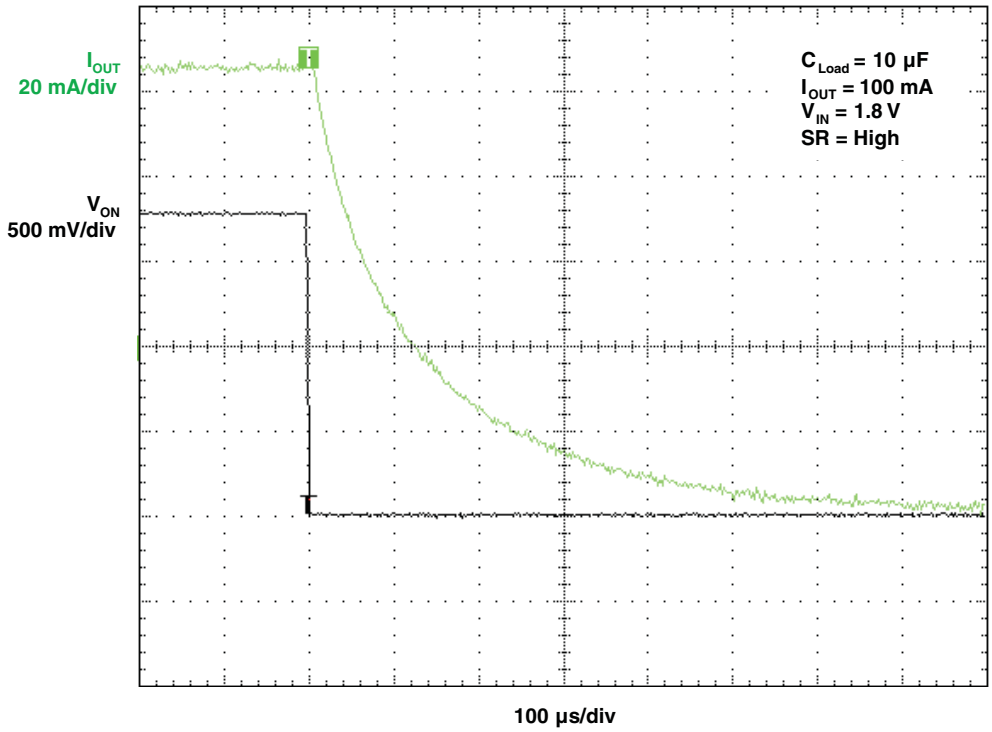


Figure 17. t_{OFF} Response

TYPICAL CHARACTERISTICS (continued)

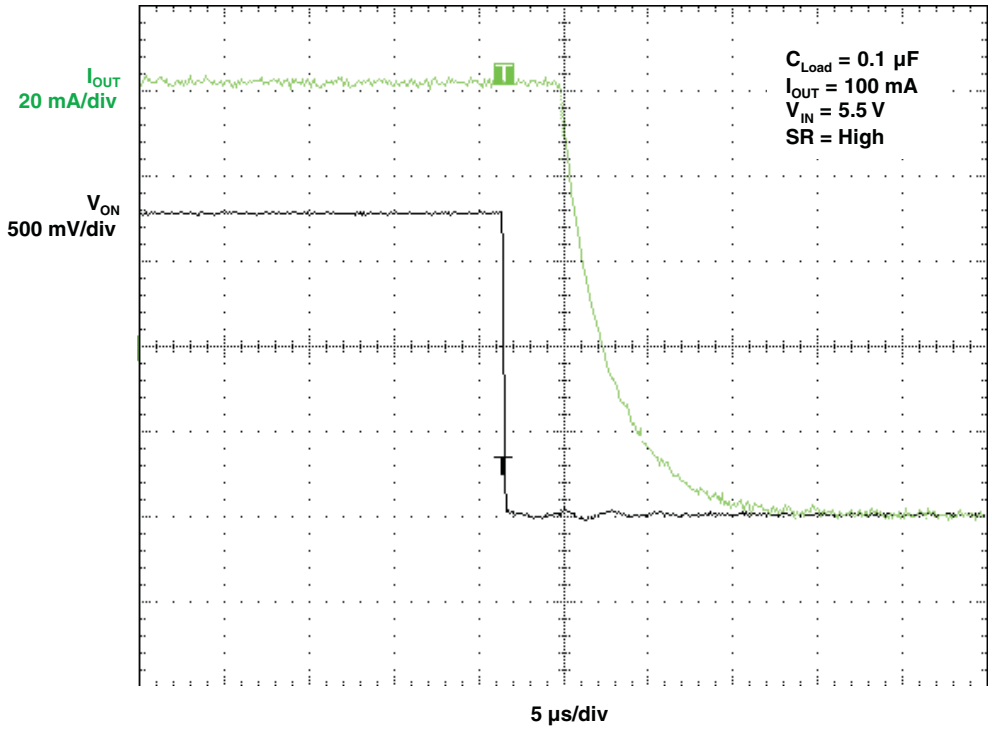


Figure 18. t_{OFF} Response

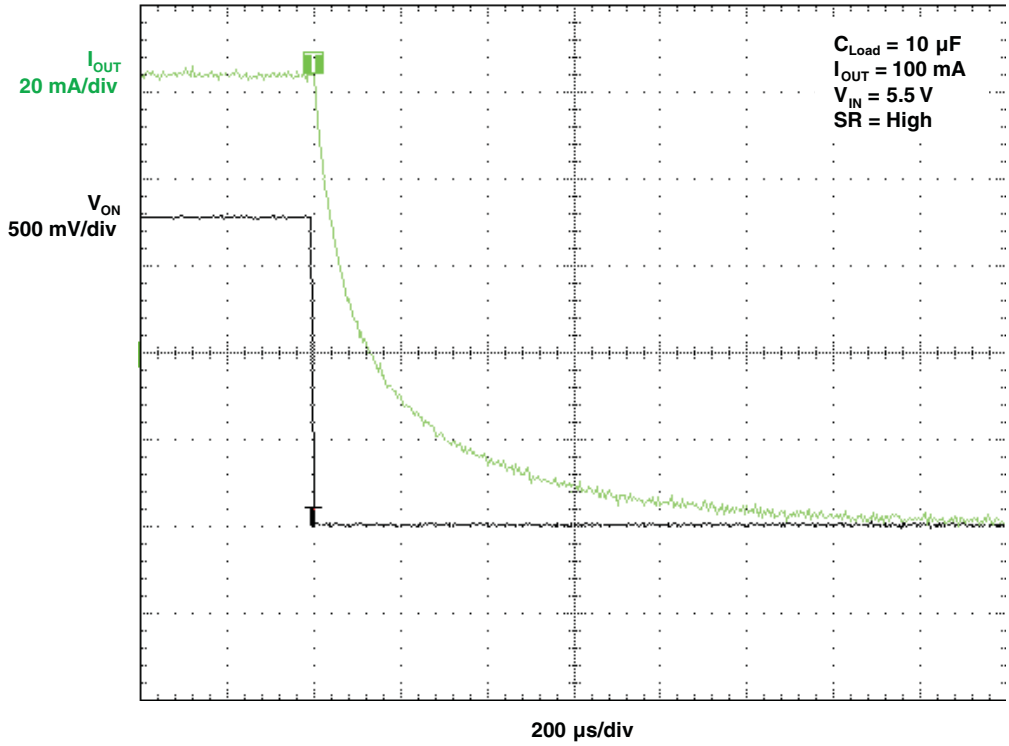


Figure 19. t_{OFF} Response

TYPICAL CHARACTERISTICS (continued)

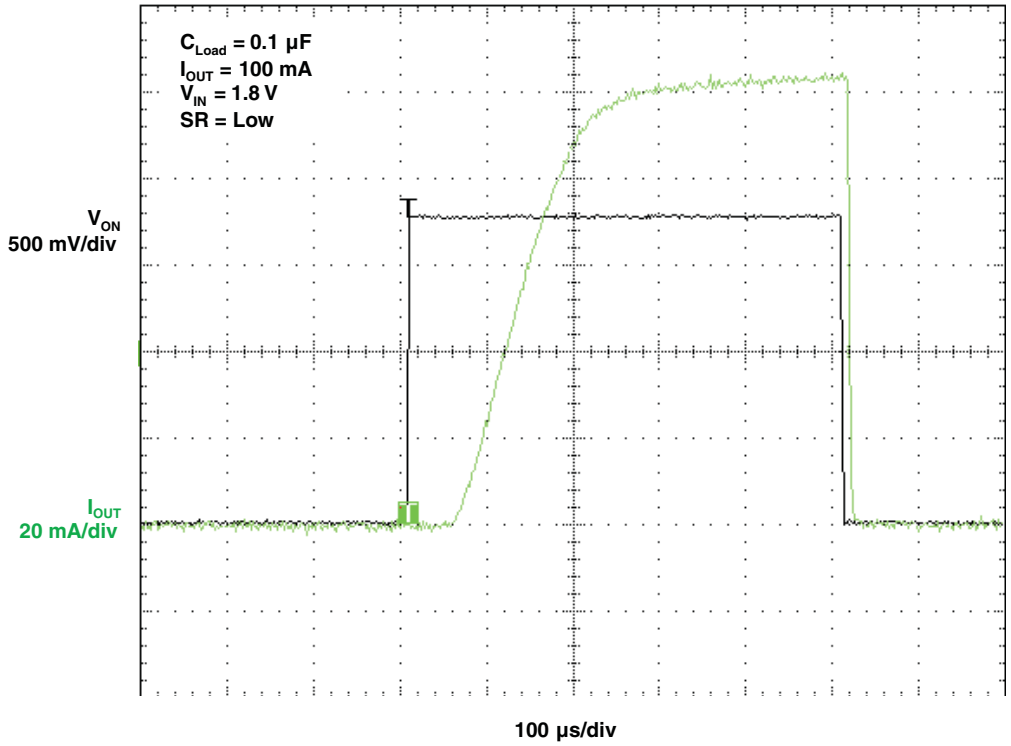


Figure 20. t_{ON} Response

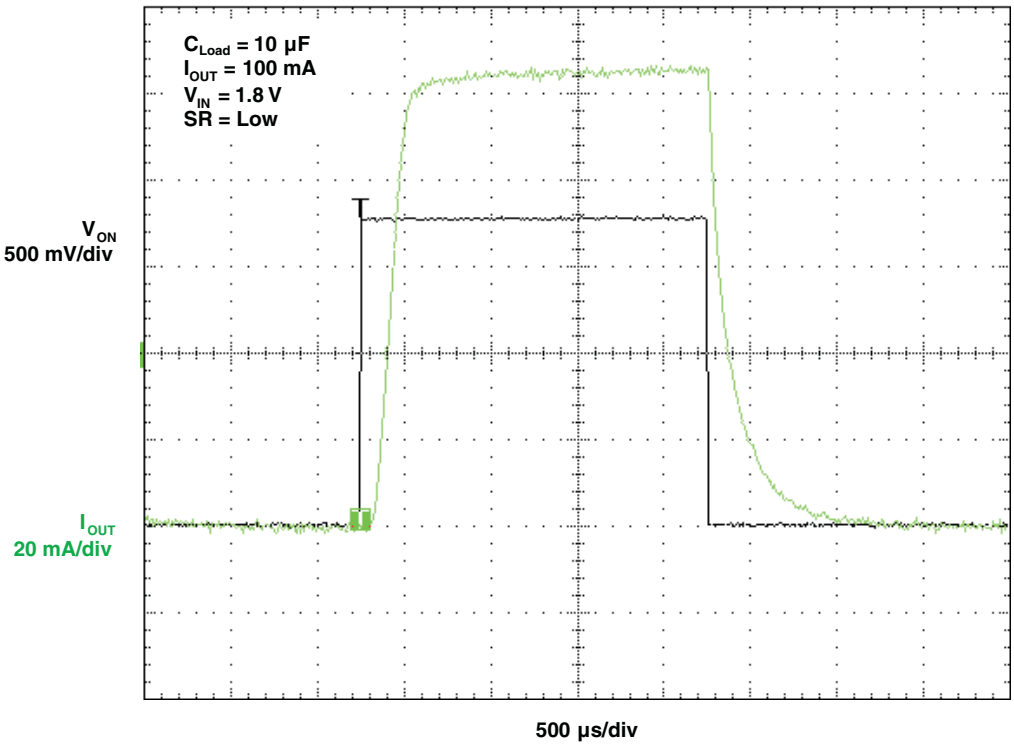


Figure 21. t_{ON} Response

TYPICAL CHARACTERISTICS (continued)

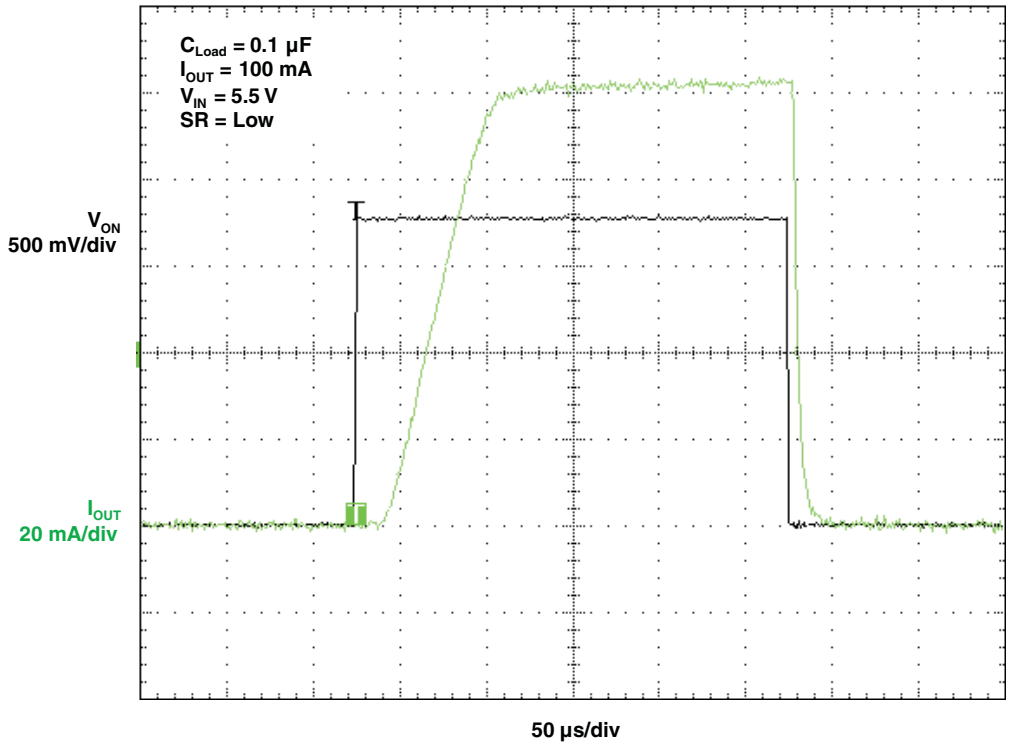


Figure 22. t_{ON} Response

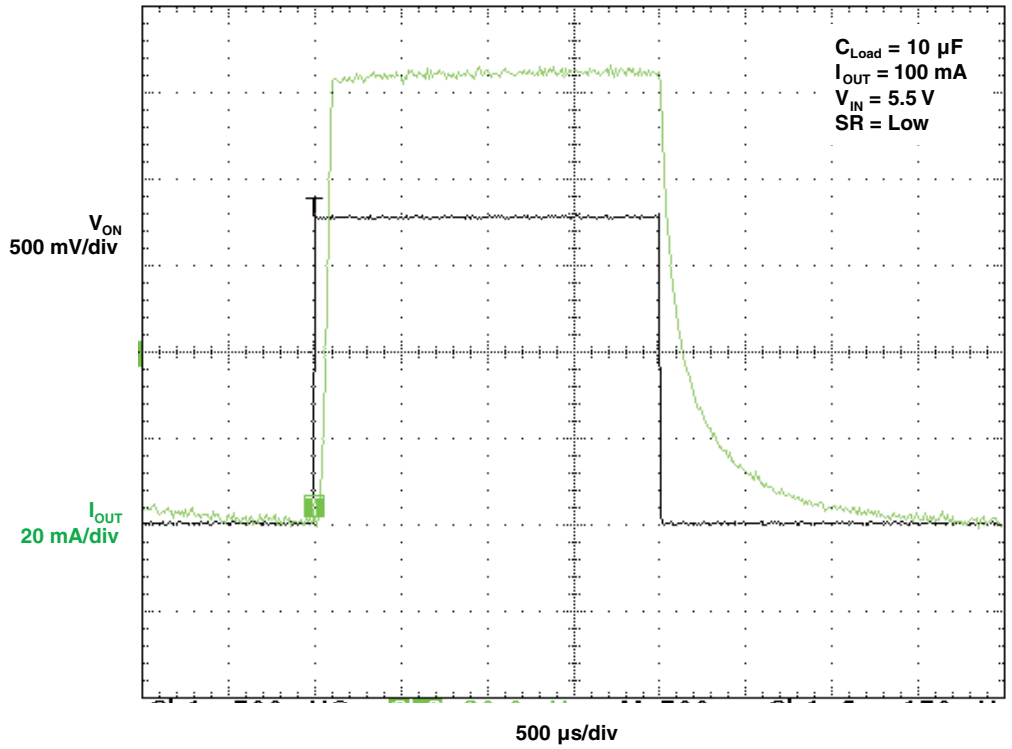


Figure 23. t_{ON} Response

TYPICAL CHARACTERISTICS (continued)

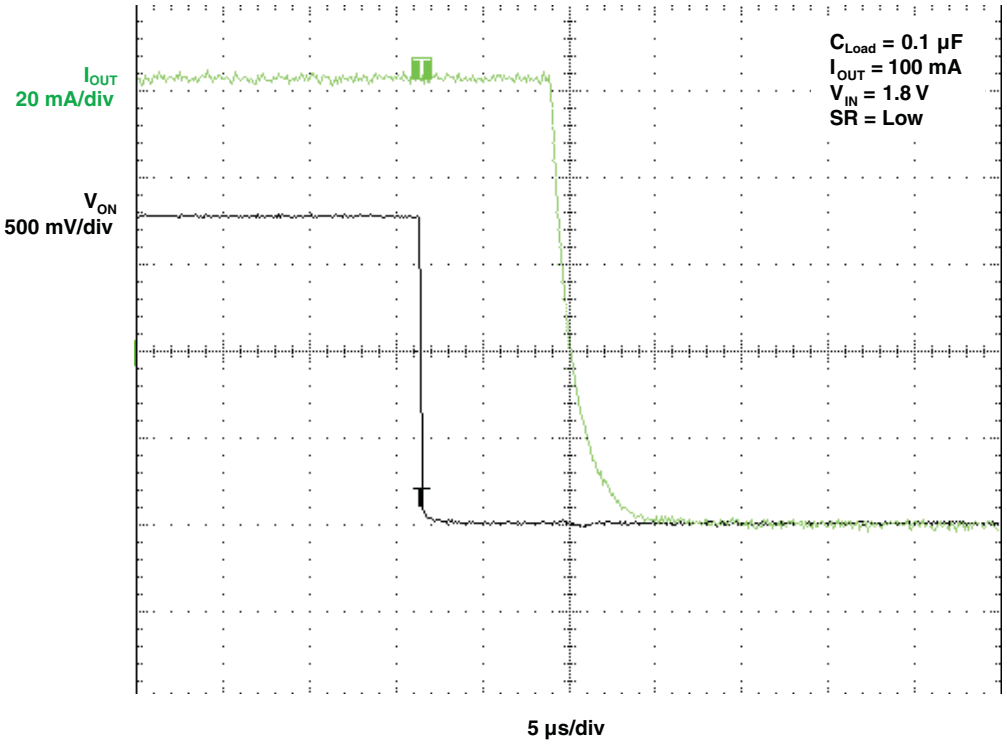


Figure 24. t_{OFF} Response

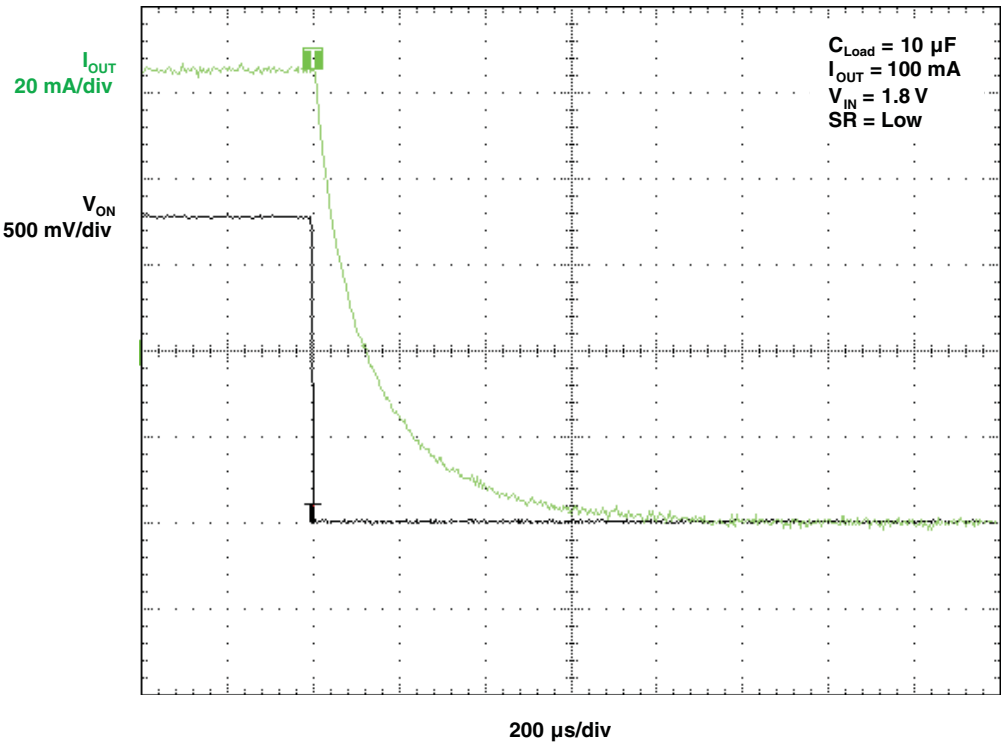


Figure 25. t_{OFF} Response

TYPICAL CHARACTERISTICS (continued)

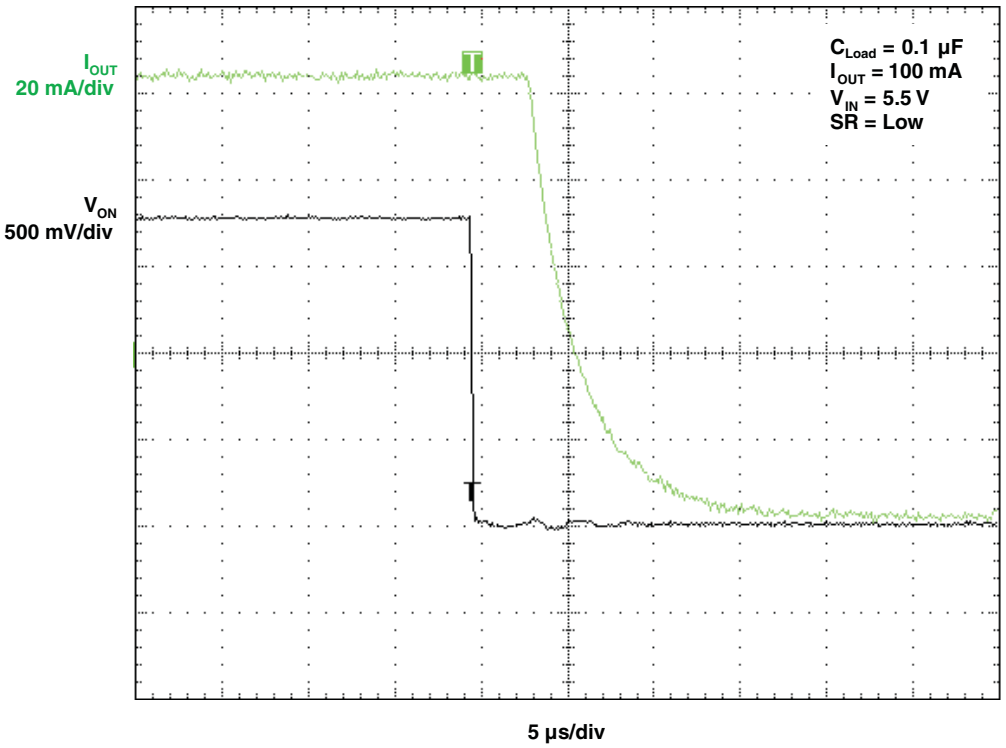


Figure 26. t_{OFF} Response

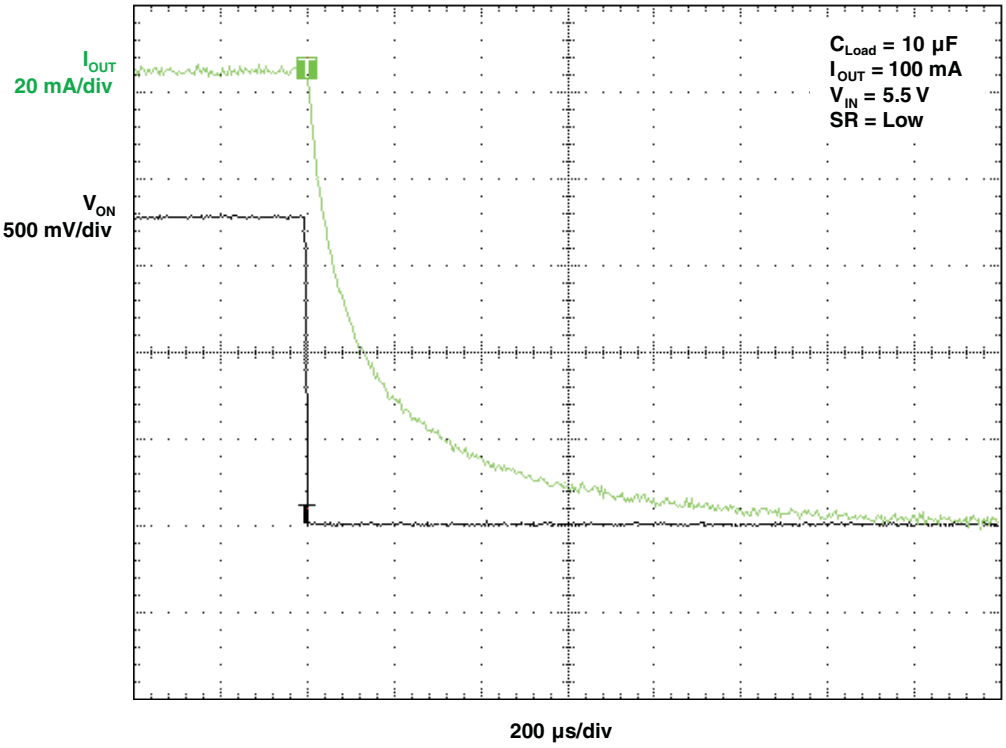
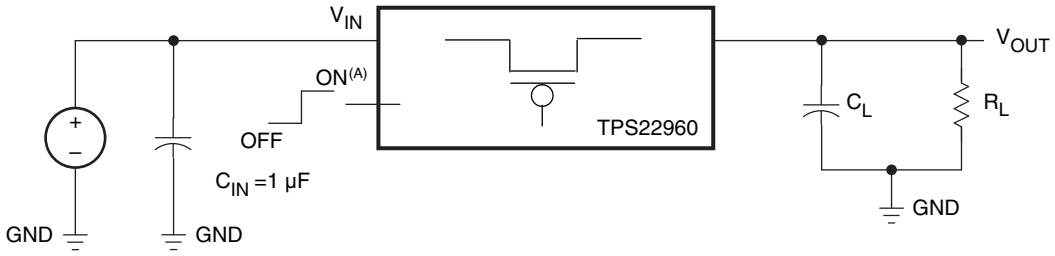
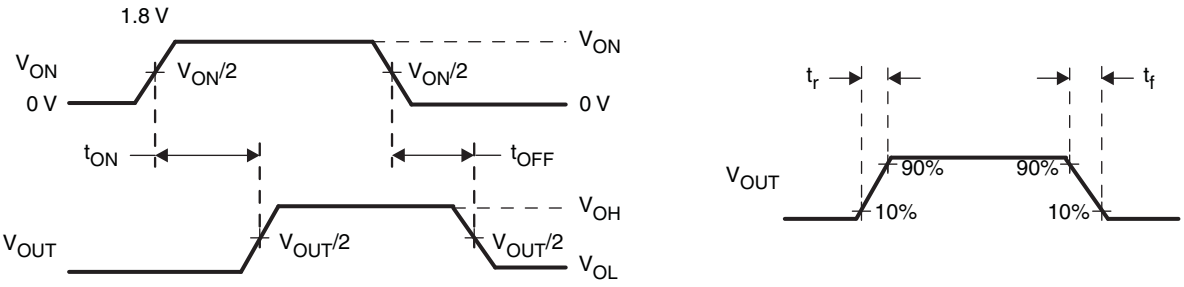


Figure 27. t_{OFF} Response

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



t_{ON}/t_{OFF} WAVEFORMS

A. t_{rise} and t_{fall} of the control signal is 100 ns.

Figure 28. Test Circuit and t_{ON}/t_{OFF} Waveforms

APPLICATION INFORMATION

ON/OFF Control

The ON pin controls the state of the switch. Activating ON continuously holds the switch in the on state so long as there is no fault. ON is active HI and has a low threshold making it capable of interfacing with low voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V, or 3.3-V GPIOs.

Input Capacitor

To limit voltage drop or voltage transients, a capacitor needs to be placed between V_{IN} and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient, but higher values of C_{IN} can be used. When switching heavy loads, it is recommended to have an input capacitor about ten times higher than the output capacitor.

Output Capacitor

Due to the integral body diode in the PMOS switch, a C_{IN} greater than C_L is recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}.

Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for VI_N, V_{OUT}, and GND will help minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

REVISION HISTORY

Changes from Original (April 2009) to Revision A **Page**

- Changed r_{ON} values for V_{INX} = 1.8 V (25°C) From: Typ 714, Max 855 To: Typ 737, Max 1100 4
- Changed r_{ON} values for V_{INX} = 1.8 V (Full) From: Max 995 To: Max 1300 4
- Changed r_{ON} values for V_{INX} = 1.62 V (25°C) From: Typ 830, Max 950 To: Typ 848, Max 1300 4
- Changed r_{ON} values for V_{INX} = 1.62 V (Full) From: Max 1100 To: Max 1500 4

Changes from Revision A (August 2011) to Revision B **Page**

- Clarified text in the DESCRIPTION. 1
- Updated CONFIGUREABLE LOGIC FUNCTION TABLE. 2
- Added T_J to the ABSOLUTE MAXIMUM RATING TABLE. 3
- Added RSE Package to DISSIPATION RATINGS table. 3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22960DCNR	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(NFRO ~ NFRR)	Samples
TPS22960RSER	ACTIVE	UQFN	RSE	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	72	Samples
TPS22960RSET	ACTIVE	UQFN	RSE	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	72	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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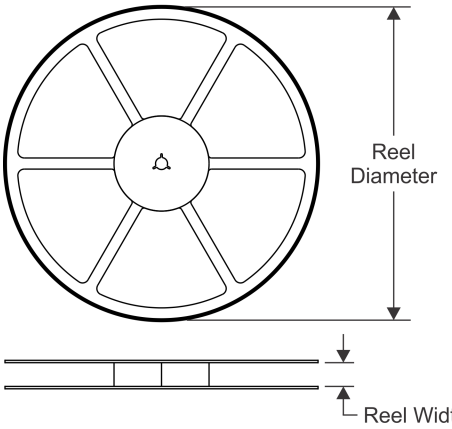
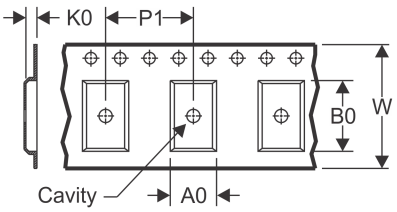
TAPE AND REEL INFORMATION

REEL DIMENSIONS

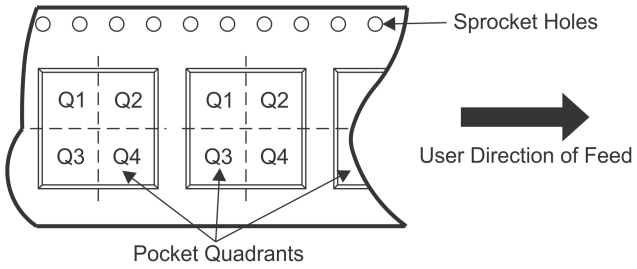


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

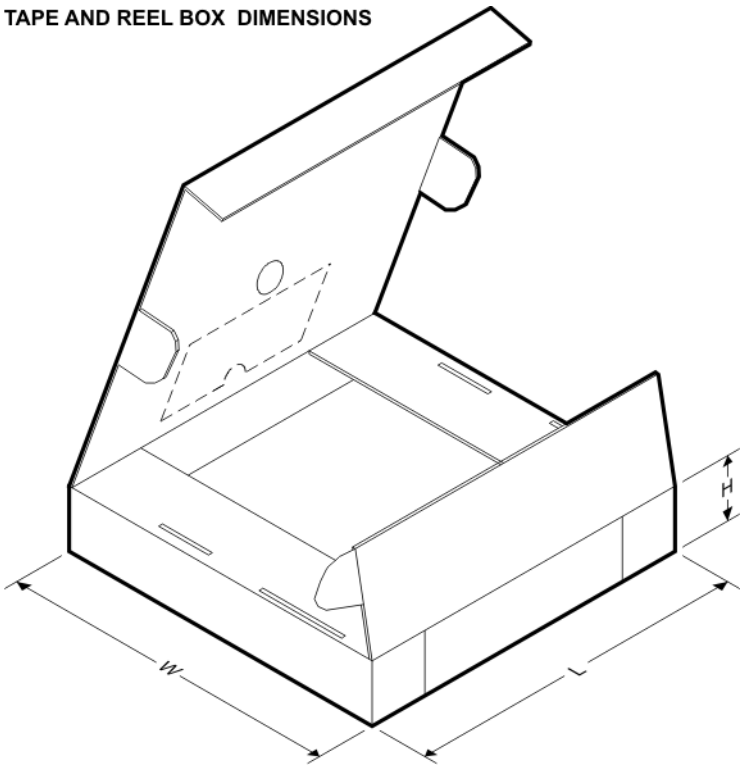
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22960DCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS22960DCNR	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS22960RSER	UQFN	RSE	8	3000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2
TPS22960RSET	UQFN	RSE	8	250	180.0	8.4	1.6	1.6	0.66	4.0	8.0	Q2

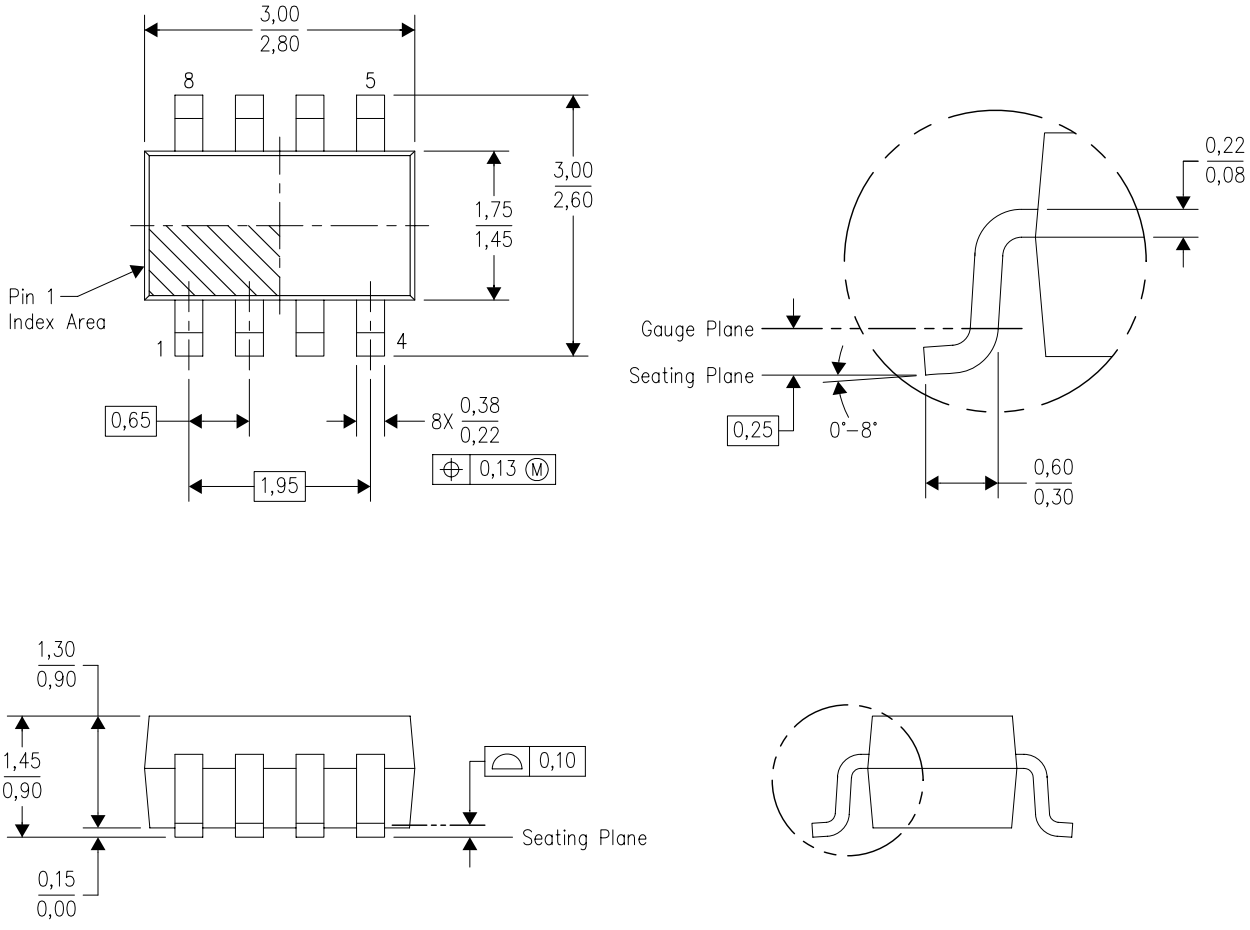
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

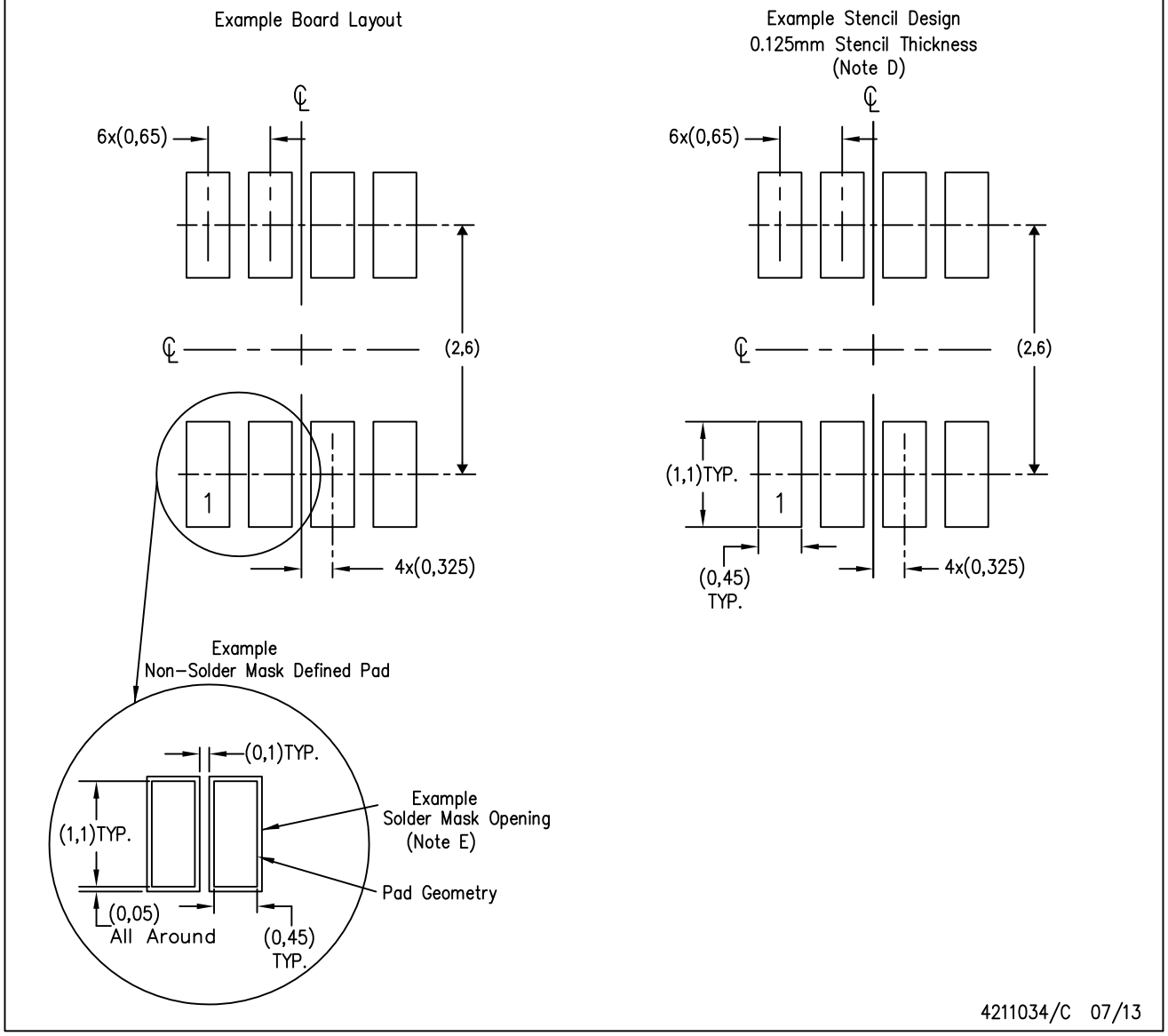
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22960DCNR	SOT-23	DCN	8	3000	202.0	201.0	28.0
TPS22960DCNR	SOT-23	DCN	8	3000	203.0	203.0	35.0
TPS22960RSER	UQFN	RSE	8	3000	202.0	201.0	28.0
TPS22960RSET	UQFN	RSE	8	250	202.0	201.0	28.0

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



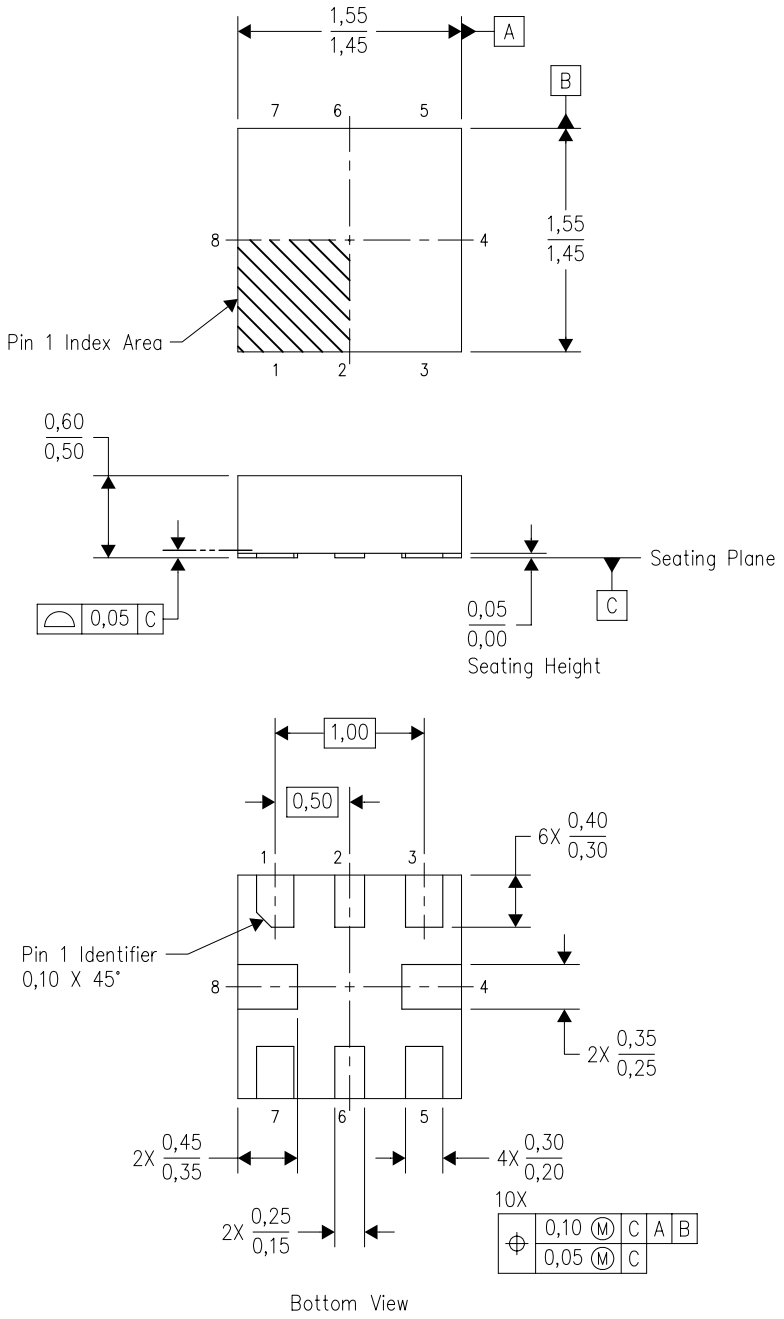
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RSE (S–PUQFN–N8) PLASTIC QUAD FLATPACK NO–LEAD

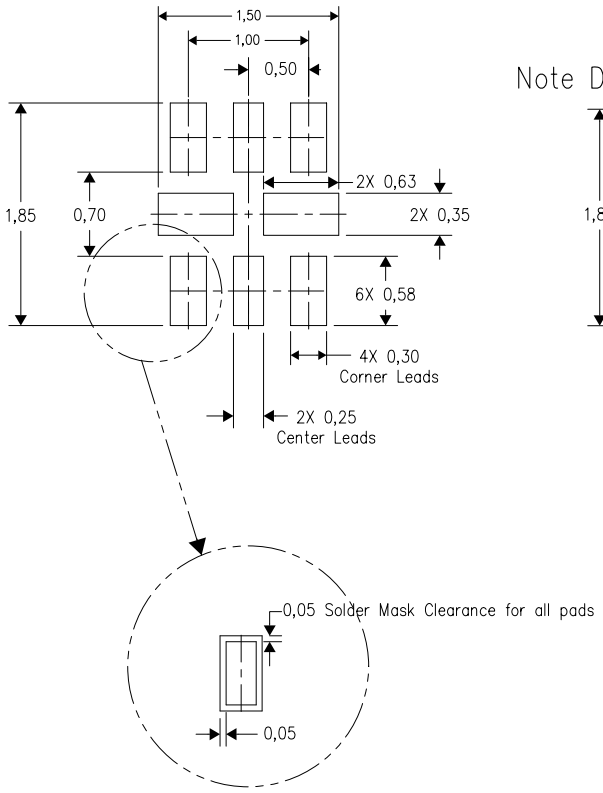


4207268–2/D 01/11

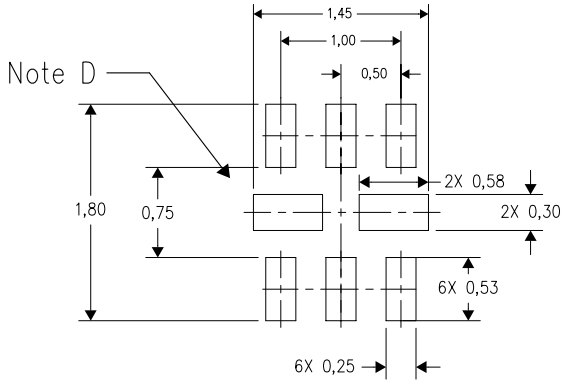
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UECD.

RSE (S–PUQFN–N8) PLASTIC QUAD FLATPACK NO–LEAD

Example Board Layout



Example Stencil Design
(Note E)



4208106–2/E 01/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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