DUAL CURRENT MODE, SYNCHRONOUS STEP-DOWN CONTROLLER WITH 100-mA STANDBY REGULATORS FOR NOTEBOOK SYSTEM POWER

FEATURES

- **3.3-V and 5-V 100-mA Bootstrapped Standby Regulators with Independent Enables**
- **Selectable D-CAP® Mode Enables Fast Transient Response Less than 100 ns**
- **Selectable Low Ripple Current Mode**
- **Less than 1% Internal Reference Accuracy**
- **Selectable PWM-only/Auto-skip Modes**
- **Low-side $R_{DS(on)}$ Loss-less Current Sensing**
- **R_{SENSE} Accurate Current Sense Option**
- **Internal Soft-start and Integrated V_{OUT} Discharge Transistors**
- **Integrated 2-V Reference**
- **Adaptive Gate Drivers with Integrated Boost Diode**
- **Power Good for Each Channel with Delay Timer**
- **Fault Disable Mode**
- **Supply Input Voltage Range: 4.5 V to 28 V**

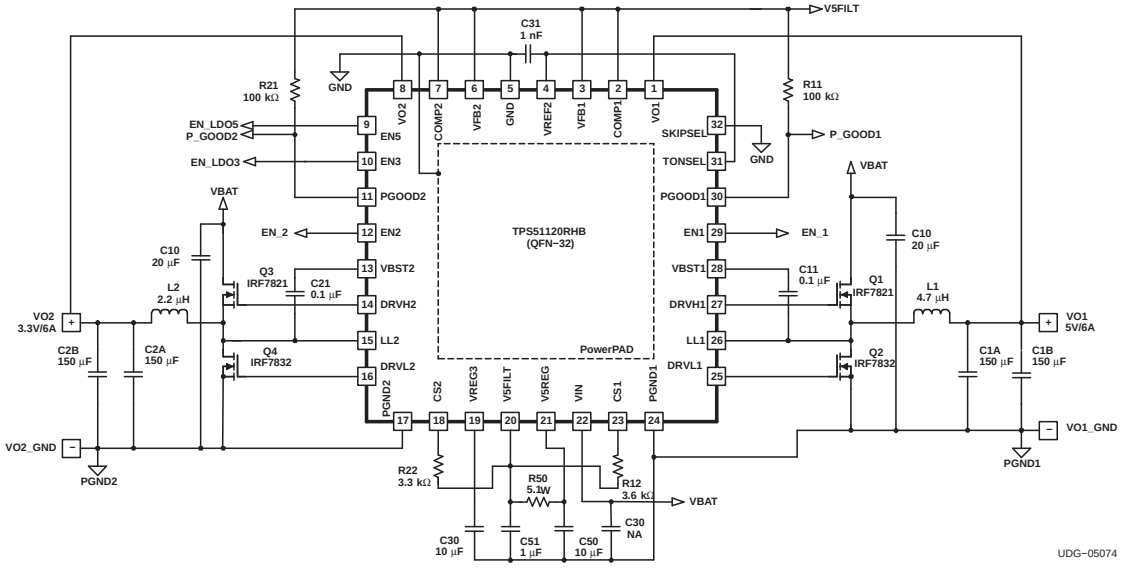
APPLICATIONS

- **Notebook Computers System Bus and I/O**

DESCRIPTION

The TPS51120 is a highly sophisticated dual current mode synchronous step-down controller. It is a full featured controller designed to run directly off a three- or four-cell Li-ion battery and provide high-power and 5-V and/or 3.3-V standby regulation for all the downstream circuitry in a notebook computer system. High current, 100-mA, 5-V or 3.3-V on-board linear regulators have glitch-free switch over function to SMPS and can be kept alive independently during standby state. The pseudo-constant frequency adaptive on-time control scheme supports full range of current mode operation including simplified loop compensation, ceramic output capacitors as well as seamless transition to reduced frequency operation at light-load condition. Optional D-CAP™ mode operation optimized for SP-CAP or POSCAP output capacitors allows further reduction of external compensation parts. Dynamic UVP supports VIN line sag without latch off by hitting 5V UVP. No negative voltage appears at output voltage node during UVLO, UVP, and OCP, OTP or loss of VIN.

The TPS51120 32-pin QFN package is specified from –40°C to 85°C ambient temperature.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

D-CAP is a registered trademark of Texas Instruments.

ORDERING INFORMATION(1)(2)

T_A	PACKAGE	ORDERABLE PART NUMBER	PINS	OUTPUT SUPPLY	MINIMUM ORDER QUANTITY	ECO PLAN
-40°C to 85°C	PLASTIC QUAD FLAT PACK (QFN)	TPS51120RHBT	32	Tape-and-reel	250	Green (RoHS and no Sb/Br)
		TPS51120RHBR		Tape-and-reel	3000	

(1) All packaging options have Cu NIPdAu lead/ball finish.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range unless otherwise noted

		TPS51120	UNITS
Input voltage range	VBST1, VBST2	-0.3 to 36	V
	VBST1, VBST2 wrt LL	-0.3 to 6	
	VIN, EN5	-0.3 to 30	
	SKIPSEL, TONSEL, EN1, EN2, CS1, CS2, V5FILT, VFB1, VFB2, EN3, VO1, VO2	-0.3 to 6	
Output voltage range	DRVH1, DRVH2	-1 to 36	V
	DRVH1, DRVH2 (wrt LL)	-0.3 to 6	
	LL1, LL2	-1 to 30	
	VREF2, VREG3, VREG5, PGOOD1, PGOOD2, DRVL1, DRVL2, COMP1, COMP2	-0.3 to 6	
	PGND1, PGND2	-0.3 to 0.3	
Source/sink current	VREF2	1	mA
	VBST	100	
	VREG5, VREG3 (source only)	200	
T_A	Operating ambient temperature range	-40 to 85	°C
T_{stg}	Storage temperature	-55 to 150	
T_J	Junction temperature	-40 to 125	
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	255	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

DISSIPATION RATINGS

PACKAGE	T_A < 25°C POWER RATING (W)	DERATING FACTOR ABOVE T_A = 25°C (W/°C)	T_A = 85°C POWER RATING (W)
32-pin QFN(1)	2.6	0.026	1.0
32-pin QFN(2)	2.9	0.029	1.2

(1) JEDEC standard PCB.
(2) Enhanced thermal conductance by 3 x 3 thermal vias beneath thermal pad.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Input voltage, V5FILT		4.5	5.5	V
Input voltage range	VBST1, VBST2	-0.1	34	V
	VBST1, VBST2 wrt LL	-0.1	5.5	
	VIN, EN5	-0.1	28	
	SKIPSEL, TONSEL, EN1, EN2, CS1, CS2, V5FILT, VFB1, VFB2, EN3	-0.1	5.5	
	VO1, VO2	-0.1	5.5	
Output voltage range	DRVH1, DRVH2	-0.8	34	V
	DRVH1, DRVH2 (wrt LL)	-0.1	5.5	
	LL1, LL2	-0.8	28	
	VREF2, VREG5, VREG3, PGOOD1, PGOOD2, DRVL1, DRVL2, COMP1, COMP2	-0.1	5.5	
	PGND1, PGND2	-0.1	0.1	
Source/sink current	VREF2		0.08	mA
	VBST		50	
	VREG5, VREF3 (source only)		100	
Operating ambient temperature range, T_A		-40	85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{VIN} = 12 V, V_{VREG5} = V_{V5FILT} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{INCCAP}	Supply current	VIN current, VREG5=VREG3=No Load, EN3=EN5=FLOAT, EN1=EN2=5V, CS=5V, COMP connected to Cap	Current mode		750	1500	μA
$I_{INNOCAP}$	Supply current	VIN current, VREG5=VREG3=No Load, EN3=EN5=FLOAT; EN1=EN2=5V, CS=5V, COMP=5V	D-CAP mode		700	1400	
$I_{IN5(STBY)}$	Stand-by current	VIN current, VREG5=No Load EN3=0V, EN5=FLOAT, EN1=EN2=0	5-V only		30	45	
$I_{IN3(STBY)}$	Stand-by current	VIN current, VREG3=No Load EN3=FLOAT, EN5=0, EN1=EN2=0	3.3-V only		12	20	
$I_{IN532(STBY)}$	Stand-by current	VIN current, VREG5=VREG3=VREF2=No Load EN3=EN5=FLOAT, EN1=EN2=0			100	160	
$I_{IN(SHDN)}$	Shut down current	VIN current, EN3=EN5=EN1=EN2=0V			10	20	
VOUT and VREF2 VOLTAGES							
V_{OUT}	Output voltage	V_{FB2} = 3.3 V, T_A= 25°C, No Load		3.241	3.300	3.359	V
		V_{FB2} = 3.3 V, T_A= 0 to 85°C, No Load		3.234	3.300	3.366	
		V_{FB2} = 3.3 V, T_A= -40 to 85°C, No Load		3.224	3.300	3.376	
		V_{FB1} = 5 V, T_A= 25°C, No Load		4.910	5.000	5.090	
		V_{FB1} = 5 V, T_A= 0 to 85°C, No Load		4.900	5.000	5.100	
		V_{FB1} = 5 V, T_A= -40 to 85°C, No Load		4.885	5.000	5.115	
		Adjustable mode output range		1.0		5.5	
V_{ADJ}	Output regulation voltage	Adjustable mode			1.00		V
$V_{ADJ\ T}$	Output regulation voltage tolerance	Adjustable mode, T_A= 25°C		-0.9%		0.9%	
		Adjustable mode, T_A= 0 to 85°C		-1.3%		1.3%	
		Adjustable mode, T_A= -40 to 85°C		-1.6%		1.6%	
V_{VREF2}	2-V output regulation voltage	I_{VREF2}± 50 μA, T_A= 25°C		1.97	2.00	2.03	V
V_{VREF2T}	2-V output regulation voltage tolerance	I_{VREF2}± 50 μA, T_A= 0 to 85°C		1.96		2.04	
		I_{VREF2}± 50 μA, T_A= -40 to 85°C		1.95		2.05	
I_{VFB}	VFB input current	VFBx=1.02V, COMPx=open			0.02		μA
		VFBx=1.02V, COMPx=5V			0.02		
$R_{DISCHARG}$	Discharge switch resistance	VOx=0.5V, T_A= 25°C			10	20	Ω

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, V_{VIN} = 12 V, V_{VREG5} = V_{V5FILT} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VREG3 VOLTAGE						
V_{VREG3}	VREG3 Output Regulation Voltage	I_{VREG3} = 20 mA, 6V < VIN < 28V, T_A= 25°C	3.25	3.30	3.35	V
V_{VREG3T}	VREG3 Output Voltage Tolerance	I_{VREG3} = 1 - 50 mA , 6V < VIN < 28V, T_A= 0 to 85°C	3.21		3.37	V
		I_{VREG3} = 1 - 100 mA , 6V < VIN < 28V, T_A= -40 to 85°C	3.16		3.39	V
I_{VREG3}	VREG3 Output Current	T_A = 25°C, VREG3=3.14V (1)		170		mA
V_{LDO3SW}	VREG3 Bootstrap Switch Threshold	Rising edge of VO2, VREG3 drops to VO2 voltage	2.85		3.10	V
		Hysteresis		120		mV
R_{LDO3SW}	VREG3 Bootstrap Switch Resistance			1.3	3.0	Ω
VREG5 VOLTAGE						
V_{VREG5}	VREG5 Output Regulation Voltage	I_{VREG5} = 20 mA, 6V < VIN < 28V, TA= 25°C	4.925	5.00	5.075	V
V_{VREG5T}	VREG5 Output Voltage Tolerance	I_{VREG5} = 1 - 50 mA , 6V < VIN < 28V, T_A= 0 to 85°C	4.89		5.11	V
		I_{VREG5} = 1 - 100 mA , 6V < VIN < 28V, T_A= -40 to 85°C	4.80		5.15	V
I_{VREG5}	VREG5 Output Current	T_A = 25°C, VREG5=4.75 V(1)		200		mA
V_{LDO5SW}	VREG5 Bootstrap Switch Threshold	Rising edge of VO1, VREG5 drops to VO1 voltage	4.30		4.85	V
		Hysteresis		140		mV
R_{LDO5SW}	VREG5 Bootstrap Switch Resistance			1.3	3.0	Ω
TRANSCONDUCTANCE AMPLIFIER						
Gm	Gain	T_A = 25°C		280		µS
$I_{COMPSINK}$	COMP Maximum Sink Current	VFBx=1.05V, COMPx=1.28V	8	12	16	µA
$I_{COMPSRC}$	COMP Maximum Source Current	VFBx=0.95V, COMPx=1.28V	-15	-11	-7	µA
V_{COMPHI}	COMP High Clamp Voltage	CSx=0V, VFBx=0.95V	1.26	1.34	1.42	V
V_{COMPLO}	COMP Low Clamp Voltage	CSx=0V, VFBx=1.05V	1.08	1.12	1.20	V
OUTPUT DRIVER						
R_{DRVH}	DRVH resistance	Source, $V_{VBST-DRVH}$ = 1V		3.5	7	Ω
		Sink, $V_{DRVH-LL}$ = 1V		1.5	3	Ω
R_{DRVL}	DRVL resistance	Source, $V_{VREG5-DRVL}$ = 1V		3.5	7	Ω
		Sink, $V_{DRVL-PGND}$ = 1V		1.5	3	Ω
T_D	Dead time	DRVH-off to DRVL-on, T_A= 25°C		20		ns
		DRVL-off to DRVH-on, T_A= 25°C	30	60		ns
V_{DTH}	DRVH-off threshold	LL to GND(1)		2		V
V_{DTL}	DRVL-off threshold	DRVL to GND (1)		1.1		V
INTERNAL BST DIODE						
V_{FBST}	Forward Voltage	$V_{VREG5-VBST}$, I_F = 10 mA, T_A= 25°C	0.7	0.8	0.9	V
I_{RBST}	Reverse Current	VBST = 34 V, VREG5=5V		0.1	1.0	µA
$I_{BST(LEAK)}$	VBST Leakage current	VBST=34V, LL=28V, EN3=EN5=EN1=EN2=0V		0.1	1.0	µA

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, V_{VIN} = 12 V, V_{VREG5} = V_{V5FILT} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ON-TIME TIMER, INTERNAL SOFT-START and HOUSEKEEPING CLOCK						
T_{ON1a}	On time, 5V, 180 kHz	V_{LL1}=12V, V_{OUT1}=5V, TONSEL=5V, T_A= 25°C	2150	2340	2530	ns
T_{ON1b}	On time, 5V, 220 kHz	V_{LL1}=12V, V_{OUT1}=5V, TONSEL=FLOAT, T_A= 25°C	1790	1950	2110	
T_{ON1c}	On time, 5V, 280 kHz	V_{LL1}=12V, V_{OUT1}=5V, TONSEL=2V, T_A= 25°C	1370	1490	1610	
T_{ON1d}	On time, 5V, 380 kHz	V_{LL1}=12V, V_{OUT1}=5V, TONSEL=GND, T_A= 25°C	1020	1110	1200	
T_{ON2a}	On time, 3.3V, 270 kHz	V_{LL2}=12V, V_{OUT2}=3.3V, TONSEL=5V, T_A= 25°C	940	1030	1120	
T_{ON2b}	On time, 3.3V, 330 kHz	V_{LL2}==12V, V_{OUT1}=3.3V, TONSEL=FLOAT, T_A= 25°C	780	850	920	
T_{ON2c}	On time, 3.3V, 430 kHz	V_{LL2}==12V, V_{OUT1}=3.3V, TONSEL=2V, T_A= 25°C	580	650	720	
T_{ON2d}	On time, 3.3V, 580 kHz	V_{LL2}==12V, V_{OUT1}=3.3V, TONSEL=GND, T_A= 25°C	430	480	530	
$T_{ON(MIN)1}$	Minimum on time, 5V	T_A = 25°C, TONSEL=GND, V_{LL1}=28V, VO1=1V		70		
$T_{ON(MIN)2}$	Minimum on time, 3.3V	T_A = 25°C, TONSEL=GND, V_{LL2}=28V, VO2=1V		45		
$T_{OFF(MIN)}$	Minimum off time	T_A = 25°C, VFB=0.9V, LL=0.5V		480		
T_{SS}	Internal Soft Start Timer	T_A = 25°C, ENx>3V		772		clks
SL_{SS}	Internal Soft Start Slope	T_A = 25°C, ENx>3V, Slope wrt. VFB (2)		0.3		V/ms
F_{CLK}	HK clock frequency		230	290	350	kHz
UVLO/LOGIC THRESHOLD						
V_{ENLDOH}	LDO enable threshold	EN3, EN5, low to high	0.3	0.6	0.8	V
		Hysteresis		0.2		
$V_{ENLDOFL3}$	EN3 pullup voltage	EN3 = FLOAT (OPEN) (2)		1.7		
$V_{ENLDOFL5}$	EN5 pullup voltage	EN5= FLOAT (OPEN) (2)		3.3		
$I_{ENLDOFL}$	EN3, EN5 pullup current	VENx < 0.5V		1.5	4.0	µA
$V_{UV(VREG5)}$	VREG5 UVLO threshold	Wake up	3.8	4.0	4.2	V
		Hysteresis	100	200	300	mV
$V_{SKIPSEL}$	SKIPSEL threshold	Auto-SKIP Mode Enabled	0		0.7	V
		Auto-SKIP Mode Enabled, Faults Off	1.3		2.2	
		PWM-Only Mode Enabled	2.7		5.5	
V_{TONSEL}	TONSEL threshold	Fast Switching Frequency	0		0.7	
		Medium Switching Frequency #2	1.3		2.2	
		Medium Switching Frequency #1	2.7		3.0	
		Slow Switching Frequency	4.5		5.5	
I_{SEL}	SKIPSEL/TONSEL input current	SKIPSEL, TONSEL=0V		1	3	µA
		SKIPSEL, TONSEL=5V		1	2	
$V_{ENSWSTAT}$	EN1, EN2 SS Start Voltage	BJT Base input, Switcher begins to Track ENx	0.5	0.9	1.2	V
$V_{ENSWEND}$	EN1, EN2 SS End Voltage	'Logic High' Level for Switcher Enable when using Internal Softstart, 0°C ≤ T_A≤ 85°C		2.75	2.90	
$I_{ENSW1,2}$	EN1, EN2 Pullup Current	EN1, EN2=0.6V	1	2	3	µA
V_{THVFB1}	VFB1 threshold	5.0V preset output	V5FILT -0.3			V
V_{THVFB2}	VFB2 threshold	3.3V preset output	V5FILT -0.3			
CURRENT SENSE						
V_{OCL}	Current limit threshold	Resistor sense scheme , $V_{PGND - VCS}$ voltage, PGOOD=Hi	67	80	93	mV
I_{TRIP}	CS Sink Current	$R_{DS(ON)}$ sense scheme, PGOOD=Hi, T_A= 25°C	9	10	11	µA
TC_{ITRIP}	I_{TRIP} temperature Coefficient	$R_{DS(ON)}$ sense scheme, On the basis of 25°C		4500		ppm/°C

(2) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, V_{VIN} = 12 V, V_{VREG5} = V_{V5FILT} = 5 V (unless otherwise noted)

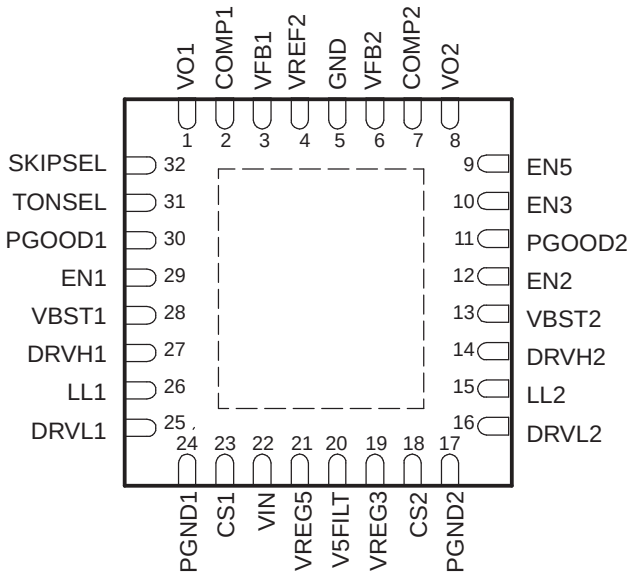
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OCLoff}	OCP Comparator Offset	($V_{VREG5-CS}$-$V_{PGND-LL}$) voltage, $V_{VREG5-CS}$ = 80mV, $R_{DS(ON)}$ sense	-10	0	10	mV
$V_{R(trip)}$	Current limit threshold setting range	V_{V5FILT}-V_{CS} voltage	30		150	
V_{ZC}	Zero cross detection Comparator offset	V_{PGNDx}-V_{LLx} voltage, SKIPSEL=0V	-5	1	5	
POWERGOOD COMPARATOR						
$V_{TH(PG)}$	PGOOD Threshold	Power Bad Threshold	±7%	±10%	±13%	
		Hysteresis		±5%		
$I_{PG(MAX}$	PGOOD Sink Current	PGOOD=0.5 V	2.5	5.0		mA
T_{PGDEL}	PGOOD Delay Timer	Delay for PGOOD in, ‘clks’=HK Clock		256		clks
UNDERVOLTAGE and OVERVOLTAGE PROTECTION						
V_{OVP}	VFBx OVP Trip Threshold	OVP detect	110%	115%	120%	
T_{OVPDEL}	VFBx OVP Delay Time			2		ms
V_{UVP}	VFBx UVP Trip Threshold	UVP detect	65%	70%	75%	
		Hysteresis		6%		
T_{UVPDEL}	VFBx UVP Delay Timer	‘clks’=HK Clock		128		clks
THERMAL SHUTDOWN						
T_{SDN1}	Thermal shutdown threshold	Shutdown temperature		145		°C
		Hysteresis		10		

DEVICE INFORMATION

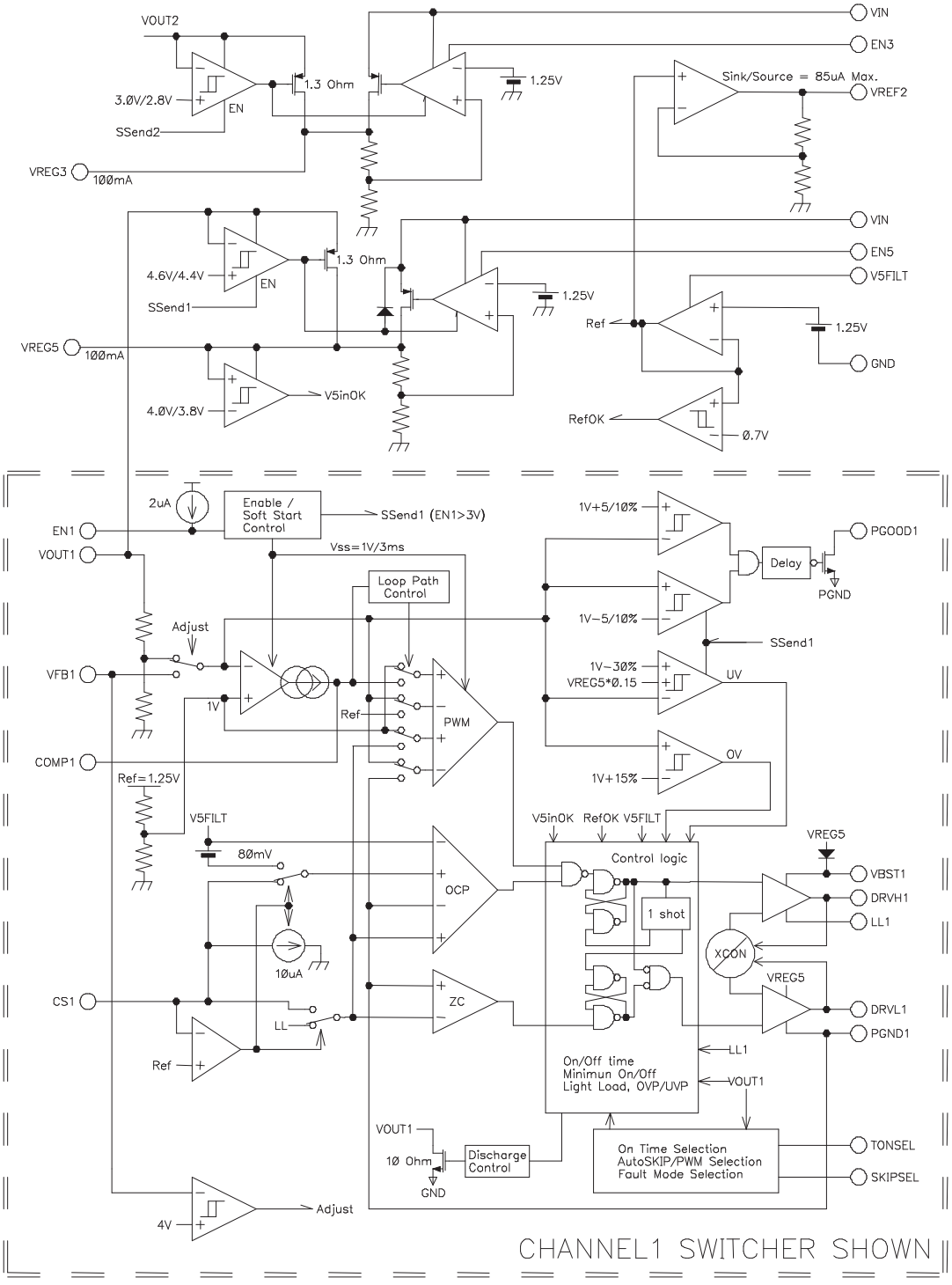
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
COMP1	2	O	Loop compensation pin (error amplifier output). Connect RC from this pin to GND for proper loop compensation with current mode operation. Tie this pin to V5FILT for D-CAP™ mode operation.
COMP2	7	O	
CS1	23	I	Current sense comparator input (-) for resistor sensing scheme. Or, overcurrent trip setting input for $R_{DS(on)}$ current sense scheme if connected to V5FILT through the threshold setting resistor.
CS2	18	I	
DRVH1	27	O	High-side MOSFET gate drive output. Source 3.5 Ω, sink 1.5 Ω, LL-node referenced floating driver. Drive voltage corresponds to VBST to LL voltage.
DRVH2	14	O	
DRVL1	25	O	Rectifying (low-side) MOSFET gate drive output. Source 3.5 Ω, sink 1.5 Ω, PGND referenced driver. Drive voltage is VREG5 voltage.
DRVL2	16	O	
EN1	29	I	Channel 1 and Channel 2 SMPS enable pins. Connect to 5 V to turn on with internal 3-ms soft-start. Slower soft-start is possible by applying an external capacitor from each of these pins to ground to program ramp rate.
EN2	12	I	
EN3	10	I	VREG3, 3.3-V low dropout linear regulator enable pin. Connect to GND to disable. Float or tie to enabled VREG5 to turn on the regulator.
EN5	9	I	VREG5, 5-V low dropout linear regulator enable pin. Connect to GND to disable. Float or tie to VBAT to turn on the regulator.
GND	5	I	Signal ground pin.
LL1	26	I/O	High-side MOSFET gate driver return. Also serve as current sense comparator input (-) for $R_{DS(on)}$ sensing, and input voltage monitor for on-time control circuitry
LL2	15	I/O	
PGND1	24	I/O	Ground return for rectifying MOSFET gate driver. Connect PGND2, PGND1 and GND strongly together near the source of the rectifying FET or the GND connection of the current sense resistor. Also serve as current sense comparator input (+).
PGND2	17	I/O	
PGOOD1	30	O	Power-good window comparator open drain output. Pull up with resistor to V5FILT or appropriate signal voltage. Current capability is 5-mA. PGOOD goes high 1-ms after VFB is within specified limits. Power bad (terminal goes low) is within 10 µs.
PGOOD2	11	O	
SKIPSEL	32	I	Skip and fault mode selection pin. Refer to Table 2
TONSEL	31	I	On-time selection pin. Refer to Table 1 and Table 2.
V5FILT	20	I	5-V supply input for the entire control circuit. Should be provided from VREG5 via RC filter.
VBST1	28	I	Supply Input for High-side MOSFET Driver. Connect capacitor from this pin to respective LL terminal. An internal PN diode is connected between VREG5 to each of these pins. User can add external schottky diode if forward drop is critical to drive the power MOSFET.
VBST2	13	I	
VFB1	3	I	SMPS feedback input. Connect the feedback resistor divider here for adjustable outputs. Tie these pins to V5FILT or for fixed output option. Refer to Table 2
VFB2	6	I	
VIN	22	I	Supply Input for 5-V and 3.3-V linear regulator. Typically connected to VBAT.
VO1	1	I	These terminals serve four functions: on-time adjustment, output discharge, VREG5, VREG3 switchover input and feedback inputs for 5-V, 3.3-V fixed-output option. Connect to positive terminal of respective switch mode power supply's output capacitor.
VO2	8	I	
VREF2	4	O	2-V reference output. Capable of ±50-µA, ±2% over 0 - 85°C temperature range. Bypass to GND by 1-nF ceramic capacitor. Tie this pin to GND disables both SMPS.
VREG3	19	O	3.3-V, 100-mA low dropout linear regulator output. Bypass to PGND by 10-µF ceramic capacitor. Runs from VIN supply. Shuts off with EN3. Switches over to VO2 when 3.1 V or above is provided.
VREG5	21	O	5-V, 100-mA low dropout linear regulator output. Bypass to PGND by 10-µF ceramic capacitor. Runs from VIN supply. Internally connected to VBST and DRVL. Shuts off with EN5. Switches over to VO1 when 4.8 V or above is provided.

QFN PACKAGE
(BOTTOM VIEW)



BLOCK DIAGRAM (One Channel Only Shown)



DETAILED DESCRIPTION

PWM Operation

The switching mode power supply (SMPS) block of TPS51120 supports an adaptive on time control pulse-width-modulation (PWM). Switching frequency is selectable from four choices for maximum efficiency (5 V/180 kHz, 3.3 V/270 kHz), minimum component size (5 V/380 kHz, 3.3 V/580 kHz) or the other two intermediates. The TPS51120 supports both true current mode control and D-CAP™ mode control, selectable up to the requirements from system design. All N-channel MOSFET totem-pole architecture is employed for external switches. The synchronous top (high-side) MOSFET is turned on, or is "SET", at the beginning of each cycle. This MOSFET is turned off, or is "RESET" after a constant "on-time" period which is defined by the frequency of customer's choice and input and output voltage ratio. The top MOSFET is turned on again if inductor current is reduced to meet both conditions of,

1. the current level corresponds to the error amount of output voltage and,
2. below the overcurrent limit level

Repeating operation in this manner, the controller regulates the output voltage. The synchronous bottom (low-side) or the rectifying MOSFET is turned on each cycle in the negative phase to the top MOSFET to keep the conduction loss minimum. The rectifying MOSFET turns off on the event reverse inductor current flow is detected. This enables seamless transition to skip mode function so that high efficiency is kept over a broad range of load current. At the beginning of the soft start period, the rectifying MOSFET remains in the off state until the top MOSFET is turned on for at least once.

Current Mode

The current mode scheme is a sequence of feedback control described as follows. The output voltage is monitored at the middle point of voltage divider resistors and fed back to a transconductance amplifier. The amplifier outputs target current level proportional to error amount between the feedback voltage and the internal 1 V reference voltage. The inductor current level is monitored during the off-cycle, when rectifying MOSFET is turned on. The PWM comparator compares the inductor current signal with this target current level that is indicated at the COMP pin voltage. When both signals are equal (at the valley of the current sense signal), the comparator provides the "SET" signal to the gate driver latch. The current mode option has relatively higher flexibility by the external compensation network provided to the COMP pin. And it is suitable for lowest ripple design with output capacitor(s) having ultra-low ESR. More detail information about loop compensation and parameter design can be found in the *Loop Compensation and External Parts* section. When sensing the inductor current, accuracy and cost always trades off. In order to give the circuit designer a choice between these two, TPS51120 supports both of external resistor sensing and MOSFET $R_{DS(on)}$ sensing. Please contact factory for current mode EVM with R_{SENSE} capability.

D-CAP™ Mode

The D-CAP™ mode operation is enabled by tying the COMP pin to V5FILT. In this mode, the PWM comparator monitors the feedback voltage directly and compares the voltage with the internal 1-V reference. When both signals are equal at the valley of the voltage sense signal, the comparator provides the "SET" signal to the top MOSFET gate driver. Because the compensation network is implemented on the part and the output waveform itself is used as the error signal, external circuit design is largely simplified. Another advantage of the D-CAP™ mode is its inherent fast transient response. A trade-off is a sufficient amount of ESR required in the output capacitor. SPCAP or POSCAP is recommended. The inductor current information is still used in the D-CAP™ mode for over current protection and light load operation. Do NOT neglect current sensing design in this mode. To summarize, the D-CAP™ mode is suitable for the lowest external component count with the fastest transient response, but with relatively large ripple voltage. It is easy to design the loop once appropriate output capacitor and inductor current ripple is selected. Please refer to loop compensation and parameter design in the *Loop Compensation and External Parts* section for more information.

DETAILED DESCRIPTION (continued)

Adaptive On-Time Control

The TPS51120 employs adaptive on time control scheme and does not have a dedicated oscillator on board. However, it works almost constant frequency over the entire input voltage range (pseudo-constant frequency) by feed-forwarding the input and output voltage into the on-time one-shot timer. The on-time is controlled inverse proportional to the input voltage and proportional to the output voltage so that the duty ratio is kept as V_{OUT}/V_{IN} technically with the same cycle time. The input voltage monitoring is accomplished through sensing the LL node, not at VIN node, during the 'ON' state. This eliminates the influence of the voltage drop across the top MOSFET to the frequency especially in heavy load condition. The VIN pin is not used for the on-time control but used only for the 5 V and 3.3 V regulators' supply. The switching frequency is selectable from four combinations shown in the table below by setting TONSEL pin voltage. This allows the system design to pursue highest efficiency (5 V/180 kHz, 3.3 V/270 kHz), smallest components size (5 V/380 kHz, 3.3 V/580 kHz) or a good balance of both in the medium. Also shown in the table are the typical on-time for each frequency and 5 V, 3.3 V outputs at VIN=12. Output voltage feed-forward is enabled after the output voltage exceeds 1.0 V in order to achieve stable start up.

Table 1. Frequency Selection and Typical On-Time

TONSEL CONNECTION	CH1(LL1=VIN=12 V)		CH2 (LL2=VIN=12 V)	
	FREQUENCY (kHz)	ON-TIME @ 5 V (ns)	FREQUENCY (kHz)	ON-TIME @ 3.3 V (ns)
V5FILT	180	2340	270	1030
FLOAT (OPEN)	220	1950	330	850
VREF2	280	1490	430	650
GND	380	1111	580	480

Programming Table

The TPS51120 has varieties of configurations choice. It is important to tailor appropriately with regard to the system design requirements. Table below shows programming table for the control scheme selection, frequency selection, output voltage selection and skip selection. Faults-off disables UVP, OVP and UVLO. This is mainly intended for debugging purpose. Enable states and possible connections for the LDO's EN3, EN5 pins and SMPS's EN1, EN2 pins are also shown.

Table 2. Function Programming Table

PIN	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current Mode (apply R-C network)	D-CAP™ Mode
TONSEL (CH1/CH2) [kHz]	380 / 580	280 / 430	220 / 330	180 / 270
VFB1	Adjustable output (connect to the resistor divider)			5V fixed output
VFB2	Adjustable output (connect to the resistor divider)			3.3 V fixed output
SKIPSEL	AUTO-SKIP	AUTO-SKIP (FAULTS OFF)	PWM	PWM
EN1, EN2	Switcher Off	Not used	Switcher on	Switcher on
EN3, EN5	LDO Off	Not used	LDO on	LDO on (EN3 only)

DETAILED DESCRIPTION (continued)

Light Load Operation

TPS51120 automatically reduces switching frequency at light load condition to maintain high efficiency. This reduction of frequency is achieved smoothly and without an increase in load regulation. Detail operation is described as follows. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its 'valley' touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when this zero inductor current is detected. The on-time is kept the same as that in the heavy load condition. As the load current further decreases, the converter runs in discontinuous conduction mode and it takes longer and longer to discharge the output capacitor to the level that requires next 'ON' cycle. This results in reducing the switching frequency. In reverse, when the output current increases from light load to heavy load, switching frequency increases to the constant predetermined frequency as the inductor current reaches to the continuous conduction. The transition load point to the light load operation $I_{OUT(LL)}$ (i.e. the threshold between continuous and discontinuous conduction mode) can be calculated as shown in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f} \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}} \quad (1)$$

where f is the PWM switching frequency which is determined by TONSEL pin. Switching frequency versus output current in the light load condition is a function of L, f, V_{IN} and V_{OUT}, but it decreases almost proportional to the output current from the $I_{OUT(LL)}$ given in Equation 1.

Forced PWM Operation

Tying SKIPSEL to V5FILT or leaving it float force the part to operate in continuous conduction mode for entire load range by disabling zero inductor current detection. Switching frequency is kept at the frequency selected by TONSEL input. System designers may want to use this mode to avoid certain frequency in light load condition with the cost of low efficiency. However, please be aware the output has a capability to both sink and source current in this mode. If the output terminal is connected to a voltage source higher than the regulated voltage, the converter sinks current from the output and boosts the charge into the input capacitor. This may cause unexpected high voltage at VIN and may damage the part.

5V, 100 mA, LDO and Switchover (VREG5)

A 5-V, 100-mA linear regulator is integrated in the TPS51120. This low drop-out (LDO) regulator services the main analog supply rail for the IC and provides the current for the gate drivers. The regulator is a PMOS type with transconductance control and the pole is determined by the value of output capacitance. Typically, the value of this capacitor must be greater than 4.7 µF. A 10-µF ceramic capacitor is recommended for a typical design. Current limit and thermal protection are included in the regulator. Additionally, if the VO1 voltage exceeds 4.8 V, then the regulator is switched off and the 5V rails are bootstrapped to the 5-V switcher output, improving the efficiency of the converter. A glitch-free switchover is accomplished. The VREG5 output voltage does not show a short "glitch" down to 4.8 V when this bootstrapping action is taken. The switchover impedance from VO1 to VREG5 is typically 1.3 Ω. Standby current is designed for 30-µA operation allowing the user to leave the regulator alive while maintaining maximum battery life. The EN5 pin is a high voltage input and can be tied to VBAT or left open to enable the 5-V regulator. This 5-V regulator must be enabled prior to enable switching regulators. Pull EN5 to ground to shut off the regulator. Disabling the regulator does not promise shutting down the switchers once 5 volts is supplied via the bootstrap path. Because switchover occurs, the 5-V switcher MUST be turned off with the LDO in order to shut down the device. EN5 does NOT function as a master disable.

DETAILED DESCRIPTION (continued)

3.3V, 100 mA, LDO and Switchover (VREG3)

A 3.3-V, 100-mA linear regulator is integrated as a second regulator in the TPS51120. This LDO provides a handy standby supply for 3.3 V 'Always On' voltages in the notebook system. The characteristics of this LDO are identical to the 5V LDO except for the switchover voltage. Apply 10-µF ceramic capacitor from VREG3 to PGND in adjacent to the device. If the VO2 voltage exceeds 3.1 V, then this regulator is switched off and the 3.3 V rail is bootstrapped to the 3.3 V switcher. Note if the VO2 voltage is set higher by external feedback dividers, for example 5 V, that high voltage is presented at VREG3 after switchover. The EN3 pin is a low voltage input that can be tied to V5FILT or left open to enable the 3.3-V regulator. This 3.3-V regulator can be turned on or kept alive independent to the 5-V regulator.

2V, 50 µA Sink/Source Reference (VREF2)

This is a handy reference for generating auxiliary voltages. The tolerance is ±2% over 50-µA load and 0°C to 85°C ambient temperature ranges. The four-state logic (SKIPSEL, TONSEL) takes advantage of this reference for additional selection modes. This reference is enabled when both EN3 and EN5 become high, shuts down after both switchers are turned off and VREG5 or VREG3 is shut down. Please refer to Table 4. If this output is forcibly tied down to ground, both SMPS are turned off without latch. Bypass VREF2 pin to GND by a 1-nF capacitor.

Low-Side Driver

The low-side gate driver, DRVL, is designed to drive high current low $R_{DS(on)}$ N-channel MOSFET(s). The maximum drive voltage is 5.5 V which is delivered from VREF5 pin. The instantaneous drive current is supplied from the output capacitor at the VREF5 pin. The average drive current is equal to the FET's gate charge at VGS=5 V times switching frequency. The VREG5 pin voltage may contain high frequency noise due to parasitic inductance by wiring and pointing current flow into the gate capacitor. The drive capability is represented by its internal resistance, which are 3.5 Ω for VREG5 to DRVL and 1.5 Ω for DRVL to PGND. Adaptive dead time control generates delay times between top MOSFET off to bottom MOSFET on, and bottom MOSFET off to top MOSFET on, preventing the totem-pole switches to shoot through. Top MOSFET off is detected as LL-node voltage declining below 2 V. Bottom MOSFET off is detected as DRVL voltage become 1.1 V.

High-Side Driver

The high-side gate driver, DRVH, is designed to drive high current, low $R_{DS(on)}$ N-channel MOSFET(s). When configured as a LL-node referenced floating driver, connect 0.1-µF ceramic capacitor between corresponding VBST pin and LL pin. A 5-V bias voltage is delivered from VREG5 supply. VBST is internally connected to VREG5 through a high voltage PN diode. This internal diode provides sufficient gate voltage for ordinary 4.5-V drive power MOSFETs and helps reducing external component. However, in the case where the gate bias voltage is critical for driving the top MOSFET, application designer may add an external schottky diode from VREG5 pin to VBST pin. Note schottky diodes have quite high reverse leakage current at high temperature. The instantaneous drive current is supplied by the flying capacitor connected between VBST and LL pins. The average drive current is equal to the gate charge at VGS=5 V times switching frequency. The drive capability is represented by its internal resistance, which are 3.5-Ω for VBST to DRVH and 1.5Ω for DRVH to LL. The maximum recommended voltage that can be applied between DRVH pin and LL pin is 5.5 V, DRVH pin to PGND pin is 34 V.

Soft-Start

The TPS51120 has an internal 3-ms voltage-servo soft start for each channel. When the EN1 or EN2 pin exceeds 0.9 V, an internal DAC begins ramping up the reference voltage. Smooth control of the output voltage during start up is maintained. However, if a slower soft-start is required, an external capacitor may be tied from the EN1 or EN2 pin to GND. In this case, the TPS51120 charges the external capacitor with the integrated 2-µA current source. The lower of either the EN voltage slew rate or the internal soft start slew rate dominates the start-up ramp. In addition, if tracking discharge is required, the EN pin can be used to control the output voltage discharge smoothly. An approximate value for the soft start reference voltage as a function of EN voltage is $V_{SSREF} = (V_{ENX} – 0.9)/1.5 < 1$ V. At the beginning of soft-start period, the rectifying MOSFET maintains an off state until the top MOSFET is turned on for at least once. This prevents high negative current to flow back from the output capacitor in the event of output capacitor pre-charged condition.

DETAILED DESCRIPTION (continued)

Soft-Stop

Discharge mode or 'Soft Stop' is always on during Faults or Disable. In this mode, an event that would cause the switcher to be turned off (EN1 or EN2 low, OVP, UVP, UVLO) causes the output to be discharged through 10-Ω transistor inside the VO terminal. The external rectifying MOSFET is not turned on for the soft off operation to avoid a chance to cause negative voltage at the output. Soft-stop time constant is a function of the output capacitance and the resistance of the discharge transistor. This discharge ensures that, upon restart, the regulated voltage always starts from zero volts. In case a SMPS is restarted before discharge completion, soft-stop is terminated and the switching resumes after the reference level comes back to the remaining output voltage.

Powergood

The TPS51120 has dedicated powergood output for each SMPS, PGOOD1 and PGOOD2. The PGOOD monitors are open drain 5-mA pull down outputs. These outputs are low on startup and stay low until the switcher feedback voltages are within a specified range for 256 clocks or approximately 1 ms. If the VFB pin falls outside the 10% tolerance band, the respective PGOOD pin goes low within microseconds. Then if the VFB pin comes back within 5% of target (1 V) for greater than 1 ms, then the respective PGOOD pin goes high again. The PGOOD pin should be typically pulled up through a 100 kΩ or greater value resistor to the V5FILT pin. Both PGOOD pins go low during fault conditions (Thermal Shutdown, UVLO, UVP, OVP) and Disable.

Current Sensing and Overcurrent Protection

The SMPS has cycle-by-cycle over current limiting. The inductor current is monitored during the rectifying MOSFET is on and the controller does not allow the next ON cycle while the current level is above the trip threshold. In order to provide good accuracy and cost effective solution, TPS51120 supports both of external resistor sensing and MOSFET $R_{DS(on)}$ sensing which are selected by CS terminal connection. For resistor sensing scheme, an appropriate current sensing resistor should be connected between the source terminal of the bottom MOSFET and PGND. CS pin is connected to the bottom MOSFET source terminal node. The inductor current is monitored by the voltage between PGND pin and CS pin. In this scheme, the trip level is fixed value of 80 mV. For $R_{DS(on)}$ sensing scheme, CS terminal is connected to V5FILT through a trip voltage setting resistor R_{TRIP}. In this scheme, CS terminal sinks 10-μA I_{TRIP} current and the trip level is set to the voltage across the R_{TRIP}. The trip level should be in the range of 30 mV to 150 mV. This allows designer to select a variety of MOSFETs for the bottom arm. The inductor current is monitored by the voltage between PGND pin and LL pin so that LL pin should be connected to the drain terminal of the bottom MOSFET. I_{TRIP} has 4500ppm/°C temperature slope, with respect to its 25°C value, to compensate the temperature dependency of the $R_{DS(on)}$. In either scheme, PGND is used as the positive current sensing node so that PGND pin should be connected to the proper current sensing device, i.e. the sense resistor or the source terminal of the bottom MOSFET. In an overcurrent condition, since the current to the output capacitor is limited while the load drags more, the output voltage tends to go down. It ends up with passing into the undervoltage protection and latches off as both DRVH and DRVL are at low level.

Table 3. Current Sensing Connection

	CS	Threshold	Temperature Coefficient (ppm/°C)
$R_{DS(on)}$ sensing	V5FILT	$I_{TRIP} \times R_{TRIP} / R_{DS(on)}$	4500
R_{SENSE} sensing	Bottom FET source node (=R_{SENSE} (-) node)	80 mV / R_{SENSE}	none

Overvoltage Protection

For over voltage protection (OVP), the TPS51120 monitors VFB voltage. When the VFB voltage is higher than 115% of the target, the OVP comparator output goes high and the circuit latches both switchers. The offending channel is latched DRVH low and DRVL high, the other channel is simply latched as DRVH and DRVL at low. Be aware negative voltage may appear at the output terminal of the offending channel because of LC resonant configured by the power inductor and the output capacitor. The system designer is responsible to this negative voltage if any protection is need. The OVP propagation delay is less than 3 μs.

DETAILED DESCRIPTION (continued)

Undervoltage Protection

For under voltage protection (UVP), the TPS51120 monitors VFB voltage. When the VFB voltage is lower than 70% of the target and the UVP comparator output goes high, the internal UVP delay counter begins count. After the 128 clocks, approximately 0.5 ms, TPS51120 latches off both channels as DRVH and DRVL at low. This function is enabled after the softstart reference has exceeded the internal 1-V reference operation to ensure startup. Please refer to Table 5.

5V Supply and UVLO Protection

TPS51120 has two 5-V terminals. VREG5 is the output of 5-V linear regulator. This terminal also serves as input pin for the gate driver circuits. Internal switchover FET is connected between this pin and VO1. V5FILT is the V_{CC} supply input for the control circuitry on the chip. Connect with R-C low pass filter from VREG5 to this V5FILT to eliminate spiky high frequency noise. State definition pins such as SKIPSEL, TONSEL, VFB (fixed output case) and COMP (for D-CAP mode) or CS resistors that need stable 5V should refer to V5FILT. The part has 5-V supply under voltage lock out protection (UVLO) to prevent unpredictable operation under insufficient power. The TPS51120 monitors VREG5 voltage. When the VREG5 voltage is lower than UVLO threshold, the SMPS's are shut off. The output discharge or 'soft stop' feature is enabled for the channel one and channel two. However, because the discharge circuit derives its power from the 5-V line, power must be presented long enough to ensure that discharge is complete during shutdown. Also, during power up, the TPS51120 attempts to discharge the output capacitor until the UVLO (on) threshold is reached. A 5-V UVLO is non-latch protection and is automatically resumed up on 5-V recovery.

VIN Line Sag protection (Dynamic UVP)

Since the TPS51120 serves primarily as system power (i.e. used for generating 3.3 V and 5 V) it is very important that the system not enter UVP if the VIN supply has dropped below 6V. UVP would be caused by the 5-V output dropping due to input line sag. When the VIN pin drops below the 5-V regulator voltage, the 5-V regulator 'tracks' VIN (LDO operation). The UVP threshold is adjusted downward when the VREG5 is below 4.8 V. This ensures that 5-V supply UVLO trips before the latching UVP condition occurs and the system power can recover normally when VIN recovers. This feature is very useful for transient VIN events such as adapter insertion

Thermal Shutdown

The TPS51120 employs thermal shutdown for the switchers at 145°C. This is a non-latch protection with hysteresis of 10°C. Both switching regulators and both internal regulators stop. VREG5 and VREG3 LDOs may not turn on if the part is preheated above the recovery temperature before starting up. Reduce the temperature to or below T_A = 85°C to resume operation safely.

Table 4. Enable Logic States (VOUT1=5 V, VOUT2=3.3 V)

EN5(1)	EN3	EN1	EN2	VREG5	VREG3	VREF2(2)	SMPS1	SMPS2
Low	Low	High or Low	High or Low	Off	Off	Off	Off	Off
Low-to-High	Low	High or Low	High or Low	LDO 5 V	Off	Off	Off	Off
Low	Low-to-High	High or Low	High or Low	Off	LDO 3.3 V	Off	Off	Off
Low-to-High	Low-to-High	Low	Low	LDO 5 V	LDO 3.3 V	On	Off	Off
High	High	Low	Low-to-High	LDO 5 V	SW 3.3 V	On	Off	On
High	High	Low-to-High	Low	SW 5 V	LDO 3.3 V	On	On	Off
High	High	High	High	SW 5 V	SW 3.3 V	On	On	On
High-to-Low	High-to-Low	High	High	SW 5 V	SW 3.3 V	On	On	On
High	High	High-to-Low	High-to-Low	LDO 5 V	LDO 3.3 V	On	Off	Off
High-to-Low	High	High-to-Low	High	Off	LDO 3.3 V	Off	Off	Off
High	High-to-Low	High	High-to-Low	SW 5 V	Off	On	On	Off

(1) Because of Switch-over, the 5-V switcher MUST be turned off with the LDO in order to shut down the device. EN5 does NOT function as a master DISABLE.
(2) Forcing VREF2 output to ground disables SMPS1 and SMPS2 without latch.

DETAILED DESCRIPTION (continued)

Table 4. Enable Logic States (VOUT1=5 V, VOUT2=3.3 V) (continued)

EN5(1)	EN3	EN1	EN2	VREG5	VREG3	VREF2(2)	SMPS1	SMPS2
High	High-to-Low	Low	High-to-Low	LDO 5 V	Off	Off	Off	Off
High-to-Low	High	Low	Low	Off	LDO 3.3 V	Off	Off	Off
High	High-to-Low	Low	Low	LDO 5 V	Off	Off	Off	Off

DETAILED DESCRIPTION (continued)

Table 5. Protection States (VOUT1 = 5 V, VOUT2 = 3.3 V)

	DRVH1	DRVL1	DRVH2	DRVL2	PGOOD1 PGOOD2	VREG5	VREG3	VREF2	FOR RESTART
UVPch1	Low	Low	Low	Low	Low/Low	LDO 5 V	LDO 3.3 V	On	Toggle EN1
UVPch2	Low	Low	Low	Low	Low/Low	LDO 5 V	LDO 3.3 V	On	Toggle EN2
OVPch1	Low	High	Low	Low	Low/Low	LDO 5 V	LDO 3.3 V	On	Toggle EN1
OVPch1	Low	Low	Low	High	Low/Low	LDO 5 V	LDO 3.3 V	On	Toggle EN2
Thermal SHDN	Low	Low	Low	Low	Low/Low	Off	Off	Off	Lower Package Temperature
VIN < 5.0	Normal	Normal	Normal	Normal	Low/Normal	SW 5 V	SW 3.3 V	On	Raise VIN
VREG UVLO	Low	Low	Low	Low	Low/Low	LDO but dropping	LDO 3.3 V	On	Raise VIN, Reduce 5V current
OCPch1	Limited Duty	Estended Duty	Normal	Normal	Low/Normal	LDO 5 V	SW 3.3 V	On	Reduce CH1 Current
OCPch2	Normal	Normal	Limited Duty	Estended Duty	Normal/Low	SW 5 V	LDO 3.3 V	On	Reduce CH2 Current
EN1 Low	Low	Low	Normal	Normal	Low/Normal	LDO 5 V	SW 3.3 V	On	Float or tie to VREG5
EN2 Low	Normal	Normal	Low	Low	Normal/Low	SW 5 V	LDO 3.3 V	On	Float or tie to VREG5
EN1, EN2, EN3 Low	Low	Low	Low	Low	Low/Low	LDO 5 V	Off	Off	Float EN3, then float EN1,2 or tie to VREG5
EN5, EN1 Low	Low	Low	Low	Low	Low/Low	Off	LDO 3.3 V	Off	Float EN5 or tie to VBAT, tie EN1 to VREG5

Loop Compensation and External Parts Selection

Current Mode Operation

A buck converter using TPS51120 current mode operation can be partitioned into three portions, a voltage divider, an error amplifier and a switching modulator. By linearizing the s witching modulator, we can derive the transfer function of the whole system. Since current mode scheme directly controls the inductor current, the modulator can be linearized as shown in Figure 1.

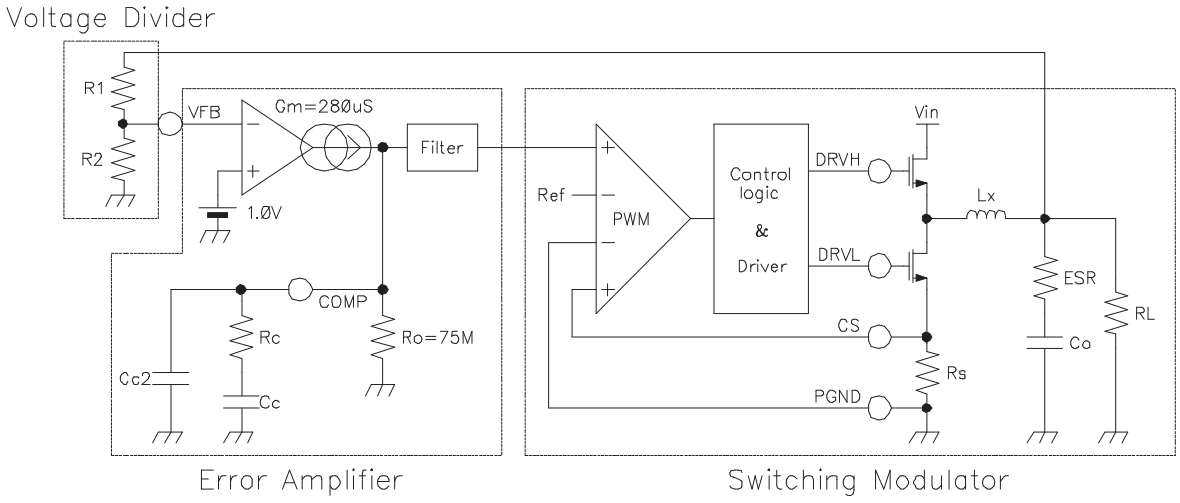


Figure 1. Linearizing the Modulator

Here, the inductor is located inside the local feedback loop and its inductance does not appear in the small signal model. As a result, a modulated current source including the power inductor can be modeled as a current source with its transconductance of $1/R_S$ and the output capacitor represent the modulator portion. This simplified model is applicable in the frequency space up to approximately a half of the switching frequency. One note is, although the inductance has no influence to small signal model, it has influence to the large signal model as it limits slew rate of the current source. This means the buck converter's load transient response, one of the large signal behaviors, can be improved by using smaller inductance without affecting the loop stability.

Total open loop transfer function of the whole system is given by Equation 2.

$$H(s) = H_1(s) \times H_2(s) \times H_3(s) \tag{2}$$

Assuming RL>>ESR, R_O>>R_C and C_C>>C_C2, each transfer function of three block is shown in Equation 3 through Equation 5.

$$H_1(s) = \frac{R_2}{(R_2 + R_1)} \tag{3}$$

$$H_2(s) = -Gm \times \frac{R_O (1 + s \times C_C \times R_C)}{(1 + s \times C_C \times R_O)(1 + s \times C_{C2} \times R_C)} \tag{4}$$

$$H_3(s) = \frac{(1 + s \times C_O \times ESR)}{(1 + s \times C_O \times RL)} \times \frac{RL}{R_S} \tag{5}$$

There are three poles and two zeros in H(s). Each pole and zero is given by Equation 6 through Equation 10.

$$\omega_{P1} = \frac{1}{(C_C \times R_O)} \tag{6}$$

$$\omega_{P2} = \frac{1}{(C_O \times RL)} \tag{7}$$

$$\omega_{P3} = \frac{1}{(C_{C2} \times R_C)} \tag{8}$$

$$\omega_{Z1} = \frac{1}{(C_C \times R_C)} \tag{9}$$

$$\omega_{Z2} = \frac{1}{(C_O \times ESR)} \tag{10}$$

Usually, each frequency of those poles and zeros is lower than the 0 dB frequency, f_0. However, the f_0 should be kept under 1/3 of the switching frequency to avoid effect of switching circuit delay. The f_0 is given by next equation Equation 11.

$$f_0 = \frac{1}{2\pi} \times \frac{R2}{R1 + R2} \times \frac{Gm}{C_O} \times \frac{R_C}{R_S} = \frac{1}{2\pi} \times \frac{1.0}{V_{OUT}} \times \frac{Gm}{C_O} \times \frac{R_C}{R_S} \tag{11}$$

Based on small signal analysis above, the external components can be selected by following manner.

1. **Choose the inductor.**The inductance value should be determined to give the ripple current of approximately 1/4 to 1/2 of maximum output current.

$$L = \frac{1}{I_{IND(ripple)} \times f} \times \frac{(V_{IN(max)} - V_{OUT}) \times V_{OUT}}{V_{IN(max)}} = \frac{2}{I_{OUT(max)} \times f} \times \frac{(V_{IN(max)} - V_{OUT}) \times V_{OUT}}{V_{IN(max)}} \tag{12}$$

   The inductor also needs to have low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation. The peak inductor current can be estimated in Equation 13.

$$I_{IND(peak)} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{1}{L \times f} \times \frac{(V_{IN(max)} - V_{OUT}) \times V_{OUT}}{V_{IN(max)}} \tag{13}$$

2. **Choose rectifying (bottom) MOSFET.** When $R_{DS(on)}$ sensing scheme is selected, the rectifying MOSFET's on-resistance is used as this R_S so that lower $R_{DS(on)}$ does not always promise better performance. In order to clearly detect inductor current, minimum R_S recommended is to give 15 mV or larger ripple voltage with the inductor ripple current. This promises smooth transition from CCM to DCM or vice versa. Upper side of the $R_{DS(on)}$ is of course restricted by the efficiency requirement, and usually this resistance affects efficiency more at high load conditions. When using external resistor current sensing, there is no restriction for low $R_{DS(on)}$. However, the current sensing resistance R_S itself affects the efficiency.
3. **Choose output capacitor(s).** If organic semiconductor capacitors (OS-CON) or specialty polymer capacitors (SP-CAP), are used, the ESR to achieve required ripple value at a stable state or transient load condition determines the amount of capacitor(s) need, and capacitance is then enough to satisfy stable operation. The peak-to-peak ripple value can be estimated by ESR times the inductor ripple current for stable state, or ESR times the load current step for a fast transient load response. In case of ceramic capacitor(s), usually ESR is small enough to meet ripple requirement. On the other hand, transient undershoot and overshoot driven by output capacitance becomes the key factor to determine the capacitor(s).
4. **Determine f_0 and calculate R_C using Equation 14**. Note that higher R_C shows faster transient response in cost of unstableness. If the transient response is not enough even with high R_C value, try increasing the output capacitance. Recommended f_0 is f/4.

$$R_C \le 2\pi \times f_0 \times V_{OUT} \times \frac{C_O}{Gm} \times R_S \tag{14}$$

5. **Calculate C_{C2}.** The purpose of this capacitance is to cancel the zero caused by ESR of the output capacitor. If ceramic capacitor are used, there is no need for C_{C2}.

$$\omega_{z2} = \frac{1}{(C_O \times ESR)} = \omega_{p3} = \frac{1}{(C_{C2} \times R_C)} \tag{15}$$

$$C_{C2} = \frac{C_O \times ESR}{R_C} \tag{16}$$

6. **Calculate C_C.** Purpose of C_C is to cut DC component to obtain high DC feedback gain. However, as it causes phase delay, another zero to cancel this effect at f_0 frequency is need. This zero, ω_{z1}, is determined by C_C and R_C. Recommended ω_{z1} is 10 times lower to the f_0 frequency.

$$f_{z1} = \frac{1}{2\pi \times C_C \times R_C} = \frac{f_0}{10} \tag{17}$$

7. **In case of adjustable mode, determine the value of R1 and R2.** Recommended R2 value is from 10 kΩ to 20 kΩ. Determine R1 using Equation 18.

$$R_1 = (V_{OUT} - 1.0) \times R_2 \tag{18}$$

D-CAP™ Mode Operation

A buck converter system using D-CAP™ mode can be simplified as shown in Figure 2.

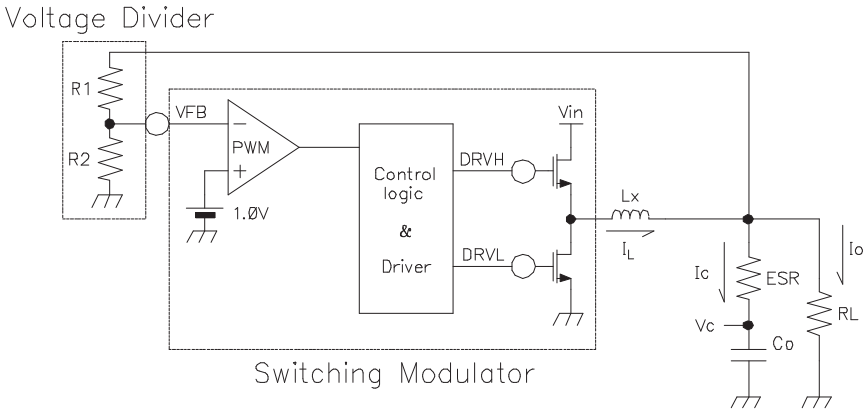


Figure 2. Linearizing the Modulator

The VO voltage is compare with internal reference voltage after divider resistors (Internal resistor mode. For adjustable mode, the comparison is directly at VFB). The PWM comparator determines the timing to turn on top MOSFET. The gain and speed of the comparator is high enough to keep the voltage at the beginning of each on cycle (or the end of off cycle) substantially constant. The DC output voltage may have line regulation due to ripple amplitude that slightly increases as the input voltage increase.

For the loop stability, the 0-dB frequency, f_0, defined below need to be lower than 1/3 of the switching frequency.

$$f_0 = \frac{1}{2\pi \times ESR \times C_O} \le \frac{f_{SW}}{3} \tag{19}$$

As f_0 is determined solely by the output capacitor's characteristics, loop stability of D-CAP™ mode is determined by the capacitor's chemistry. For example, specialty polymer capacitors (SP-CAP) have Co in the order of several 100 µF and ESR in range of 10 mΩ. These produce an f_0 in the order of 100 kHz or less and the loop is stable. However, ceramic capacitors have f_0 at more than 700 kHz, which is not suitable for this operational mode.

Although D-CAP™ mode provides many advantages such as ease-of-use, minimum external components configuration and extremely short response time, due to not employing an error amplifier in the loop, sufficient amount of feedback signal needs to be provided by external circuit to reduce jitter level. The required signal level is approximately 15 mV at comparing point, either the internal or external VFB voltages. The output capacitor's ESR should meet this requirement.

The external components selection is much simple in D-CAP™ mode.

1. **Choose inductor based on frequency and acceptable ripple current**.
2. **Choose output capacitor(s)**.Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended. Determine ESR to meet required ripple voltage above. A quick approximation is shown in Equation 20.

$$ESR = \frac{V_{OUT} \times 0.015}{I_{RIPPLE}} \tag{20}$$

Layout Considerations

Certain points must be considered before starting a layout work using the TPS51120.

- Connect RC low-pass filter from VREG5 to V5FILT, 1 µF and 5.1 Ω are recommended. Place the filter capacitor close to the device, within 12 mm (0.5 inches) if possible.
- VREG5 and VREG3 require at least 4.7 µF, VREF2 requires a 1-nF ceramic bypass capacitor which should be placed close to the device and traces should be no longer than 10 mm.
- Connect the overcurrent setting resistors from CSx to V5FILT (NOT VREG5) and close to the device, right next to the device if possible. The trace from CSx to V5FILT should avoid coupling to high-voltage switching node.
- In the case of using adjustable output voltage with an external resistor divider, the discharge path (VOx) should have a dedicated trace to the output capacitor; separate from the output voltage sensing trace, and use 1.5 mm or wider trace with no loops. Make the feedback current setting resistor (the resistor between VFBx to GND) is tied close to the device's GND. Place on the component side and avoid vias between this resistor and the device.
- Connections from the drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use 0.65 mm (25 mils) or wider trace.
- All sensitive analog traces and components such as VOx, COMPx, VFBx, VREF2, GND, ENx, PGOODx, CSx, V5FILT, TONSEL and SKIPSEL should be placed away from high-voltage switching nodes such as LLx, DRVLx or DRVHx nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback trace from power traces and components.
- Gather ground terminal of VIN capacitor(s), V_{OUT} capacitor(s) and source of low-side MOSFETs as close as possible. GND (signal ground) and PGNDx (power ground) should be connected strongly together near the device. PCB trace defined as LLx node, which connects to source of high-side MOSFET, drain of low-side MOSFET and high-voltage side of the inductor, should be as short and wide as possible.
- In order to effectively remove heat from the package, prepare thermal land and solder to the package's thermal pad. Three by three or more vias with a 0.33-mm (13mils) diameter connected from the thermal land to the internal ground plane should be used to help dissipation. Do NOT connect PGNDx to this thermal land underneath the package.

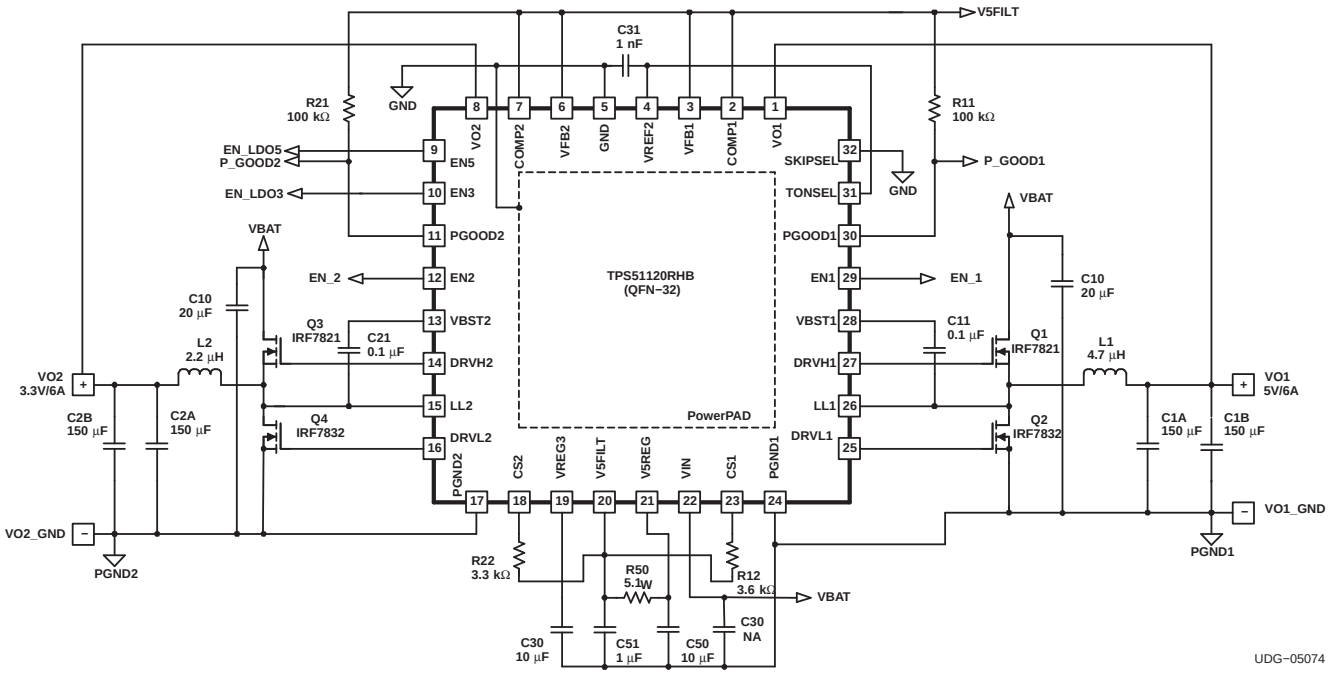


Figure 3. D-CAP™ Mode, Fixed 5-V/6-A, +3.3-V/6-A, $R_{DS(on)}$ Sensing

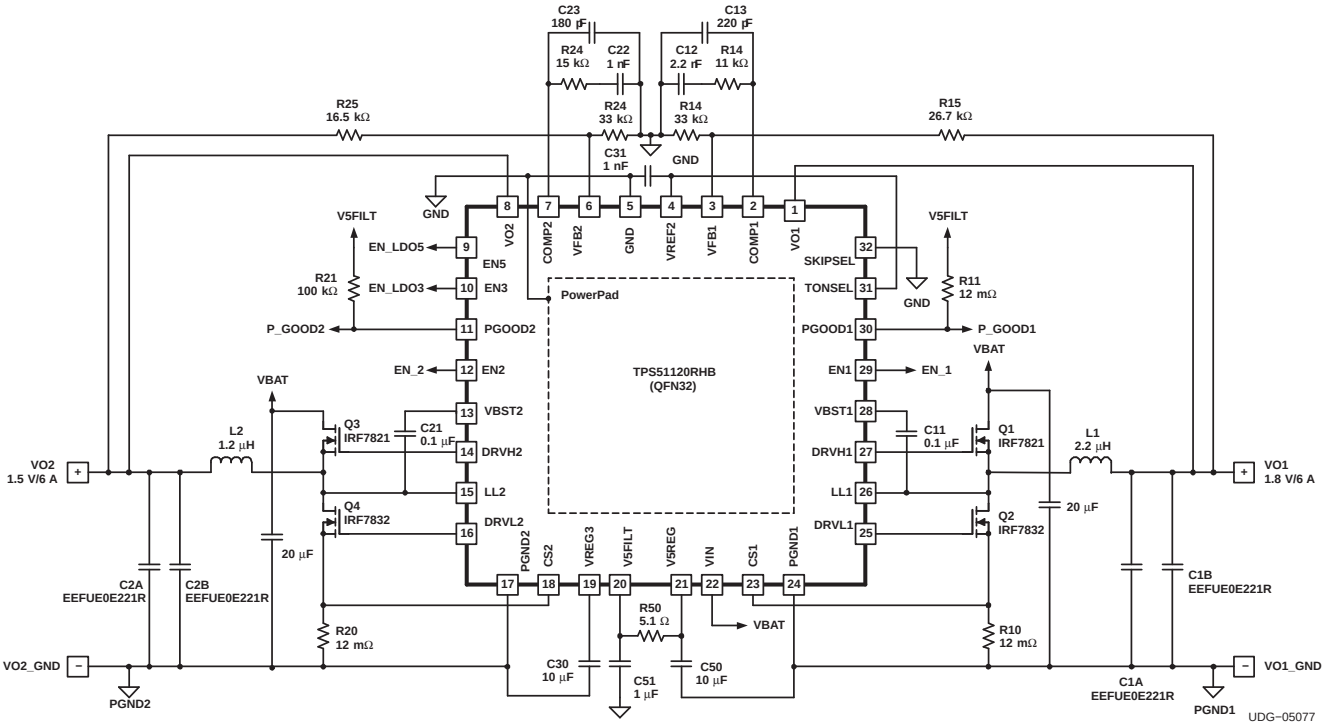


Figure 4. Current Mode, External 1.8-V/6-A, +1.5-V/6-A, R_{SENSE} Sensing

TYPICAL CHARACTERISTICS

VIN SUPPLY CURRENT vs JUNCTION TEMPERATURE

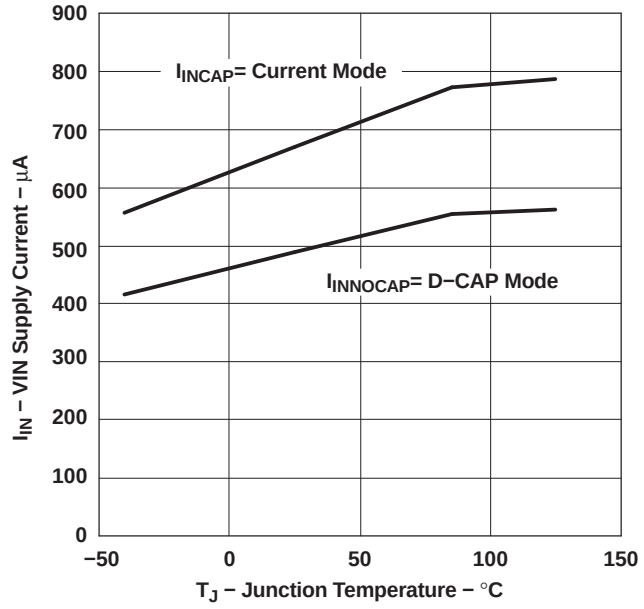


Figure 5.

VIN SUPPLY CURRENT vs INPUT VOLTAGE

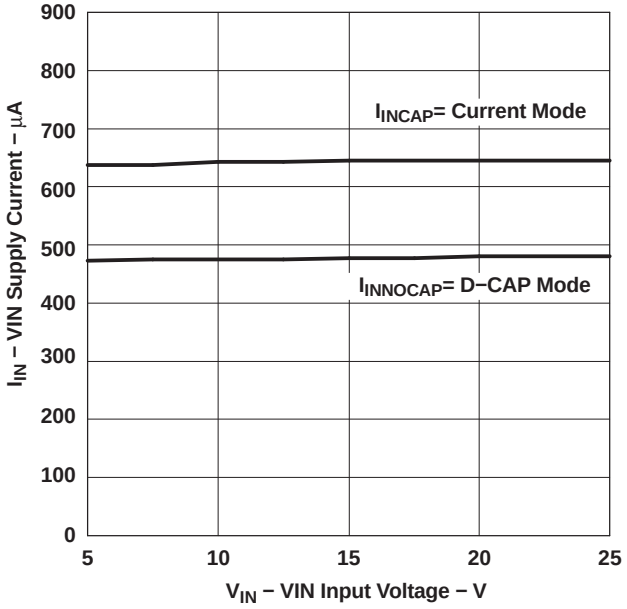


Figure 6.

TYPICAL CHARACTERISTICS (continued)

VIN STANDBY CURRENT
vs
JUNCTION TEMPERATURE

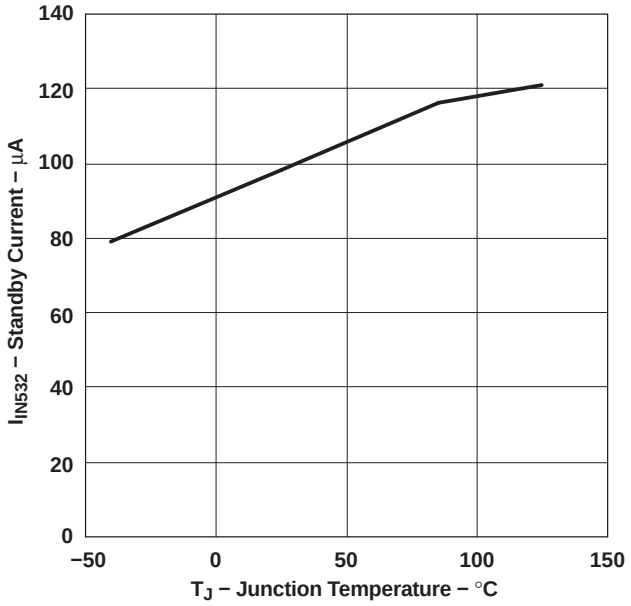


Figure 7.

VIN STANDBY CURRENT
vs
INPUT VOLTAGE

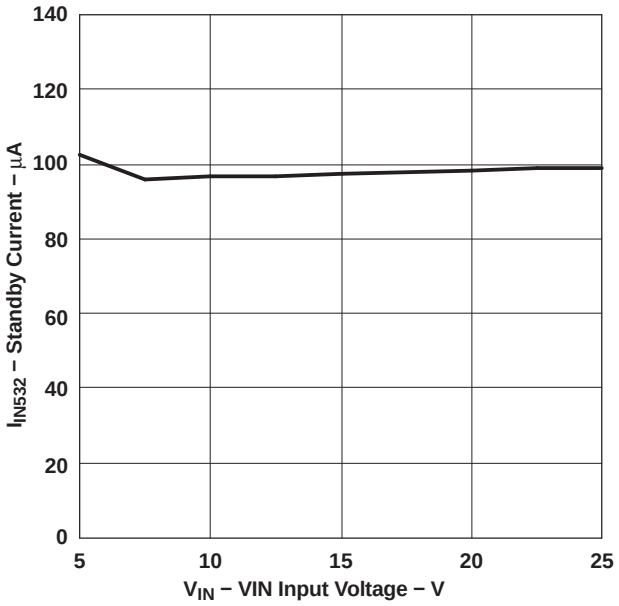


Figure 8.

VIN SHUTDOWN CURRENT
vs
JUNCTION TEMPERATURE

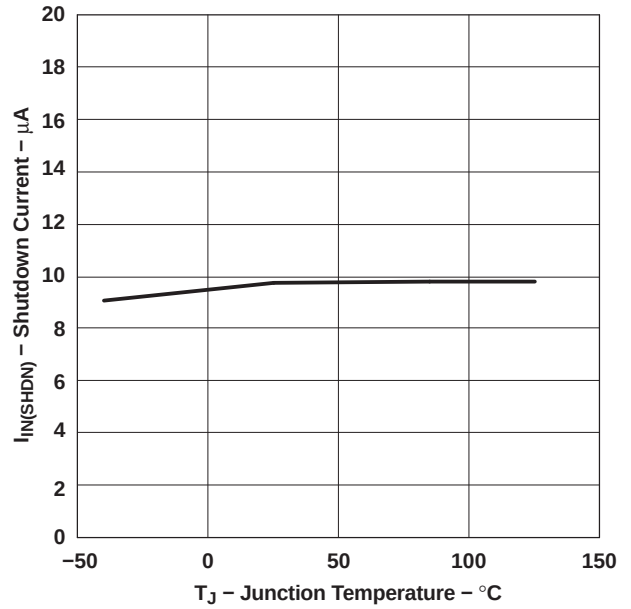


Figure 9.

VIN SHUTDOWN CURRENT
vs
INPUT VOLTAGE

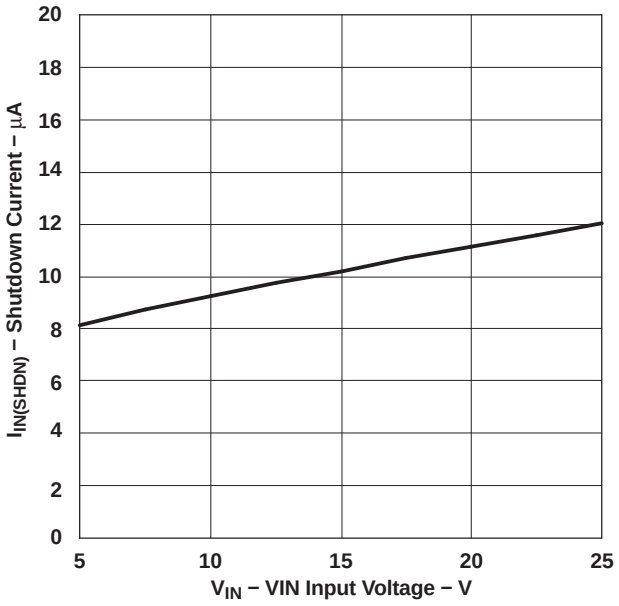


Figure 10.

TYPICAL CHARACTERISTICS (continued)

NO-LOAD BATTERY CURRENT vs INPUT VOLTAGE

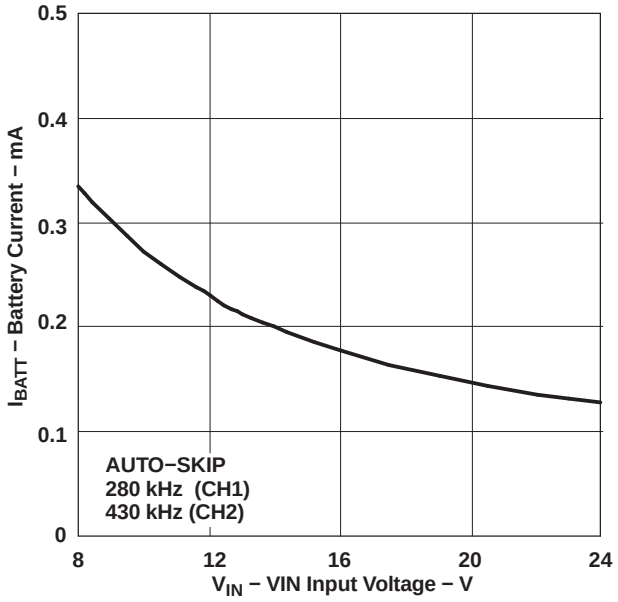


Figure 11.

CURRENT SENSE CURRENT vs JUNCTION TEMPERATURE

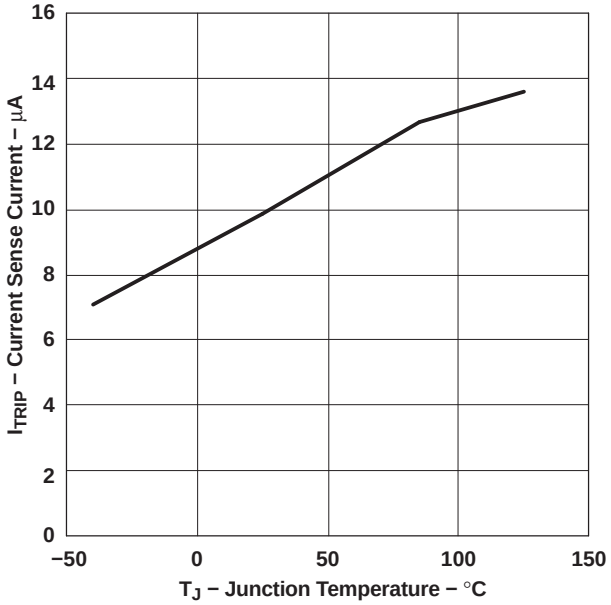


Figure 12.

SWITCHING FREQUENCY vs INPUT VOLTAGE

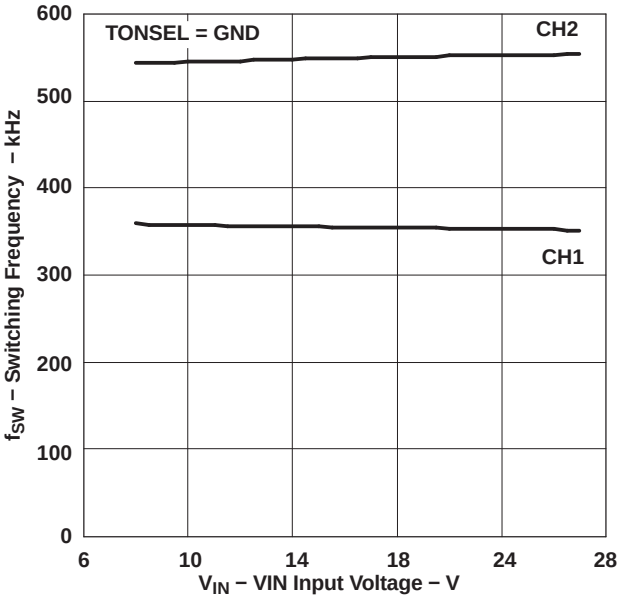


Figure 13.

SWITCHING FREQUENCY vs INPUT VOLTAGE

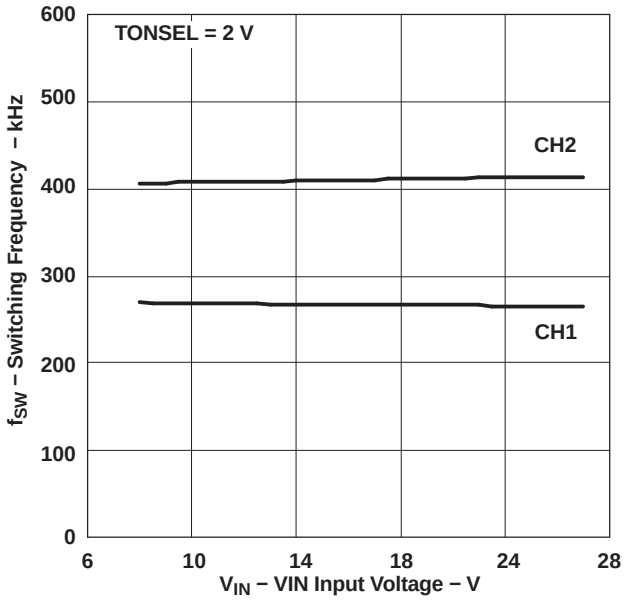


Figure 14.

TYPICAL CHARACTERISTICS (continued)

SWITCHING FREQUENCY
vs
INPUT VOLTAGE

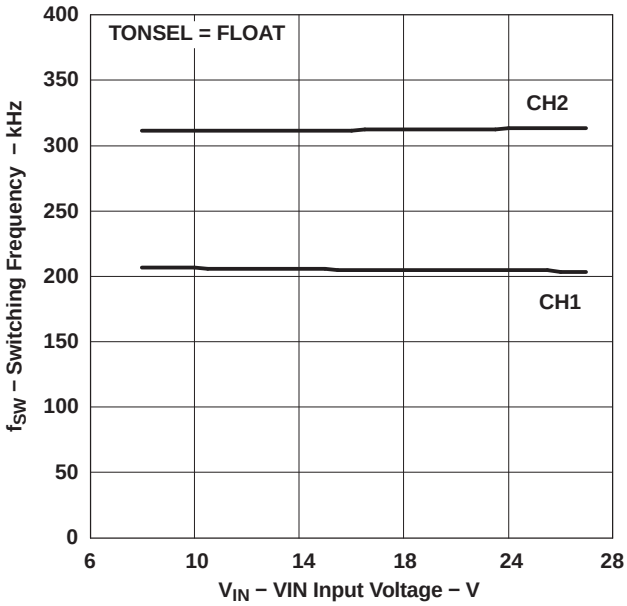


Figure 15.

SWITCHING FREQUENCY
vs
INPUT VOLTAGE

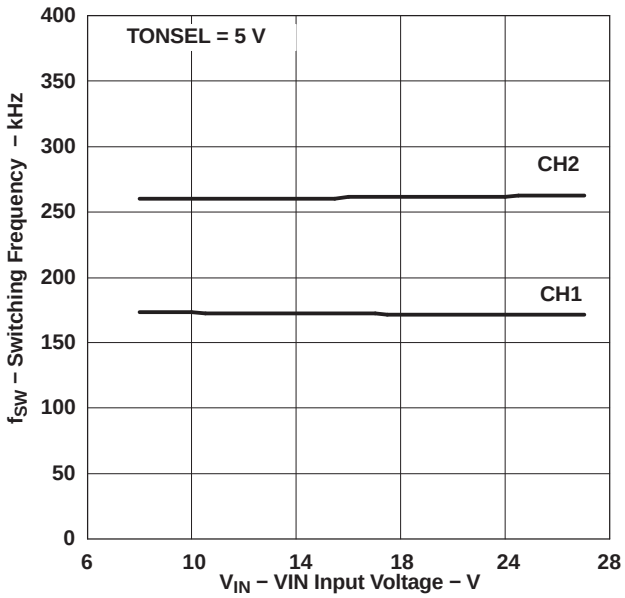


Figure 16.

SWITCHING FREQUENCY
vs
OUTPUT CURRENT

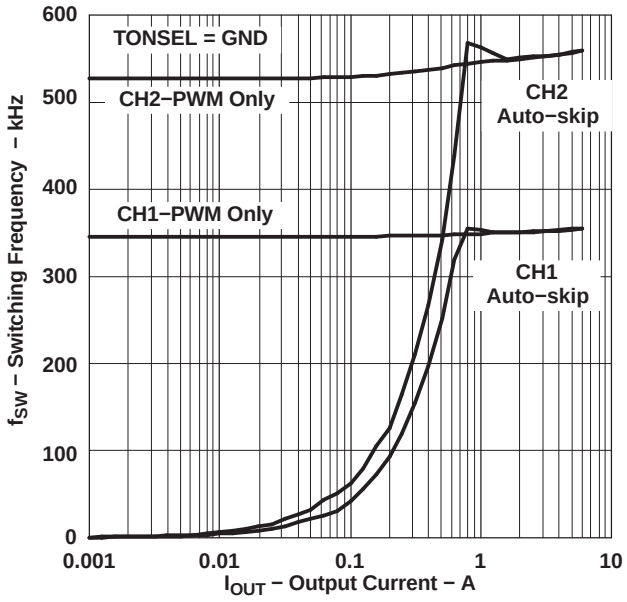


Figure 17.

SWITCHING FREQUENCY
vs
OUTPUT CURRENT

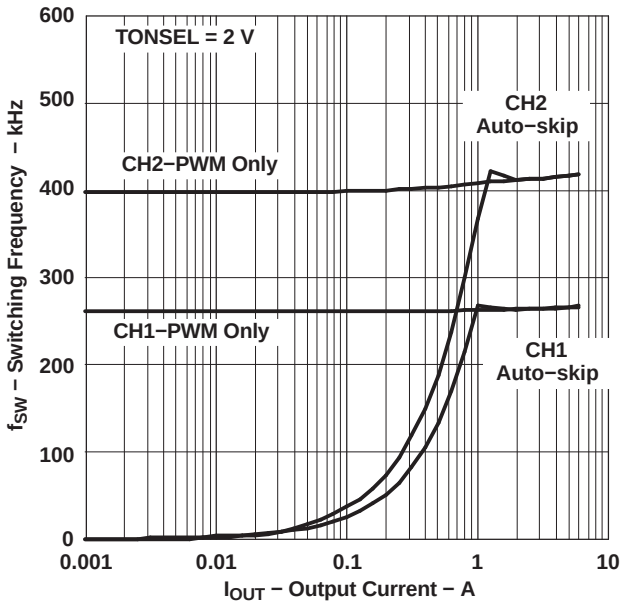


Figure 18.

TYPICAL CHARACTERISTICS (continued)

SWITCHING FREQUENCY
vs
OUTPUT CURRENT

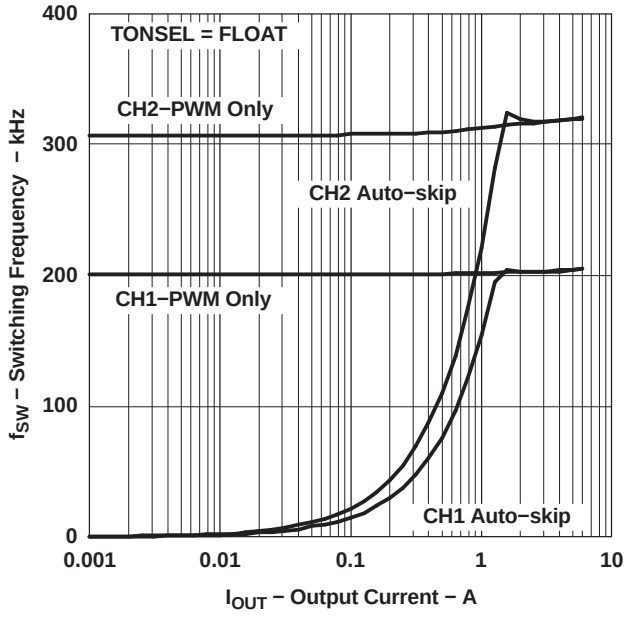


Figure 19.

SWITCHING FREQUENCY
vs
OUTPUT CURRENT

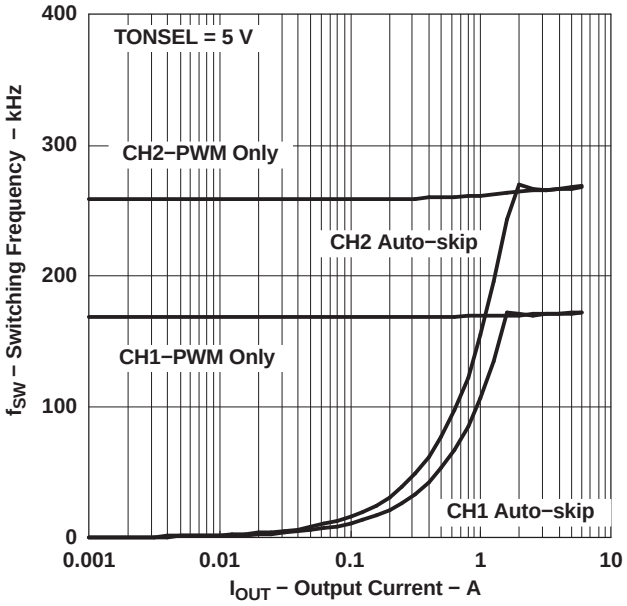


Figure 20.

OVP/UVP THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

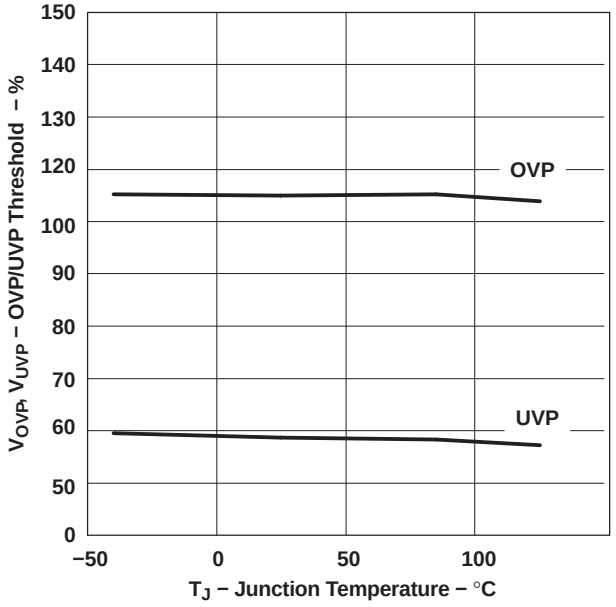


Figure 21.

VREG5 OUTPUT VOLTAGE
vs
OUTPUT CURRENT

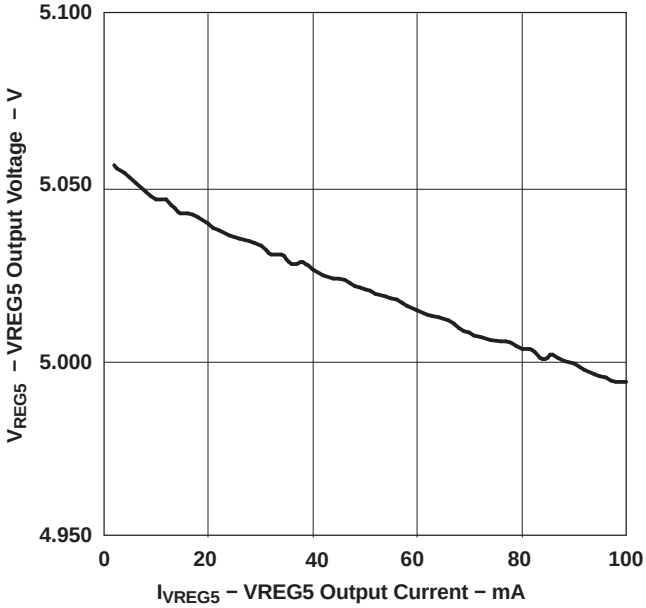


Figure 22.

TYPICAL CHARACTERISTICS (continued)

VREG3 OUTPUT VOLTAGE
vs
OUTPUT CURRENT

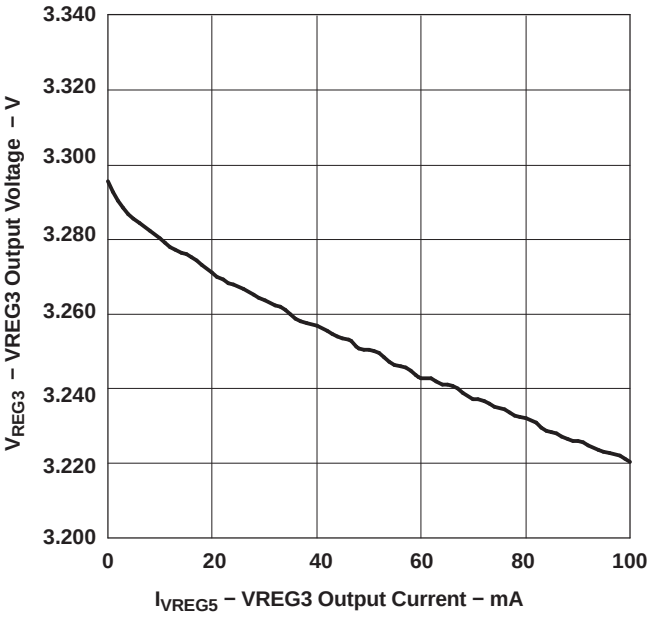


Figure 23.

VREF2 OUTPUT VOLTAGE
vs
OUTPUT CURRENT

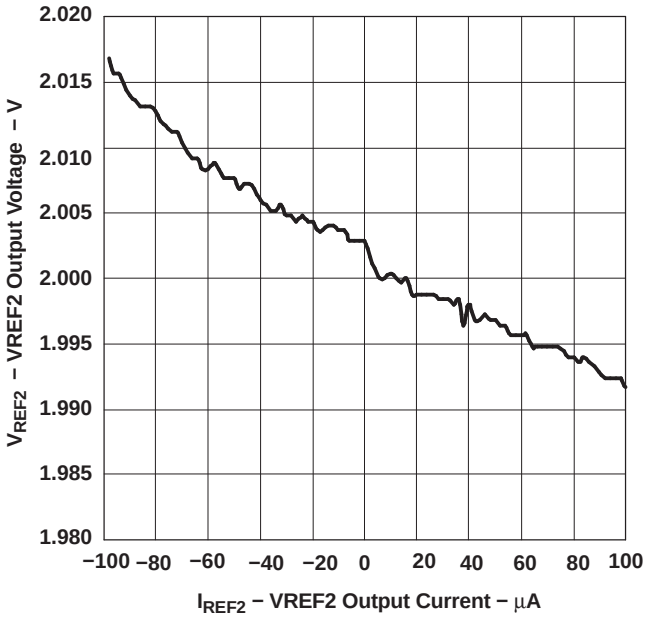


Figure 24.

5-V OUTPUT VOLTAGE
vs
OUTPUT CURRENT

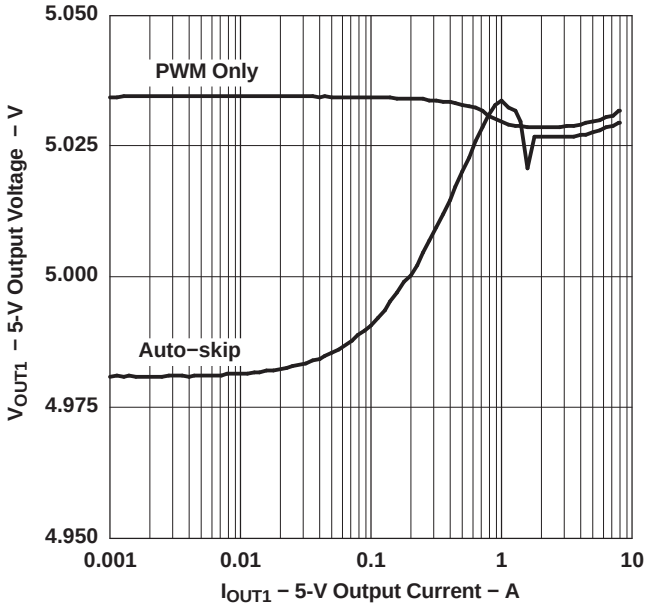


Figure 25.

3.3-V OUTPUT VOLTAGE vs
OUTPUT CURRENT

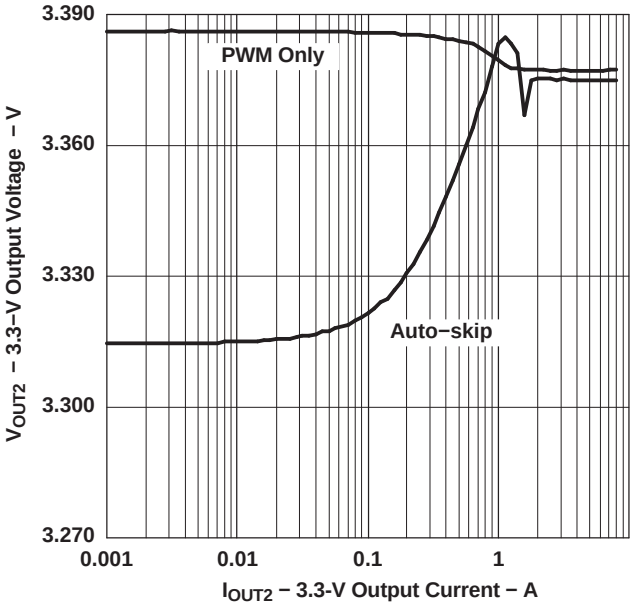


Figure 26.

TYPICAL CHARACTERISTICS (continued)

5-V OUTPUT VOLTAGE vs INPUT VOLTAGE

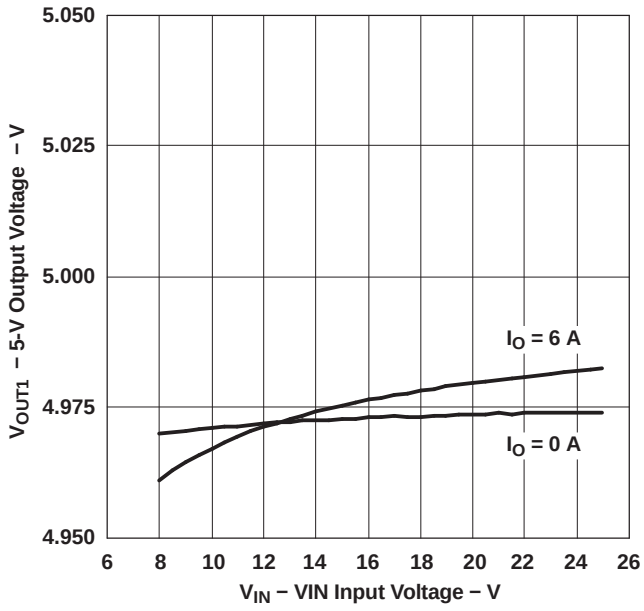


Figure 27.

3.3-V OUTPUT VOLTAGE vs INPUT VOLTAGE

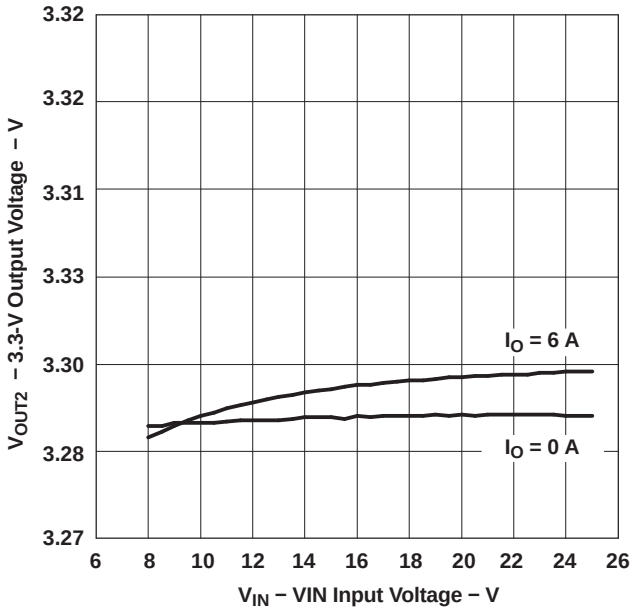


Figure 28.

5-V EFFICIENCY vs OUTPUT CURRENT

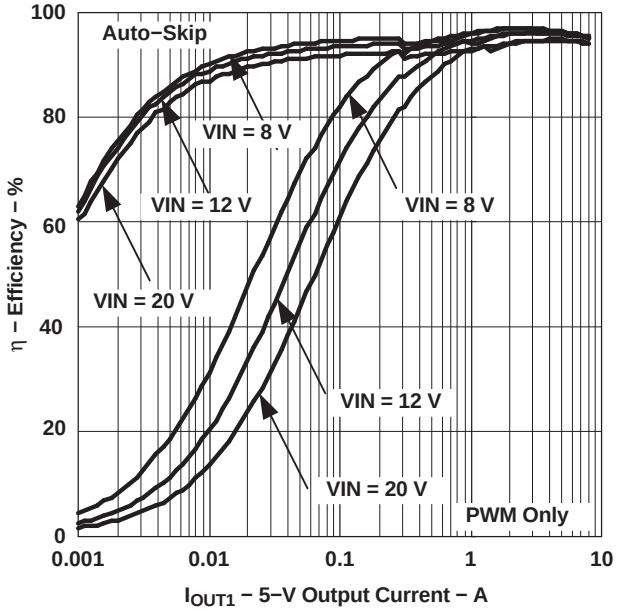


Figure 29.

3.3-V EFFICIENCY vs OUTPUT CURRENT

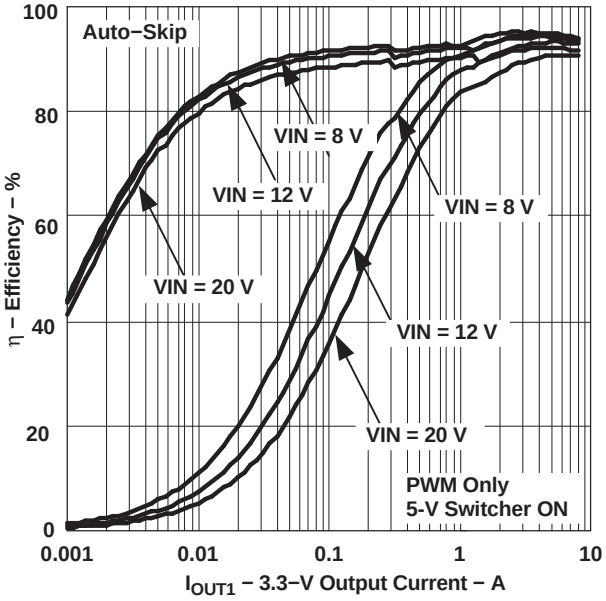


Figure 30.

TYPICAL CHARACTERISTICS (continued)

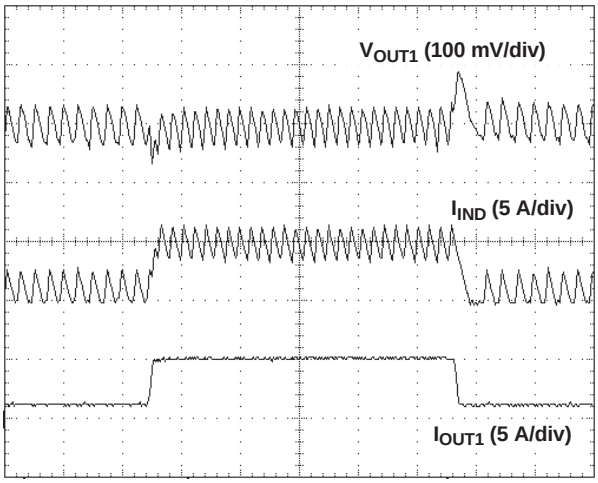


Figure 31. 5-V Load Transient Response

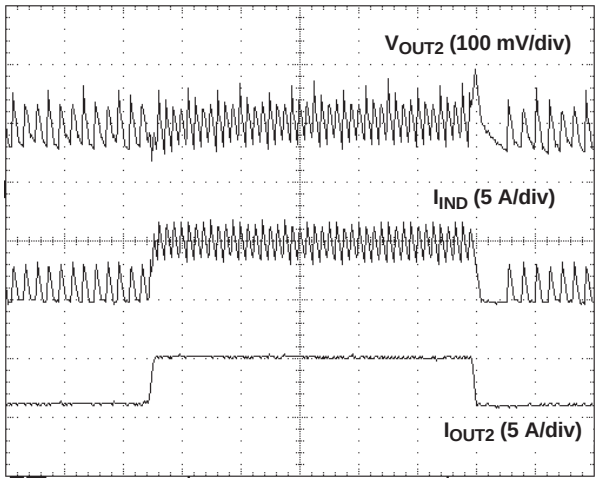


Figure 32. 3.3-V Load Transient Response

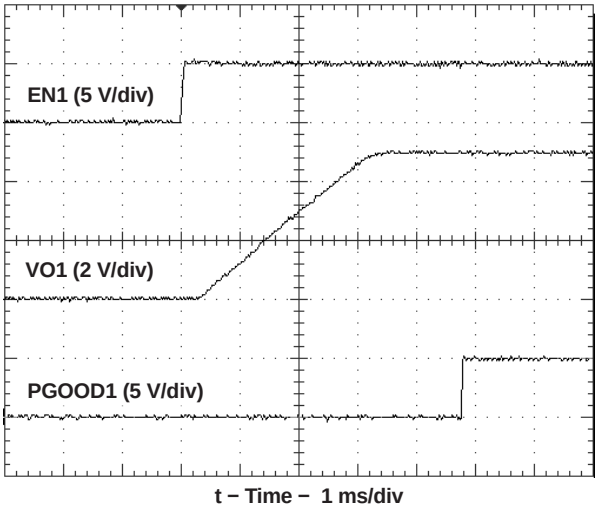


Figure 33. 5-V Startup Waveforms

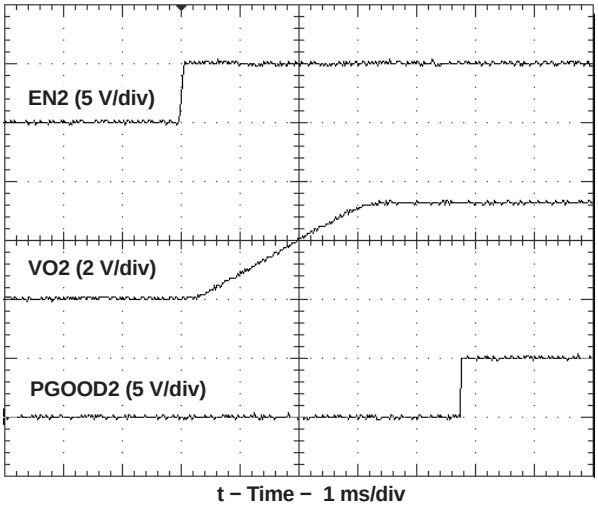


Figure 34. 3.3-V Startup Waveforms

TYPICAL CHARACTERISTICS (continued)

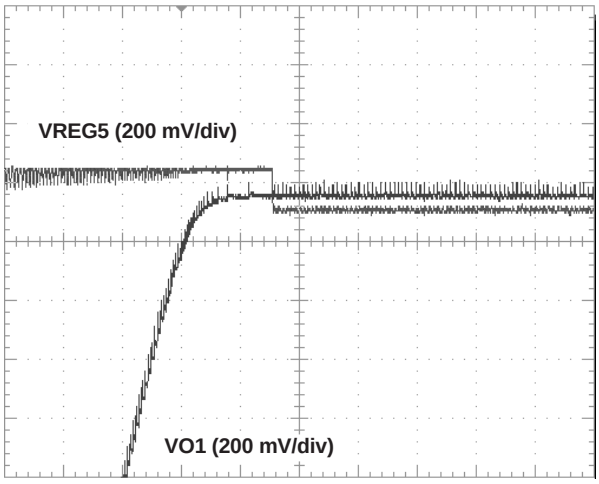


Figure 35. 5-V Switchover Waveforms

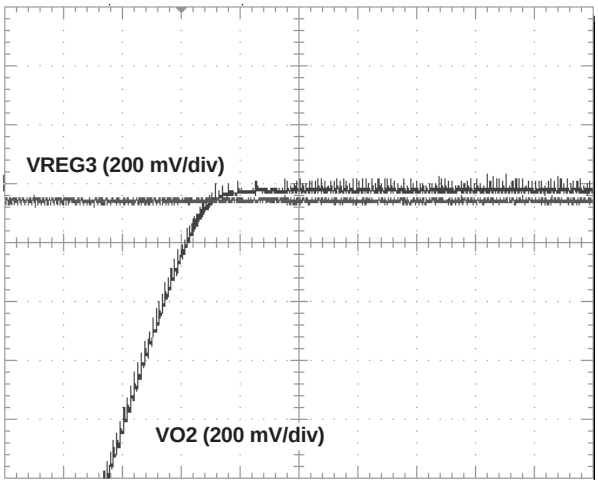


Figure 36. 3.3-V Switchover Waveforms

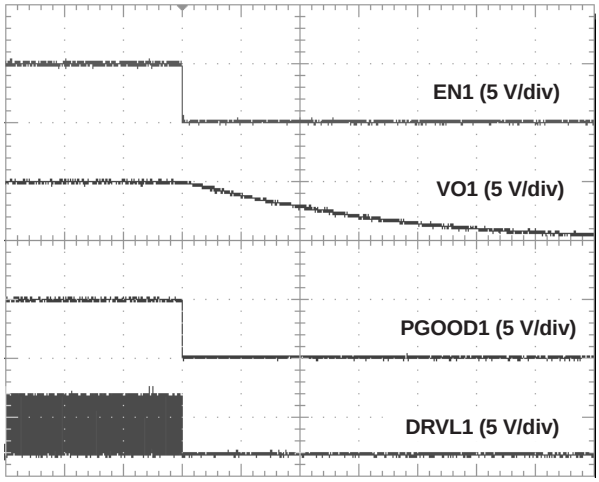


Figure 37. 5-V Soft-Stop Waveforms

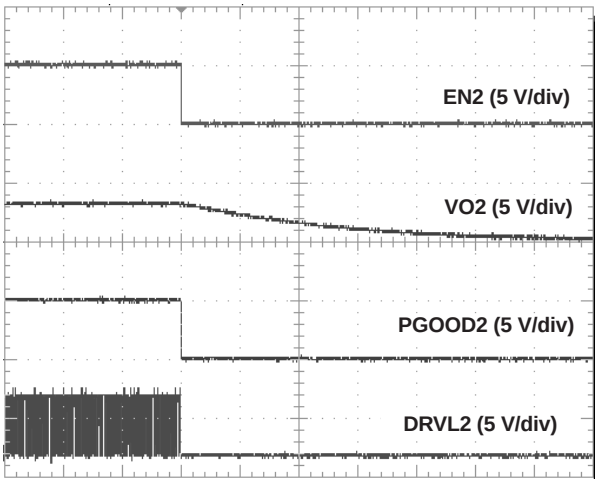


Figure 38. 3.3-V Soft-Stop Waveforms

TYPICAL CHARACTERISTICS (continued)

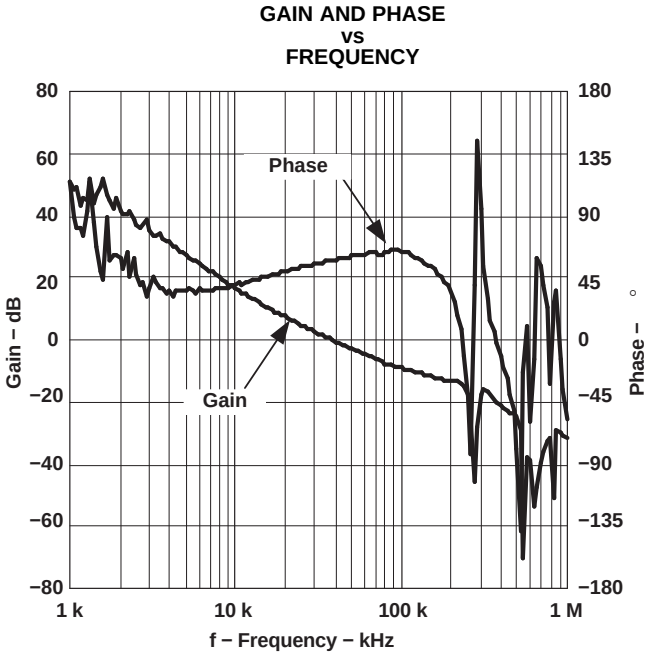


Figure 39. 5-V Bode Plot (Current Mode)

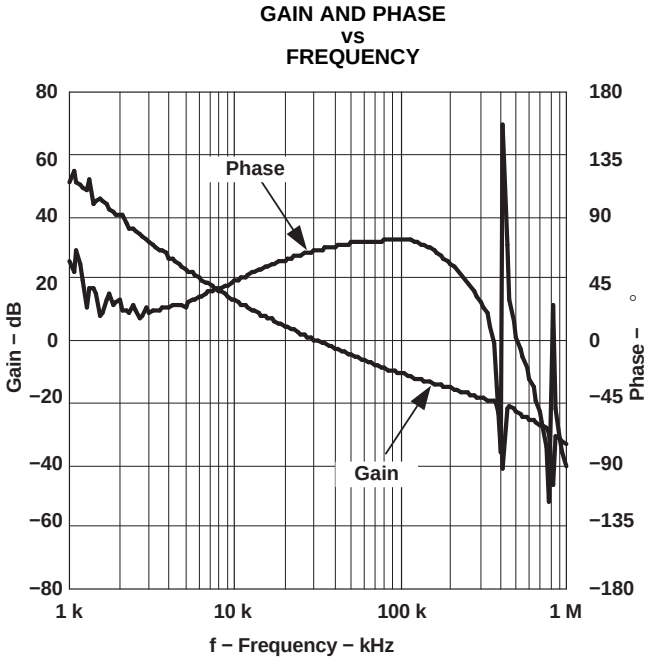


Figure 40. 3.3-V Bode Plot (Current Mode)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS51120RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS51120RHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS51120RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS51120RHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

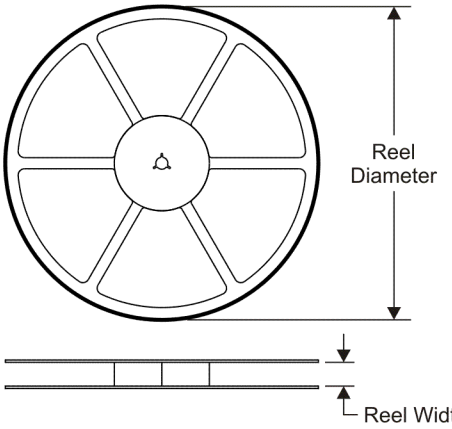
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

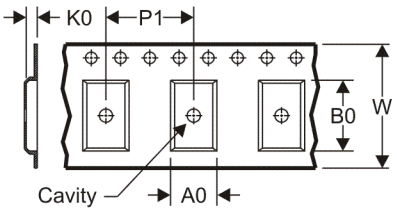
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

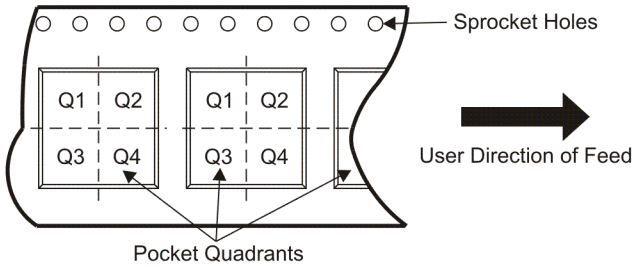


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

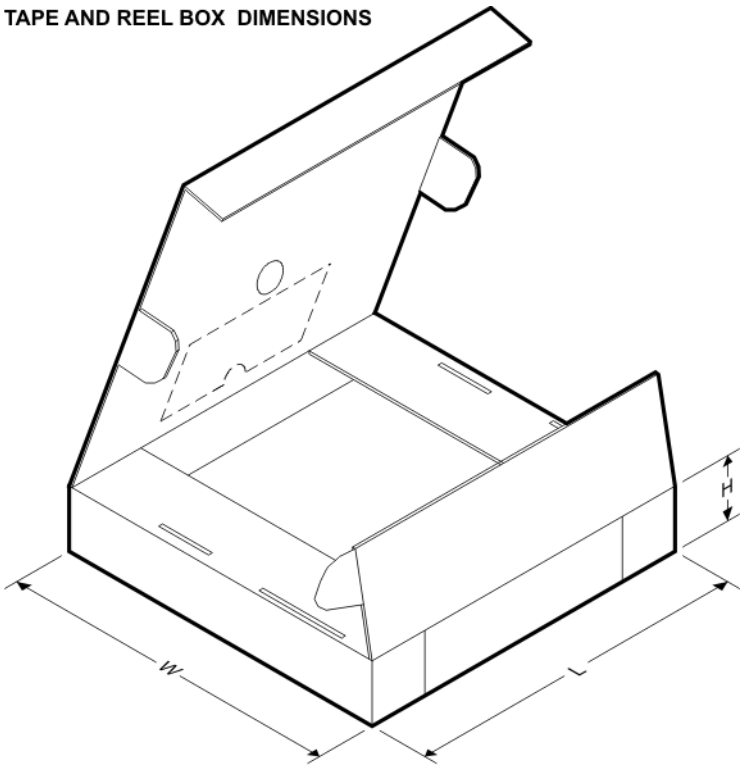
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51120RHBR	QFN	RHB	32	3000	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2
TPS51120RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS51120RHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

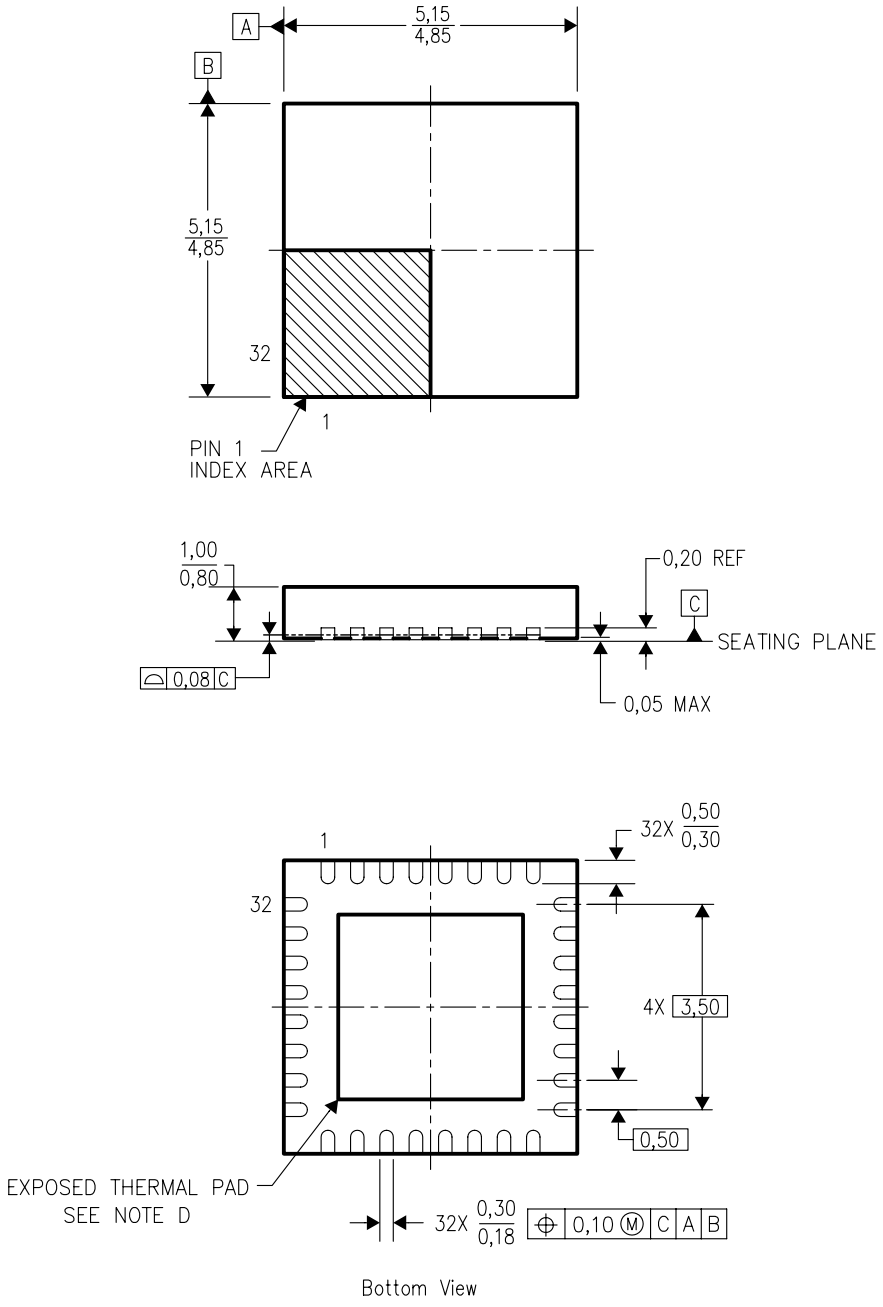
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51120RHBR	QFN	RHB	32	3000	370.0	355.0	55.0
TPS51120RHBR	QFN	RHB	32	3000	346.0	346.0	29.0
TPS51120RHBT	QFN	RHB	32	250	190.5	212.7	31.8

RHB (S–PQFP–N32) PLASTIC QUAD FLATPACK



4204326/C xx/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

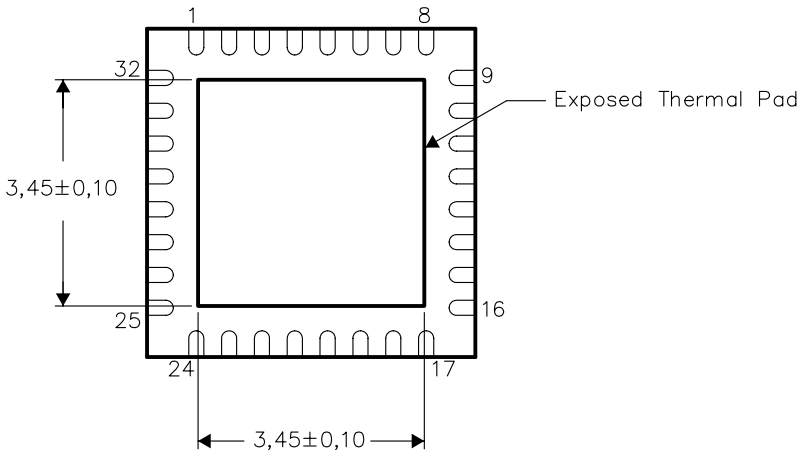
RHB (S–PQFP–N32)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

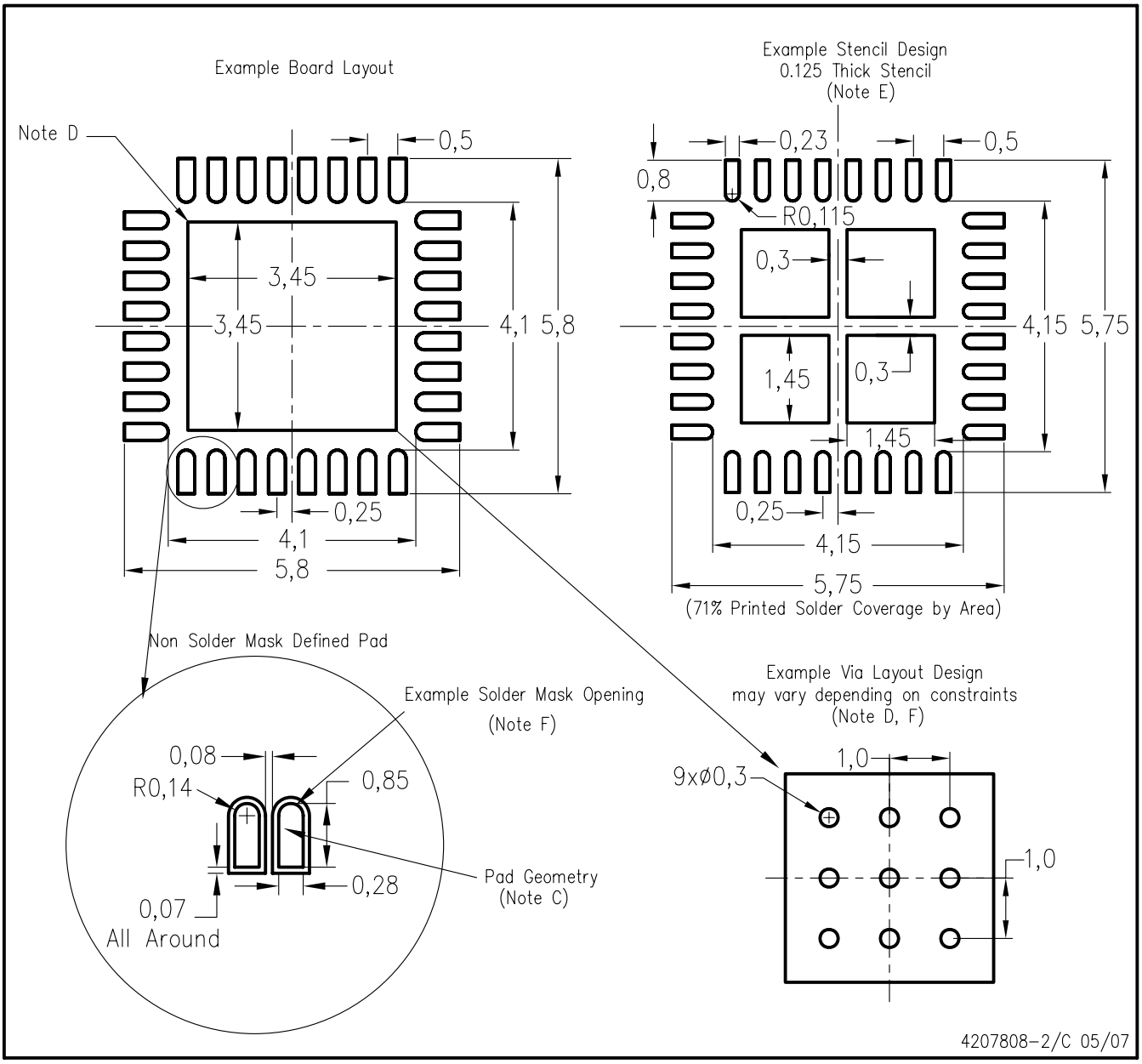


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHB (S–PQFP–N32)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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