TPS6120x Low Input Voltage Synchronous Boost Converter With 1.3-A Switches

1 Features

- More than 90% Efficiency at
  - 300 mA Output Current at 3.3 V (VIN ≥ 2.4 V)
  - 600 mA Output Current at 5 V (VIN ≥ 3 V)
- Automatic Transition between Boost Mode and Down Conversion Mode
- Device Quiescent Current Less than 55 µA
- Startup into Full Load at 0.5 V Input Voltage
- Operating Input Voltage Range from 0.3 V to 5.5 V
- Programmable Undervoltage Lockout Threshold
- Output Short Circuit Protection Under all Operating Conditions
- Fixed and Adjustable Output Voltage Options from 1.8 V to 5.5 V
- Power Save Mode for Improved Efficiency at Low Output Power
- Forced Fixed Frequency Operation Possible
- Load Disconnect During Shutdown
- Overtemperature Protection
- Small 3 mm x 3 mm VSON-10 Package

2 Applications

- All Single-Cell, Two-Cell and Three-Cell Alkaline, NiCd or NiMH or Single-Cell Li Battery Powered Products
- Fuel Cell And Solar Cell Powered Products
- Portable Audio Players
- PDAs
- Cellular Phones
- Personal Medical Products
- White LED Driver

3 Description

The TPS6120x devices provide a power supply solution for products powered by either a single-cell, two-cell, or three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-polymer battery. It is also used in fuel cell or solar cell powered devices where the capability of handling low input voltages is essential. Possible output currents depend on the input to output voltage ratio. The devices provide output currents of up to 600 mA at a 5-V output, while using a single-cell Li-Ion or Li-Polymer battery and discharges it down to 2.6 V. The boost converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. At low load currents, the converter enters the Power Save mode to maintain a high efficiency over a wide load current range. The Power Save mode can be disabled, forcing the converter to operate at a fixed switching frequency. The average input current is limited to a maximum value of 1500 mA. The output voltage is programmed by an external resistor divider, or is fixed internally on the chip. The converter can be disabled to minimize battery drain. During shutdown, the load is completely disconnected from the battery. The device is packaged in a 10-pin VSON package measuring 3 mm x 3 mm.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6120x	VSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Typical Application

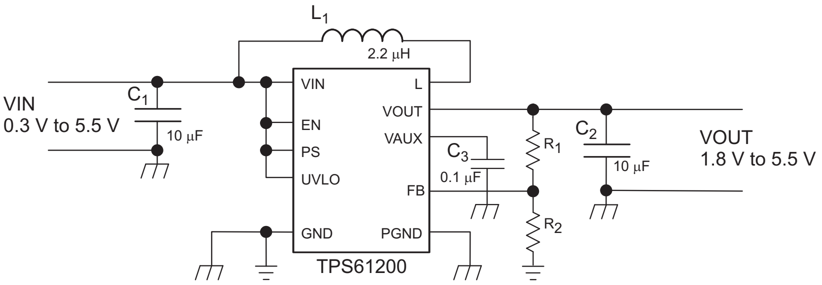

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Table of Contents

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision C (September 2012) to Revision D	Page
• Changed the PS pin description From: Enable/disable Power Save mode (High = enabled, Low = disabled) To: Enable/disable Power Save mode (High = disabled, Low = enabled)	4

Changes from Revision B (FEBRUARY 2008) to Revision C	Page
• Changed Feature From: Small 3 mm x 3 mm QFN-10 Package To: Small 3 mm x 3 mm SON-10 Package	1
• Changed Application From: White LED's To: White LED Driver	1
• Changed the Available Device Options Package type From: 10-PIN QFN To: 10-Pin SON	4
• Changed V_{SS} to V_{IN} in the Recommended Operating Conditions table	5
• Changed From: DISSIPATION RATINGS TABLE To: Thermal Information table	5
• Changed the Parameters and Test Conditions in the Electrical Characteristics table	6
• Updated Figure 1 through Figure 11	7
• Added C3 to the List of Components	14
• Added text to the Input Capacitor section "An R-C filter may be placed..."	16
• Added Figure 26, Figure 27, and Figure 28	19
• Added Figure 29	21

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Changes from Revision A (JUNE 2007) to Revision B — Page

- Added DSC package and tape and reel note to the Available Device Options. 4

Changes from Original (MARCH 2007) to Revision A — Page

- Changed Features bullet From: 600 mA Output Current at 3.3 V (VIN ≥ 1.2 V) To: 300 mA Output Current at 3.3 V (VIN ≥ 2.4 V) 1
- Changed Figure 6 label From: Power Save Disabled To: Power Save Enabled 7
- Changed Figure 7 label From: Power Save Enabled To: Power Save Disabled 8

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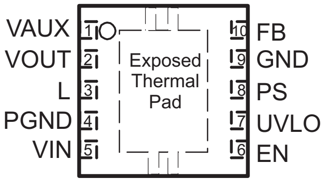
6 Device Options

T_A	OUTPUT VOLTAGE(1)	PART NUMBER(2)
–40°C to 85°C	Adjustable	TPS61200DRC
	3.3 V	TPS61201DRC
	5 V	TPS61202DRC
	5 V	TPS61202DSC

(1) Contact the factory to check availability of other fixed output voltage versions.
(2) The DRC and the DSC package are available taped and reeled. Add R suffix to device type (e.g., TPS61200DRCR or TPS61202DSCR) to order quantities of 3000 devices per reel. It is also available in minireels. Add a T suffix to the device type (i.e. TPS61200DRCT or TPS61202DSCT) to order quantities of 250 devices per reel.

7 Pin Configuration and Functions

DSC and DRC Package
10 Pins
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	6	I	Enable input (High = enabled, Low = disabled). Do not leave floating.
Exposed thermal pad	—	—	Must be soldered to achieve appropriate power dissipation and mechanical reliability. Should be connected to PGND.
FB	10	I	Voltage feedback of adjustable versions, must be connected to V_{OUT} at fixed output voltage versions
GND	9	—	Control / logic ground
PGND	4	—	Power ground
PS	8	I	Enable/disable Power Save mode (High = disabled, Low = enabled). Do not leave floating.
L	3	I	Connection for Inductor
UVLO	7	I	Undervoltage lockout comparator input. Must be connected to VAUX if not used
VAUX	1	I/O	Supply voltage for control stage
VIN	5	I	Boost converter input voltage
VOUT	2	O	Boost converter output

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage range on VIN, L, VAUX, VOUT, PS, EN, FB, UVLO	–0.3	7	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
		Machine Model (MM)(3)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

8.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage at VIN	0.3		5.5	V
T_A	Operating free air temperature range	–40		85	°C
T_J	Operating junction temperature range	–40		125	°C

8.4 Thermal Information

THERMAL METRIC(1)		TPS6120x		UNIT
		DRC	DSC	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.2	40.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.8	37.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	16.6	15.4	
ψ_{JT}	Junction-to-top characterization parameter	1.2	0.3	
ψ_{JB}	Junction-to-board characterization parameter	16.8	15.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.1	2.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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8.5 Electrical Characteristics

over recommended junction temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC-DC STAGE							
V_{IN}	Input voltage range			0.3		5.5	V
V_{IN}	Minimum input voltage at startup					0.5	V
V_{OUT}	TPS61200 output voltage range			1.8		5.5	V
V_{FB}	TPS61200 feedback voltage			495	500	505	mV
V_{OUT}	TPS61201 output voltage		$V_{IN} < V_{OUT}$, PS = High	3.27	3.3	3.33	V
V_{OUT}	TPS61202 output voltage		$V_{IN} < V_{OUT}$, PS = High	4.95	5.0	5.05	V
f	Oscillator frequency			1250		1650	kHz
I_{LIM}	average inductor current limit		V_{OUT} = 3.3 V	1200	1350	1500	mA
$R_{DS(on)}$	Rectifying switch on resistance		V_{OUT} = 3.3 V		180		mΩ
$R_{DS(on)}$	Main switch on resistance		V_{OUT} = 3.3 V		150		mΩ
	Line regulation		$V_{IN} < V_{OUT}$, PS = High		0.1%	0.5%	
	Load regulation		$V_{IN} < V_{OUT}$, PS = High		0.1%	0.5%	
I_Q	Quiescent current	V_{IN}	I_O = 0 mA, $V_{EN} = V_{IN}$ = 1.2 V, V_{OUT} = 3.3 V, V_{AUX} = 3.3 V PS = Low		1	2	μA
		V_{OUT}			50	70	μA
		V_{AUX}			4	6	μA
I_{SD}	Shutdown current	V_{IN}	V_{EN} = 0 V, V_{IN} = 1.2 V		0.5	1.5	μA
		V_{AUX}			1	2	μA
I_{LKG}	Input leakage current (L)		V_{EN} = 0 V, V_{IN} = 1.2 V, V_L = 1.2 V		0.01	1	μA
CONTROL STAGE							
V_{AUX}	Auxiliary Output Voltage			2.4		5.5	V
V_{IL}	Low level input threshold voltage (EN)		V_{IN} < 0.8 V			0.1 × V_{IN}	V
V_{IH}	High level input threshold voltage (EN)		V_{IN} < 0.8 V	0.9 × V_{IN}			V
V_{IL}	Low level input threshold voltage (EN)		0.8 V ≤ V_{IN} ≤ 1.5 V			0.2 × V_{IN}	V
V_{IH}	High level input threshold voltage (EN)		0.8 V ≤ V_{IN} ≤ 1.5 V	0.8 × V_{IN}			V
V_{IL}	Low level input threshold voltage (EN)		V_{IN} > 1.5 V			0.4	V
V_{IH}	High level input threshold voltage (EN)		V_{IN} > 1.5 V	1.2			V
V_{IL}	Low level input threshold voltage (PS)					0.4	V
V_{IH}	High level input threshold voltage (PS)			1.2			V
I_{LKG}	Input leakage current (EN, PS)		EN, PS = GND or V_{IN}		0.01	0.1	μA
V_{UVLO}	Undervoltage lockout threshold		Falling UVLO voltage	235	250	265	mV
V_{UVLO}	Undervoltage lockout threshold		Rising UVLO voltage	330	350	370	mV
I_{LKG}	Input leakage current (UVLO)		V_{UVLO} = 0.5 V			0.3	μA
V_{OVP}	Overvoltage protection threshold			5.5		7	V
	Thermal shutdown temperature		Rising temperature		140		°C
	Thermal shutdown temperature hysteresis				20		°C

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8.6 Typical Characteristics

Table 1. Table of Graphs

		FIGURE
Maximum output current	vs Input voltage	Figure 1
Efficiency	vs Output current (TPS61200), Power Save Enabled	Figure 2
	vs Output current (TPS61200), Power Save Disabled	Figure 3
	vs Output current (TPS61201), Power Save Enabled	Figure 4
	vs Output current (TPS61201), Power Save Disabled	Figure 5
	vs Output current (TPS61202), Power Save Enabled	Figure 6
	vs Output current (TPS61202), Power Save Disabled	Figure 7
	vs Input voltage (TPS61201), Power Save Enabled	Figure 8
	vs Input voltage (TPS61201), Power Save Disabled	Figure 9
	vs Input voltage (TPS61202), Power Save Enabled	Figure 10
	vs Input voltage (TPS61202), Power Save Disabled	Figure 11
Output voltage	vs Output current (TPS61201)	Figure 12
	vs Output current (TPS61202)	Figure 13

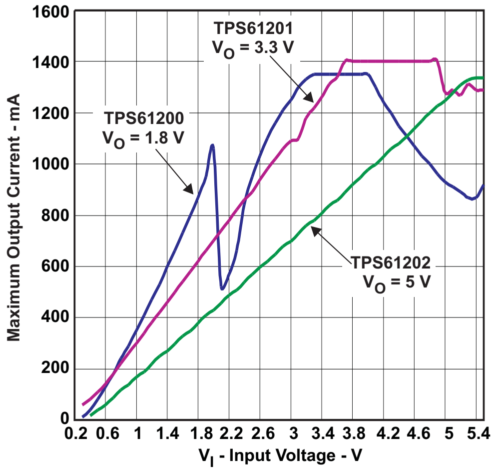

Figure 1. Maximum Output Current vs Input Voltage

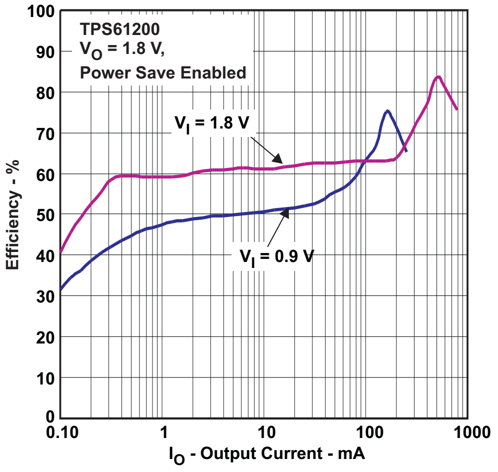

Figure 2. Efficiency vs Output Current

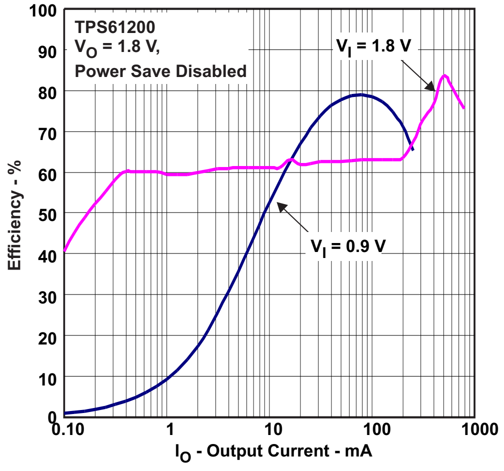

Figure 3. Efficiency vs Output Current

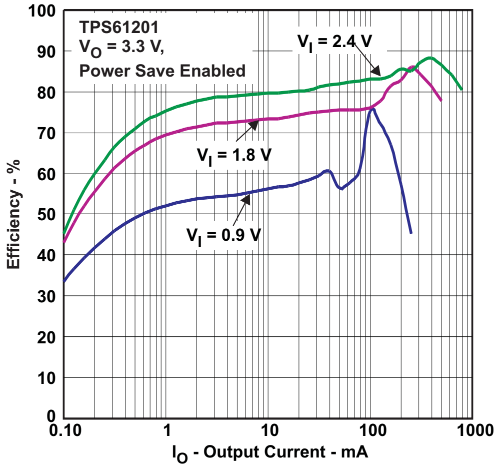

Figure 4. Efficiency vs Output Current

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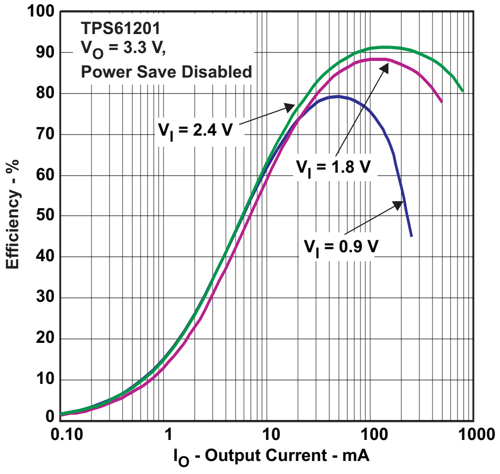

Figure 5. Efficiency vs Output Current

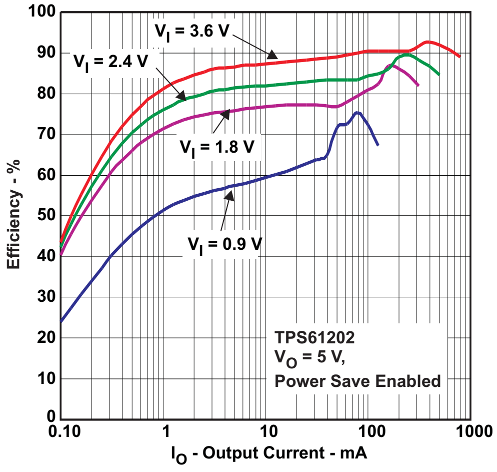

Figure 6. Efficiency vs Output Current

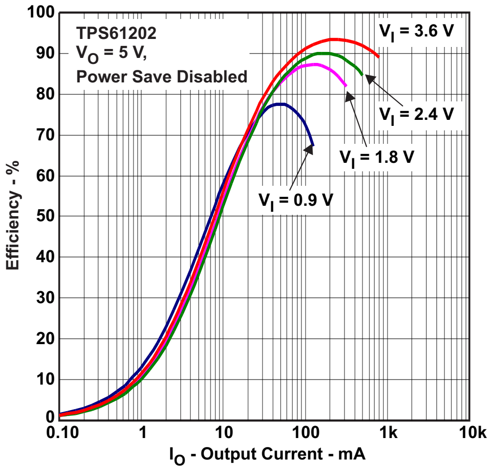

Figure 7. Efficiency vs Output Current

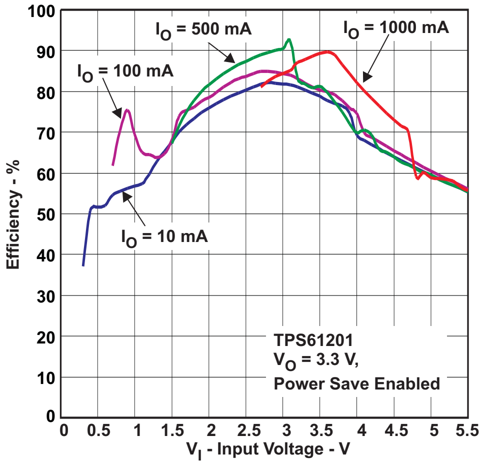

Figure 8. Efficiency vs Input Voltage

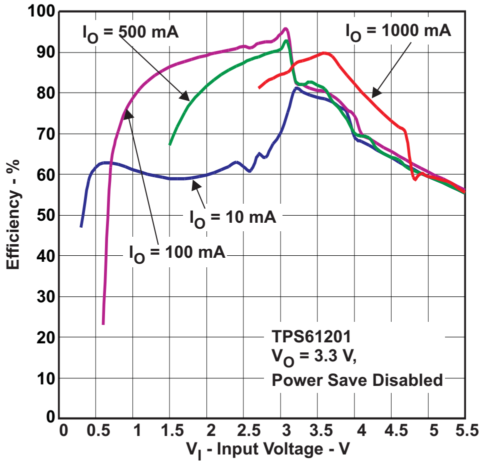

Figure 9. Efficiency vs Input Voltage

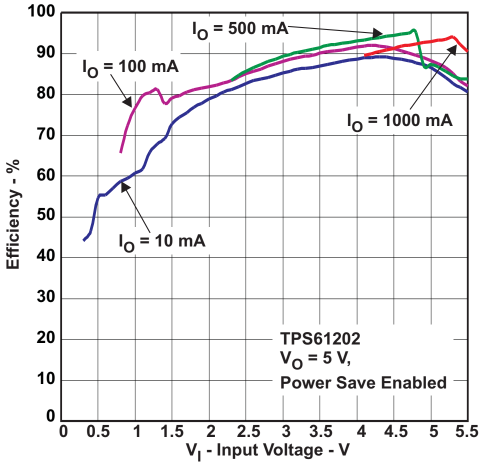

Figure 10. Efficiency vs Input Voltage

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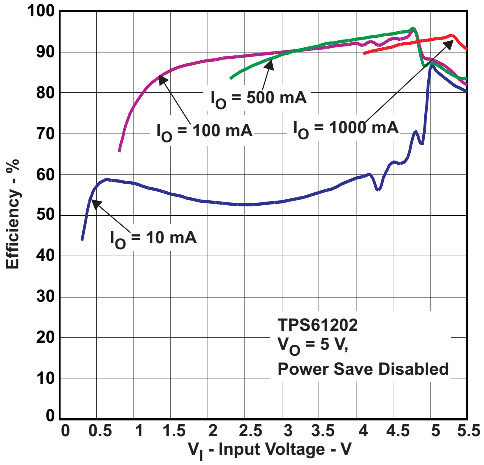

Figure 11. Efficiency vs Input Voltage

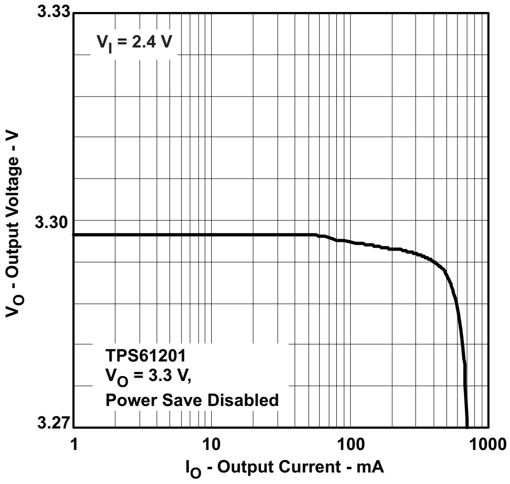

Figure 12. Output Voltage vs Output Current

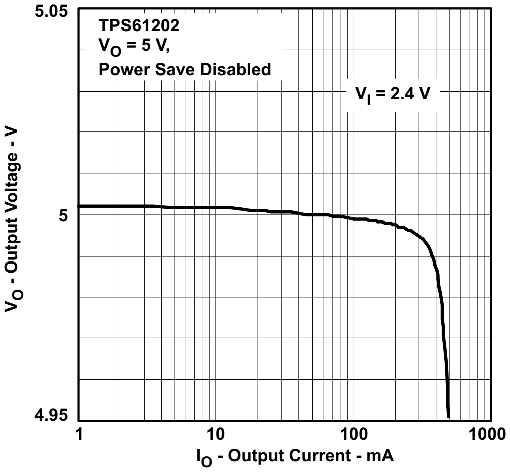

Figure 13. Output Voltage vs Output Current

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9 Parameter Measurement Information

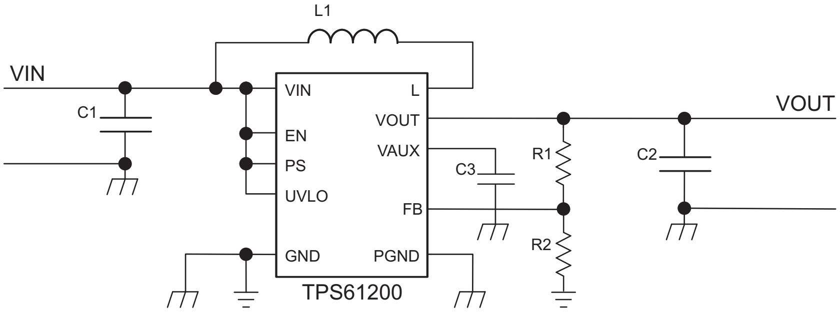

Figure 14. Parameter Measurement Schematic

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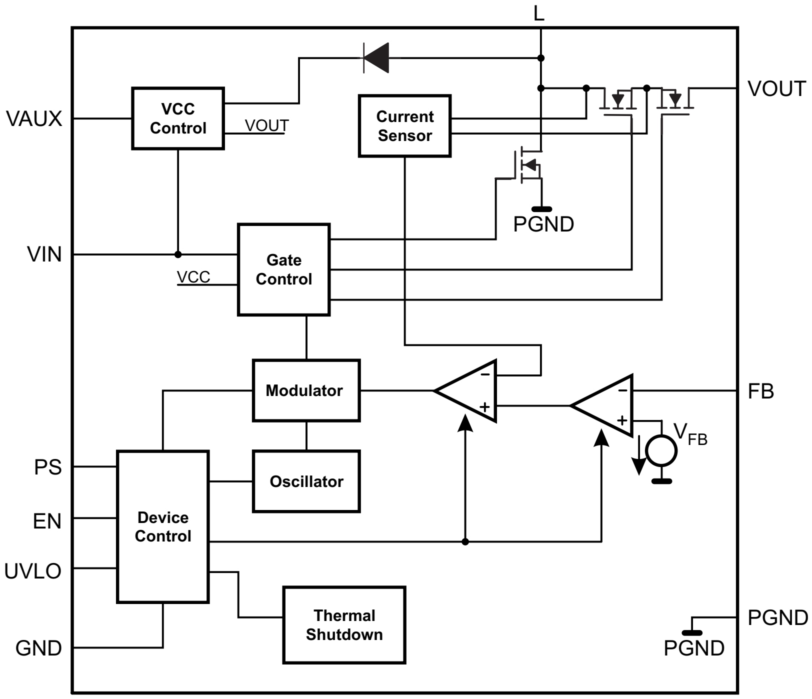
10 Detailed Description

10.1 Overview

The TPS6120x is a low input voltage synchronous boost converter family. The devices support 0.3-V to 5.5-V input voltage range, so can provide power supply solutions for products powered by either a single-cell, two-cell, or three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-polymer battery. It is also used in fuel cell or solar cell powered devices where the capability of handling low input voltages is essential. The devices provide output currents of up to 600 mA at a 5-V output, while using a single-cell Li-Ion or Li-Polymer battery and discharges it down to 2.6 V. The boost converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. At low load currents, the converter enters the Power Save mode to maintain a high efficiency over a wide load current range. The Power Save mode can be disabled, forcing the converter to operate at a fixed switching frequency. The average input current is limited to a maximum value of 1500 mA. The output voltage is programmed by an external resistor divider, or is fixed internally on the chip. The converter can be disabled to minimize battery drain. During shutdown, the load is completely disconnected from the battery.

10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 Controller Circuit

The controlling circuit of the device is based on an average current mode topology. The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. The controller also uses input and output voltage feedforward. Changes of input and output voltage are monitored and immediately change the duty cycle in the modulator to achieve a fast response to those errors. The voltage error amplifier gets its feedback input from the FB pin. For adjustable output voltage devices, a resistive voltage divider must be connected to that pin. For fixed output voltage devices, FB must be connected to the output voltage to directly sense the voltage. Fixed output voltage versions use a trimmed internal resistive divider. The feedback voltage is compared with the internal reference voltage to generate a stable and accurate output voltage.

The controller circuit also senses the average input current as well as the peak input current. Thus, the maximum input power is controlled as well as the maximum peak current, to achieve a safe and stable operation under all possible conditions. To protect the device from overheating, an internal temperature sensor is implemented.

10.3.1.1 Synchronous Operation

The device uses three internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over a wide input voltage and output power range.

To avoid ground shift problems due to the high currents in the switches, two separate ground pins, GND and PGND, are used. The reference for all control functions is the GND pin. The power switches are connected to PGND. Both grounds must be connected on the PCB at only one point, ideally close to the GND pin. Due to the 3-switch topology, the load is always disconnected from the input during shutdown of the converter.

10.3.1.2 Down Regulation

A boost converter only regulates output voltages which are higher than the input voltage. This device operates differently. For example, it is able to regulate 3 V at the output with two fresh alkaline cells at the input having a total cell voltage of 3.2 V. Another example is powering white LEDs with a forward voltage of 3.6 V from a fully charged Li-Ion cell with an output voltage of 4.2 V. To control these applications properly, a Down Conversion mode is implemented.

If the input voltage reaches or exceeds the output voltage, the converter automatically changes to a Down Conversion mode. In this mode, the control circuit changes the behavior of the two rectifying switches. While continuing switching, it sets the voltage drop across the rectifying switches as high as needed to regulate the output voltage. This means the power losses in the converter increase. This must be taken into account for thermal consideration.

10.3.1.3 Device Enable

The device is put into operation when EN is set high. It is put into Shutdown mode when EN is set to low. In Shutdown mode, the regulator stops switching, all internal control circuitry including the UVLO comparator is switched off, and the load is disconnected from the input. Current does not flow from input to output or from output to input. This also means that the output voltage can drop below the input voltage during shutdown.

10.3.1.4 Softstart and Short-Circuit Protection

During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents drawn from the battery. After being enabled, the device starts operating. At first, it keeps the main output VOUT disconnected, and charges the capacitor at VAUX. Once the capacitor at VAUX is charged to about 2.5 V, the device switches to normal operation. This means VOUT is turned on and the capacitor at VOUT is charged, while the load connected to the device is supplied. To ramp up the output voltage in a controlled way, the average current limit is set to 400 mA and rises proportional to the increase of the output voltage. At an output voltage of about 1.2 V the current limit is at its nominal value. If the output voltage does not increase, the current limit does not increase. There is no timer implemented. Thus the output voltage overshoot at startup, as well as the inrush current, is kept at a minimum. The device ramps up the output voltage in a controlled manner even if a large capacitor is connected at the output. When the output voltage does not increase above 1.2 V, the device assumes a short-circuit at the output, and keeps the current limit low to protect itself and the application. When there is a short at the output during operation, the current limit is decreased accordingly.

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Feature Description (continued)

The device can also start into a Prebias on the outputs.

10.3.1.5 Current Limit

The device current limit limits the average current in the inductor. In a boost connector, this is the input current. If an excessive load requires an input current greater than the average current limit, the device limits the input current by reducing the output power delivered. In this case, the output voltage decreases.

10.3.1.6 Undervoltage Lockout

An undervoltage lockout function prevents the main output at VOUT from being supplied if the voltage at the UVLO pin drops below 0.25 V. When using a resistive divider at the voltage to be monitored, for example the supply voltage, any threshold for the monitored voltage can be programmed. If in undervoltage lockout mode, the device still maintains its supply voltage at VAUX, and it is not turned off until EN is programmed low. This undervoltage lockout function is implemented in order to prevent the malfunctioning of the converter.

10.3.1.7 Thermal Shutdown

The device has a built-in temperature sensor which monitors the internal IC temperature. If the temperature exceeds the programmed threshold (see electrical characteristics table), the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at IC temperatures at the thermal shutdown threshold.

10.4 Device Functional Modes

10.4.1 Power Save Mode

The Power Save (PS) pin can be used to select different operation modes. To enable Power Save mode the PS pin must be set low. Power Save mode is used to improve efficiency at light load. If Power Save mode is enabled, the converter stops operating if the average inductor current decreases below about 300 mA and the output voltage is at or above its nominal value. If the output voltage decreases below its nominal value, the device ramps up the output voltage again by starting operation using a programmed average inductor current higher than required by the current load condition. Operation can last for one or several pulses. The converter stops operating once the conditions for stopping operation are met again.

The Power Save mode can be disabled by programming a high at the PS pin. In Down Conversion mode, Power Save mode is always enabled and the device cannot be forced into fixed frequency operation at light loads. The PS input supports standard logic thresholds.

10.4.2 Down Conversion Mode

If the input voltage reaches or exceeds the output voltage, the converter automatically changes to a Down Conversion mode. In this mode, the control circuit changes the behavior of the two rectifying switches. While continuing switching, it sets the voltage drop across the rectifying switches as high as needed to regulate the output voltage. This means the power losses in the converter increase. This must be taken into account for thermal consideration.

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11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The TPS6120x DC-DC converters are intended for systems powered by a single up to triple cell Alkaline, NiCd, NiMH battery with a typical terminal voltage between 0.7 V and 5.5 V. They can also be used in systems powered by one-cell Li-Ion or Li-Polymer with a typical voltage between 2.5 V and 4.2 V. Additionally, any other voltage source like solar cells or fuel cells with a typical output voltage between 0.3 V and 5.5 V can power systems where the TPS6120x is used.

11.2 Typical Application

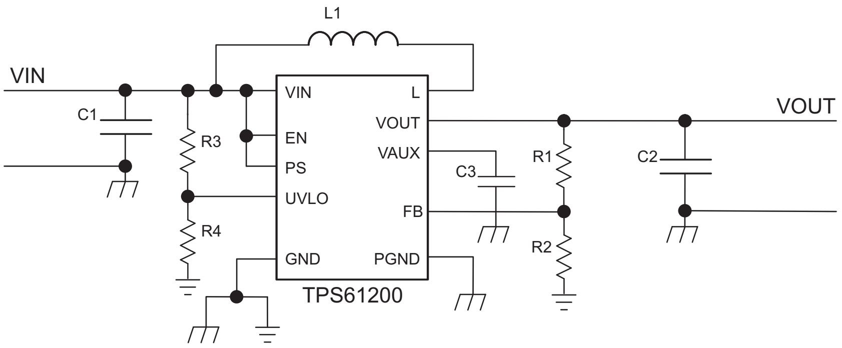

Figure 15. Typical Application Circuit for Adjustable Output Voltage Option

11.2.1 Design Requirements

In this example, TPS61200 is used to design a 3.3-V power supply with 100-mA output current capability. The TPS61200 can be powered by either a single-cell, two-cell, or three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-Polymer battery. In this example, the input voltage range is from 0.8 V to 1.65 V for single-cell alkaline input.

11.2.2 Detailed Design Procedure

Table 2. List of Components

COMPONENT REFERENCE	PART NUMBER	MANUFACTURER	VALUE
C1		any	10 µF, X7R Ceramic
C2		any	2 x 10 µF, X7R Ceramic
C3		any	1 µF, X7R, Ceramic
L1	LPS3015-222ML	Coilcraft	2.2 µH

11.2.2.1 Programming the Output Voltage

Within the TPS6120X family, there are fixed and adjustable output voltage versions available. To properly configure the fixed output voltage devices, the FB pin is used to sense the output voltage. This means that it must be connected directly to VOUT. For the adjustable output voltage version, an external resistor divider is used to adjust the output voltage. The resistor divider must be connected between VOUT, FB and GND. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 500 mV. The maximum recommended value for the output voltage is 5.5 V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 µA, and the voltage

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across the resistor between FB and GND, R2, is typically 500 mV. Based on those two values, the recommended value for R2 should be lower than 500 kΩ, in order to set the divider current at 1 µA or higher. It is recommended to keep the value for this resistor in the range of 200 kΩ. The value of the resistor connected between VOUT and FB, R1, depending on the needed output voltage (V_{OUT}), can be calculated using Equation 1:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \tag{1}$$

As an example, for an output voltage of 3.3 V, a 1-MΩ resistor should be chosen for R_1 when a 180-kΩ is selected for R_2.

11.2.2.2 Programming the UVLO Threshold Voltage

The UVLO input can be used to shut down the main output if the supply voltage is getting too low. The internal reference threshold is typically 250 mV. If the supply voltage should cause the shutdown when it is dropping below 250 mV, V_{IN} can be connected directly to the UVLO pin. If the shutdown should happen at higher voltages, a resistor divider can be used. R3 and R4 in Figure 15 show an example of how to monitor the input voltage of the circuit. The current through the resistive divider should be about 100 times greater than the current into the UVLO pin. The typical current into the UVLO pin is 0.01 µA, and the voltage across R4 is equal to the UVLO voltage threshold that is generated on-chip, which has a value of 250 mV. Therefore, the recommended value for R4 is in the range of 250 kΩ. From this, the value of resistor R3, depending on the desired shutdown voltage $V_{INMIN,}$ can be calculated using Equation 2.

$$R3 = R4 \times \left(\frac{V_{INMIN}}{V_{UVLO}} - 1 \right) \tag{2}$$

11.2.2.3 Inductor Selection

To make sure that the TPS6120X devices can operate, an inductor must be connected between the VIN and L pins. To estimate the minimum inductance value, Equation 3 can be used.

$$L_{MIN} = V_{IN} \times 0.5 \ \frac{\mu s}{A} \tag{3}$$

In Equation 3, the minimum inductance, L_{MIN} , for boost mode operation is calculated. V_{IN} is the maximum input voltage. The recommended inductor value range is between 1.5 µH and 4.7 µH. The minimum inductor value should not be below 1.5 µH, even if Equation 3 yields something lower. Using 2.2 µH is recommended anyway for getting best performance over the whole input and output voltage range.

With the chosen inductance value, the peak current for the inductor in steady state operation can be calculated using Equation 4.

$$I_{LMAX} = \frac{V_{OUT} \times I_{OUT}}{0.8 \times V_{IN}} + \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times V_{OUT} \times f \times L} \tag{4}$$

This would be the critical value for the current rating for selecting the inductor. It also needs to be taken into account that load transients and error conditions may cause higher inductor currents. The following inductor series from different suppliers have been used with TPS6120x converters:

Table 3. List of Inductors

VENDOR	INDUCTOR SERIES
Coilcraft	LPS3015
	LPS4012
Murata	LQH3NP
Tajo Yuden	NR3015
Wurth Elektronik	WE-TPC Typ S

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11.2.2.4 *Capacitor Selection*

11.2.2.4.1 *Input Capacitor*

At least a 4.7-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended.

An R-C filter may be placed on the VIN pin to improve performance in applications with a noisy input source. A 100-Ω resistor and 0.1-µF capacitor are recommended in this case. This filter is not required operation.

11.2.2.4.2 *Output Capacitor*

For the output capacitor, it is recommended to use small X5R or X7R ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, using a smaller ceramic capacitor in parallel to the large one is required. This small capacitor should be placed as close as possible to the VOUT and PGND pins of the IC.

To get an estimate of the recommended minimum output capacitance, Equation 5 can be used.

$$C_{OUT} = 5 \times L \times \frac{\mu F}{\mu H} \quad (5)$$

A capacitor with a value in the range of the calculated minimum should be used. This is required to maintain control loop stability. There are no additional requirements regarding minimum ESR. There is also no upper limit for the output capacitance value. Larger capacitors cause lower output voltage ripple as well as lower output voltage drops during load transients.

11.2.2.4.3 Capacitor at VAUX

Between the VAUX pin and GND pin, a capacitor must be connected. This capacitor is used to maintain and filter the control supply voltage, which is chosen from the highest of VIN, VOUT, and L. It is charged during startup and before the main output VOUT is turned on. To ensure stable operation, using at least 0.1µF is recommended. At output voltages below 2.5 V, the capacitance should be in the range of 1 µF. Since this capacitor is also used as a snubber capacitor for the main switch, using a X5R or X7R ceramic capacitor with low ESR is important.

11.2.3 Application Curves

	FIGURE
Output Voltage TPS61201, Power Save Mode Disabled	Figure 16
Output Voltage TPS61202, Power Save Mode Disabled	Figure 17
Output Voltage TPS61201, Power Save Mode Enabled	Figure 18
Output Voltage TPS61202, Power Save Mode Enabled	Figure 19
TPS61201 Load Transient Response	Figure 20
TPS61202 Load Transient Response	Figure 21
TPS61201 Line Transient Response	Figure 22
TPS61202 Line Transient Response	Figure 23
TPS61201 Startup after Enable	Figure 24
TPS61202 Startup after Enable	Figure 25

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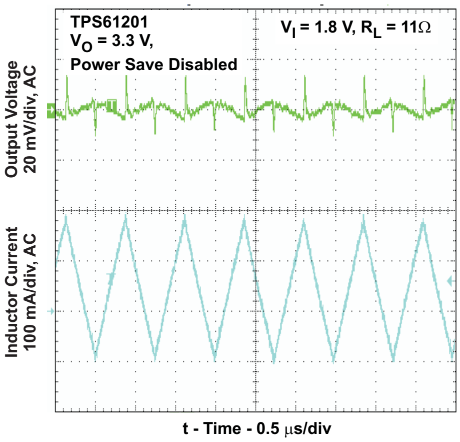

Figure 16. Output Voltage, Power Save Mode Disabled

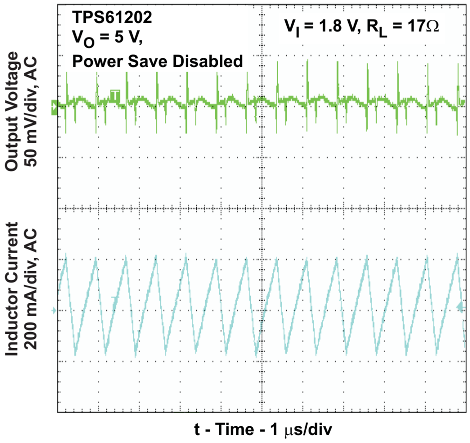

Figure 17. Output Voltage, Power Save Mode Disabled

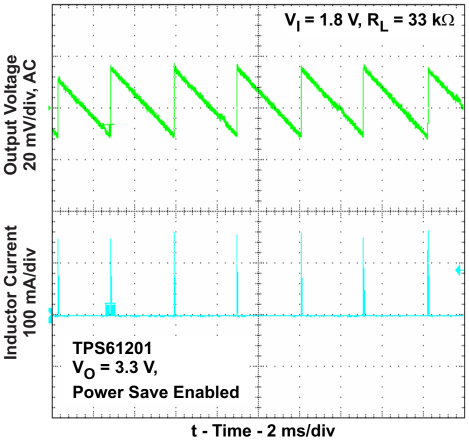

Figure 18. Output Voltage in Power Save Mode

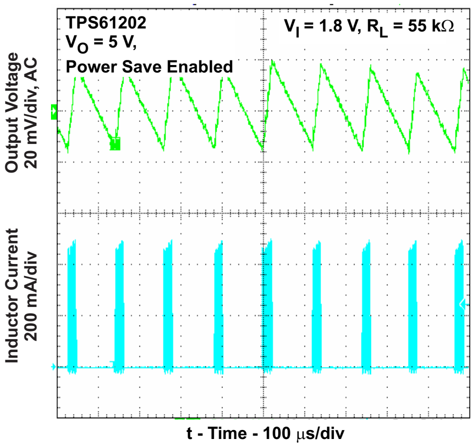

Figure 19. Output Voltage in Power Save Mode

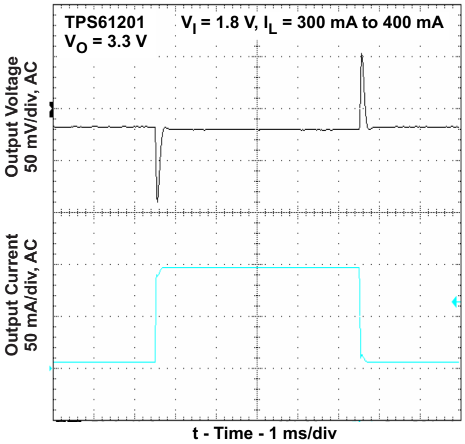

Figure 20. Load Transient Response

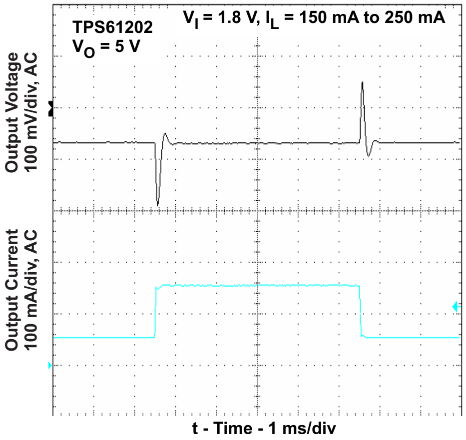

Figure 21. Load Transient Response

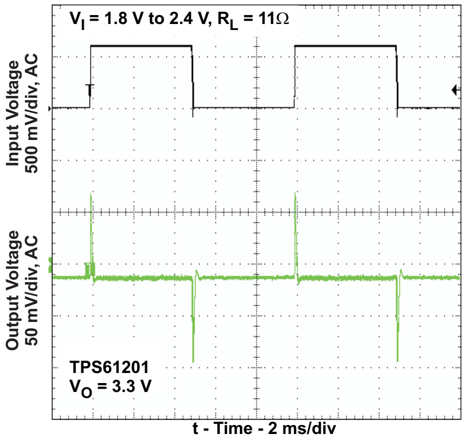

Figure 22. Line Transient Response

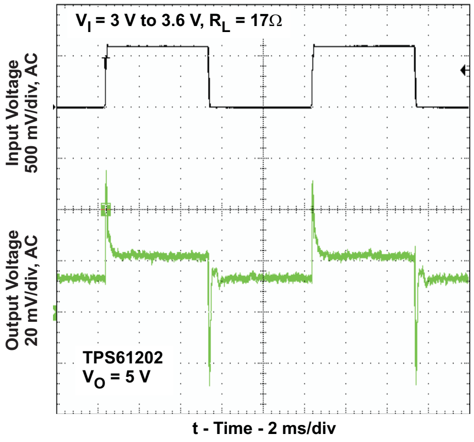

Figure 23. Line Transient Response

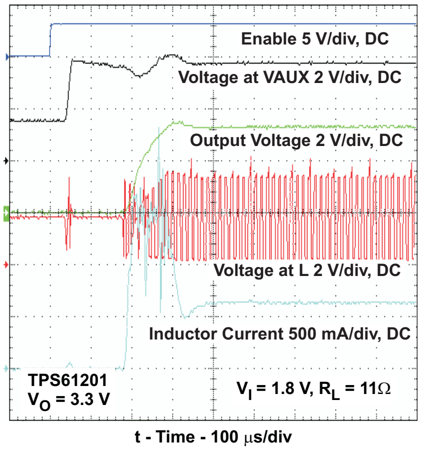

Figure 24. Start-Up After Enable

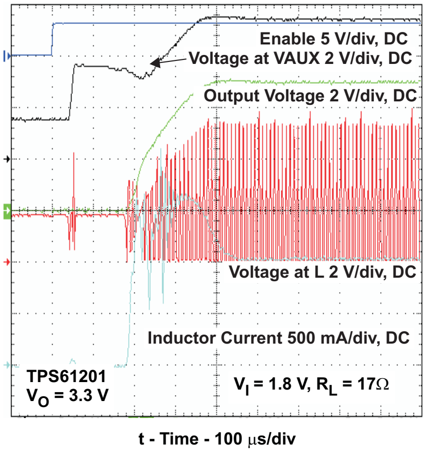

Figure 25. Start-Up After Enable

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11.3 System Examples

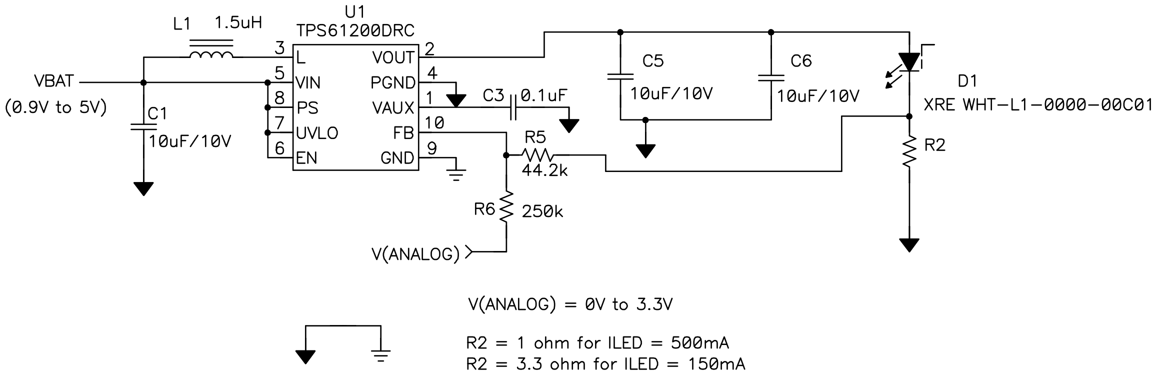
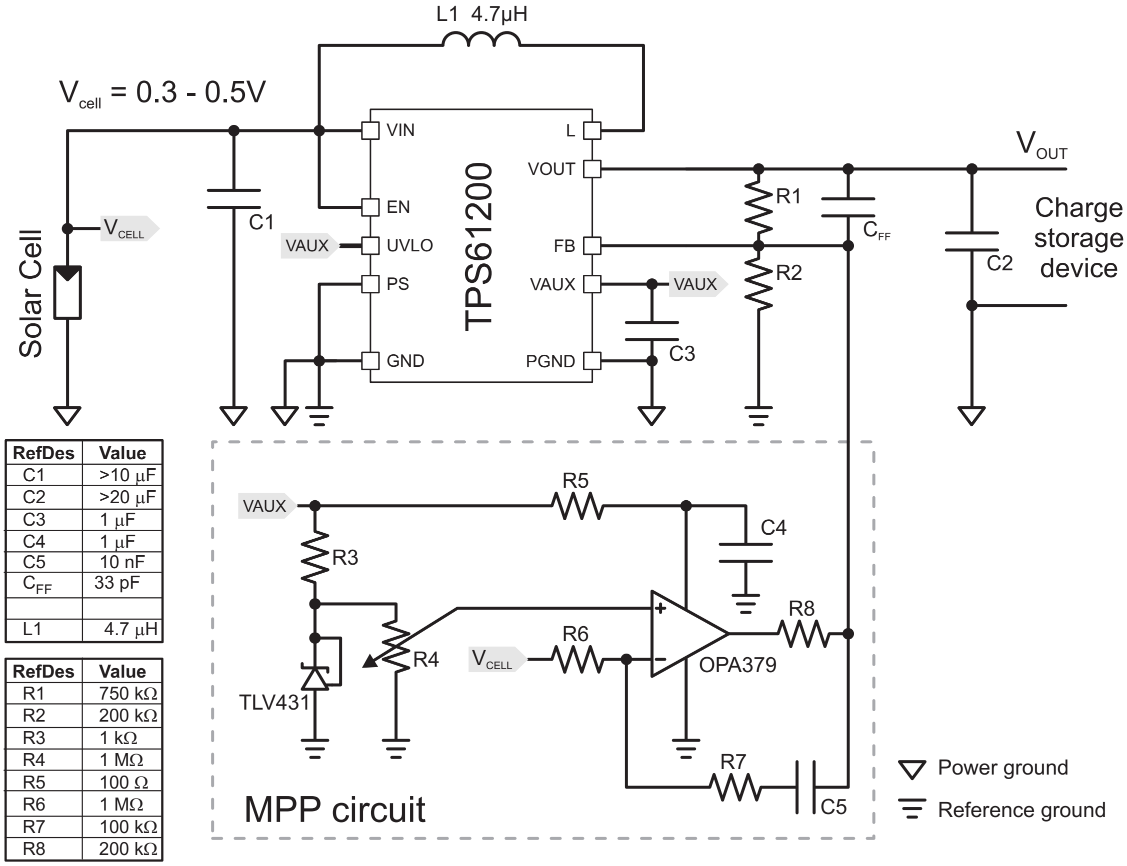


Figure 26. WLED Driver Circuit (See SLVA364)



RefDes	Value
C1	>10 µF
C2	>20 µF
C3	1 µF
C4	1 µF
C5	10 nF
C_{FF}	33 pF
L1	4.7 µH

RefDes	Value
R1	750 kΩ
R2	200 kΩ
R3	1 kΩ
R4	1 MΩ
R5	100 Ω
R6	1 MΩ
R7	100 kΩ
R8	200 kΩ

Figure 27. Solar Cell Circuit (See SLVA345)

System Examples (continued)

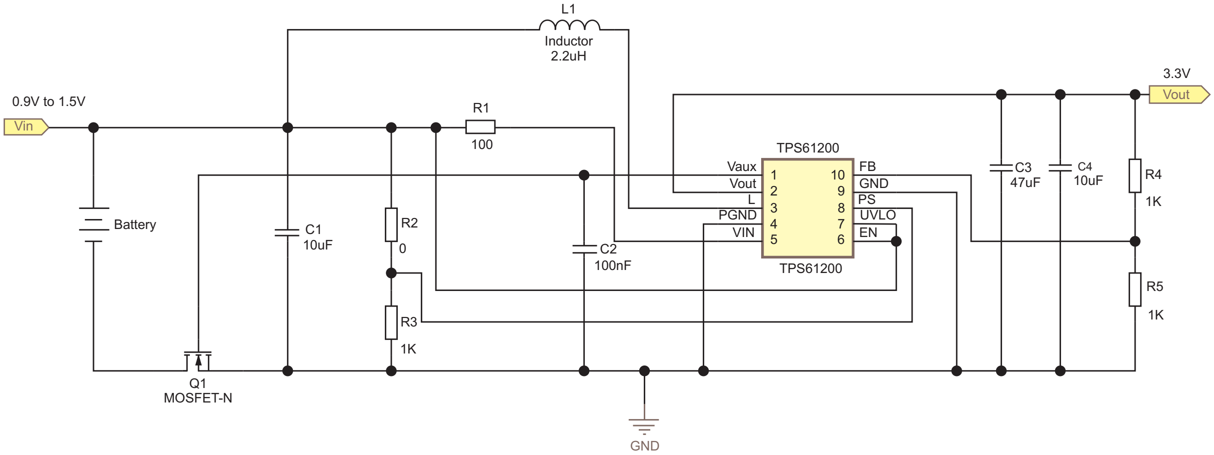


Figure 28. Reverse Battery Protection Circuit (See SLVA315)

12 Power Supply Recommendations

The power supply of TPS6120x DC-DC converters can be a single up to triple cell Alkaline, NiCd, NiMH battery with a typical terminal voltage between 0.7 V and 5.5 V. The TPS6120x can also be powered by one-cell Li-Ion or Li-Polymer with a typical voltage between 2.5 V and 4.2 V. Additionally, any other voltage source like solar cells or fuel cells with a typical output voltage between 0.3 V and 5.5 V can also be the power supply.

The input supply should be well regulated with the rating of TPS6120x. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

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13 Layout

13.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input and output capacitor, as well as the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current. See Figure 29 for the recommended layout.

13.2 Layout Example

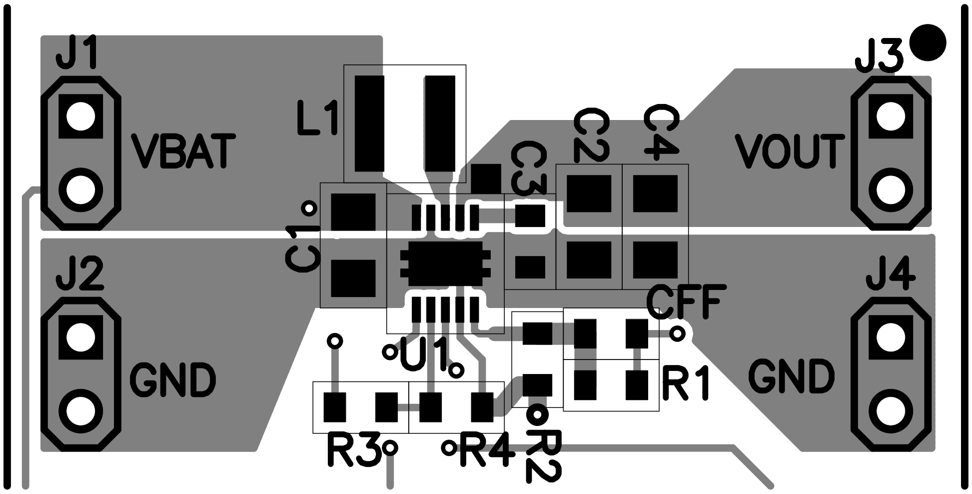

Figure 29. EVM Layout

13.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

The maximum recommended junction temperature (T_J) of the TPS6120x devices is 125°C. The thermal resistance of the 10-pin SON 3 × 3 package (DRC) is $R_{\theta JA}$ = 41.2 °C/W, when the exposed thermal pad is soldered. Specified regulator operation is assured to a maximum ambient temperature, T_A, of 85°C. Therefore, the maximum power dissipation is about 971 mW. More power can be dissipated if the maximum ambient temperature of the application is lower.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{125°C - 85°C}{41.2°C / W} = 971\,mW \tag{6}$$

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14 Device and Documentation Support

14.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61200	Click here	Click here	Click here	Click here	Click here
TPS61201	Click here	Click here	Click here	Click here	Click here
TPS61202	Click here	Click here	Click here	Click here	Click here

14.2 Trademarks

All trademarks are the property of their respective owners.

14.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61200DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRR	Samples
TPS61200DRCRG4	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRR	Samples
TPS61200DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRR	Samples
TPS61200DRCTG4	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRR	Samples
TPS61201DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRS	Samples
TPS61201DRCRG4	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRS	Samples
TPS61201DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRS	Samples
TPS61201DRCTG4	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRS	Samples
TPS61202DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRT	Samples
TPS61202DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRT	Samples
TPS61202DRCTG4	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRT	Samples
TPS61202DSCR	ACTIVE	WSON	DSC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CER	Samples
TPS61202DSCT	ACTIVE	WSON	DSC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CER	Samples
TPS61202DSCTG4	ACTIVE	WSON	DSC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CER	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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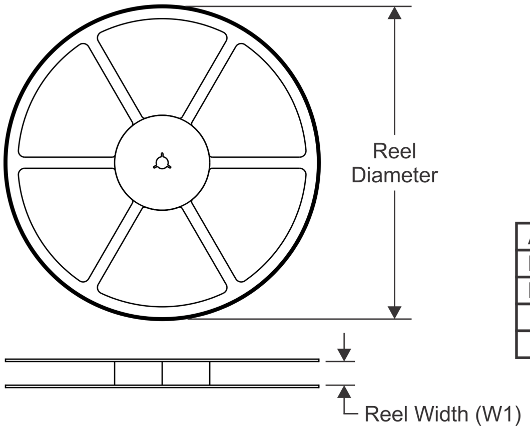
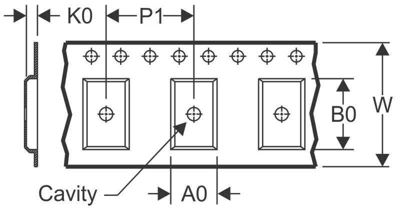
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

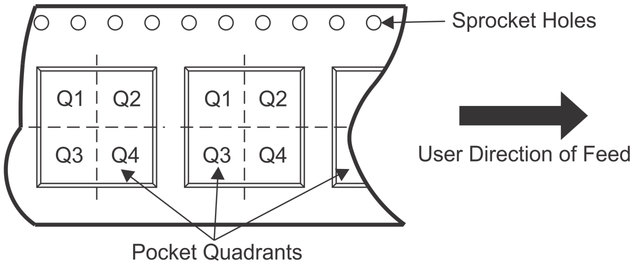


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

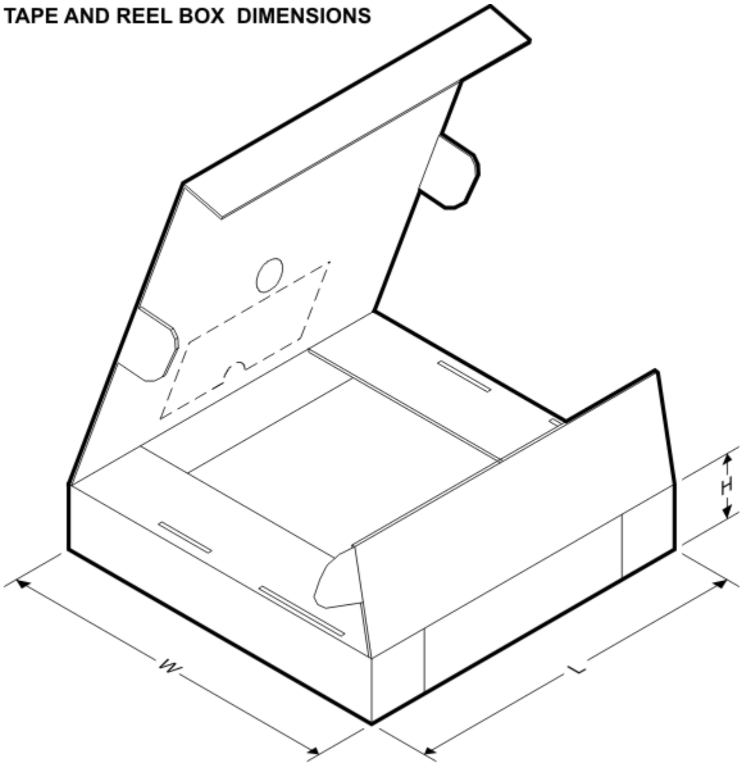
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61200DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61200DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61200DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61200DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61201DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61201DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61201DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61201DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61202DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61202DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61202DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61202DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61202DSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61202DSCT	WSON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

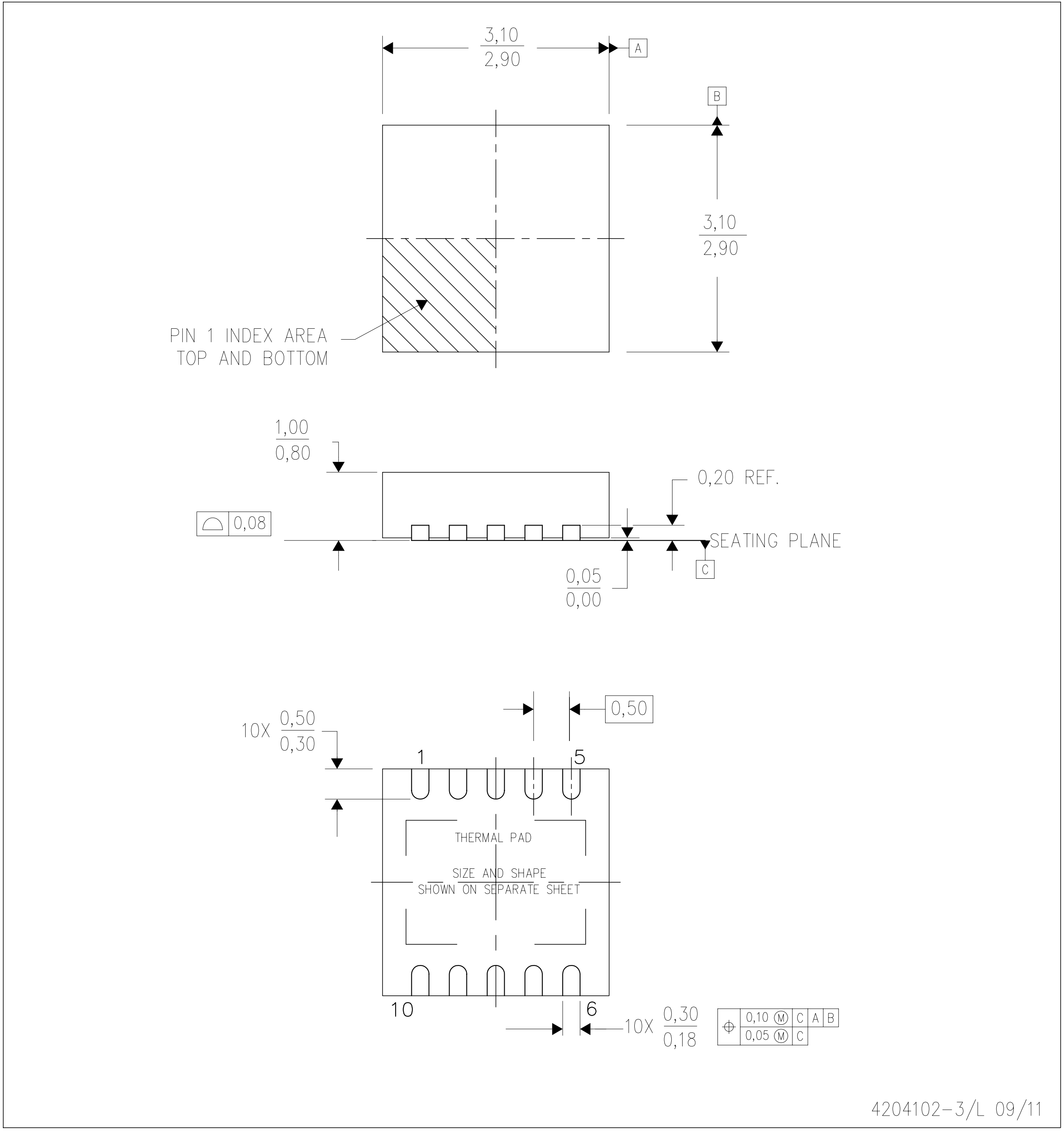
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61200DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS61200DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS61200DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS61200DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS61201DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS61201DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS61201DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS61201DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS61202DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS61202DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS61202DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS61202DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS61202DSCR	WSON	DSC	10	3000	367.0	367.0	35.0
TPS61202DSCT	WSON	DSC	10	250	210.0	185.0	35.0

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No–Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

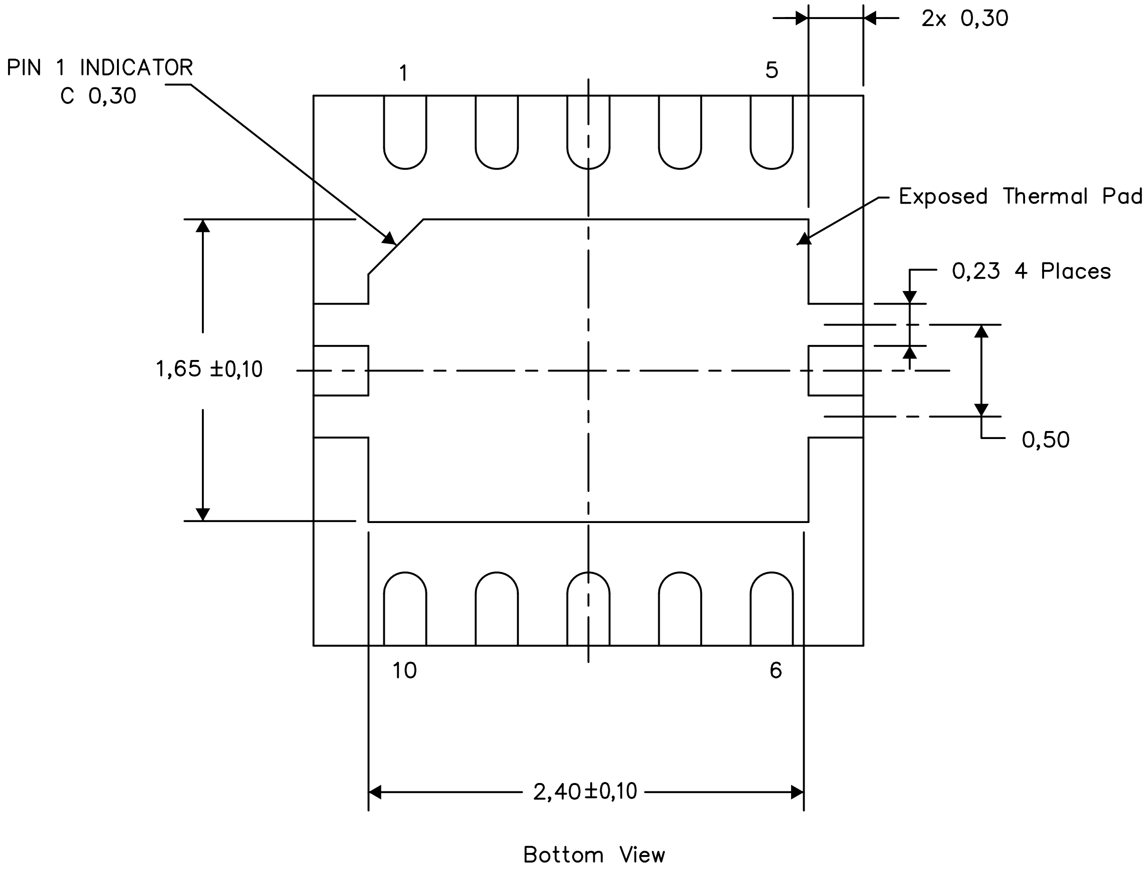
DRC (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

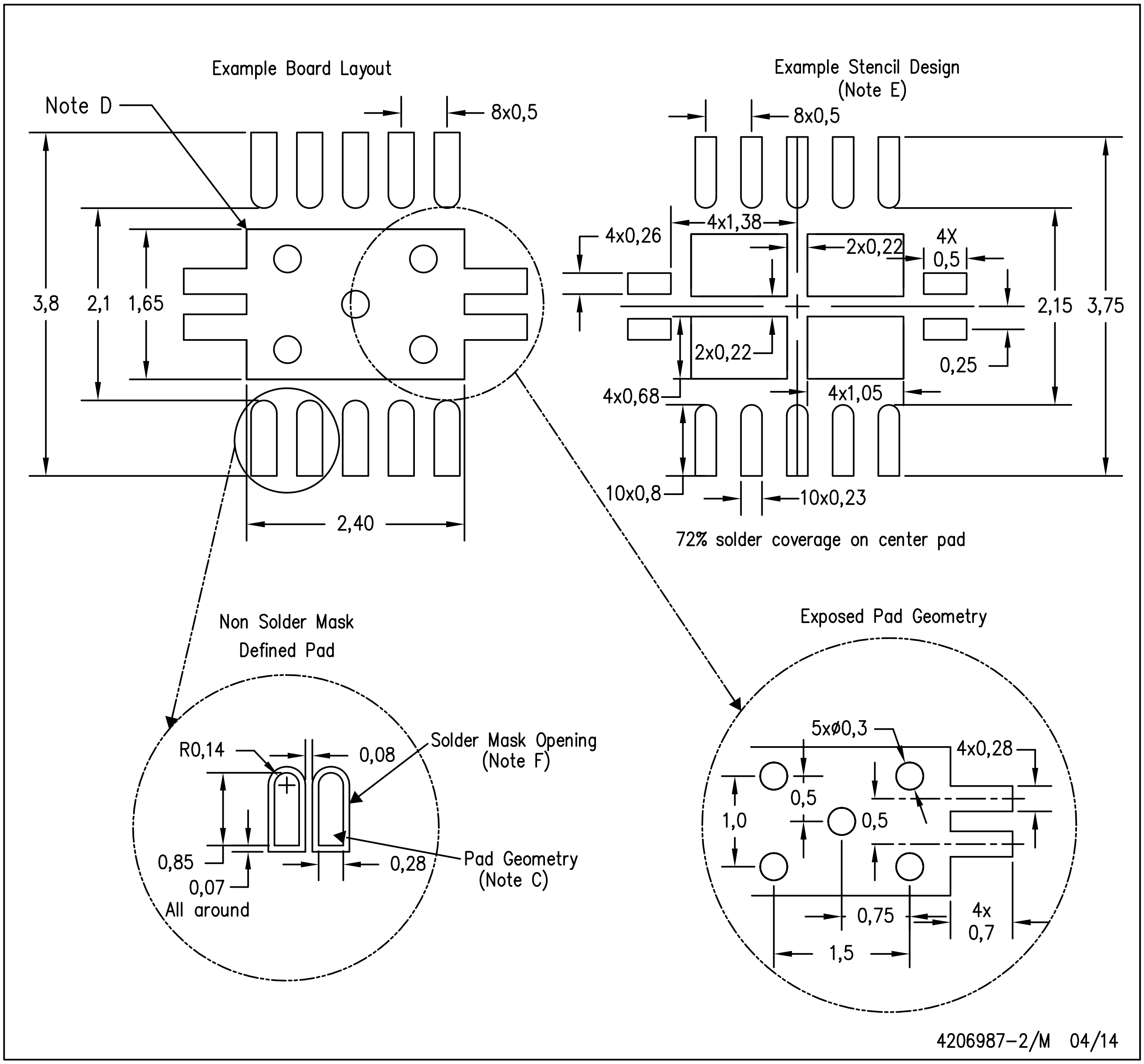


Exposed Thermal Pad Dimensions

4206565-3/U 04/14

NOTE: A. All linear dimensions are in millimeters

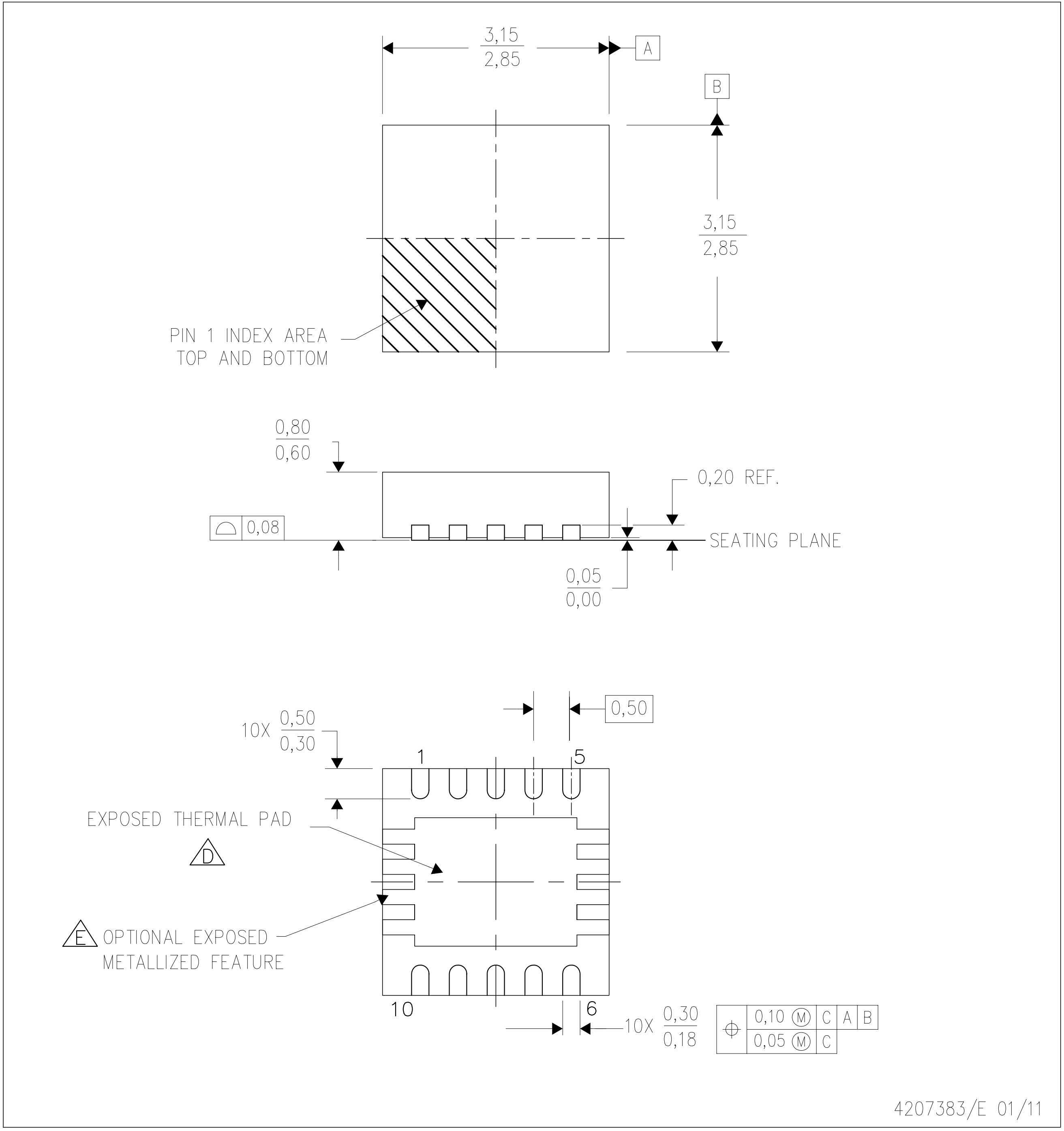
DRC (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD



4206987-2/M 04/14

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DSC (S-PWSON-N10) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No–Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

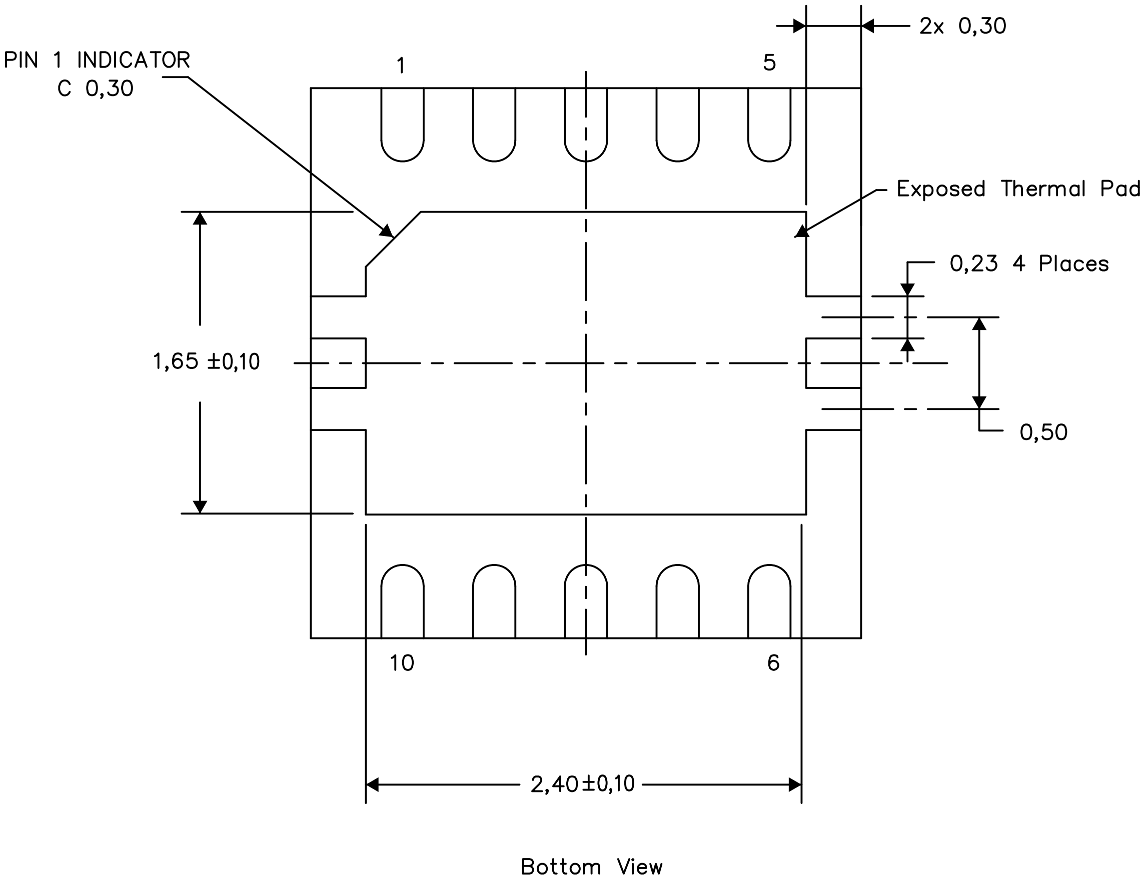
DSC (S-PWSON-N10) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

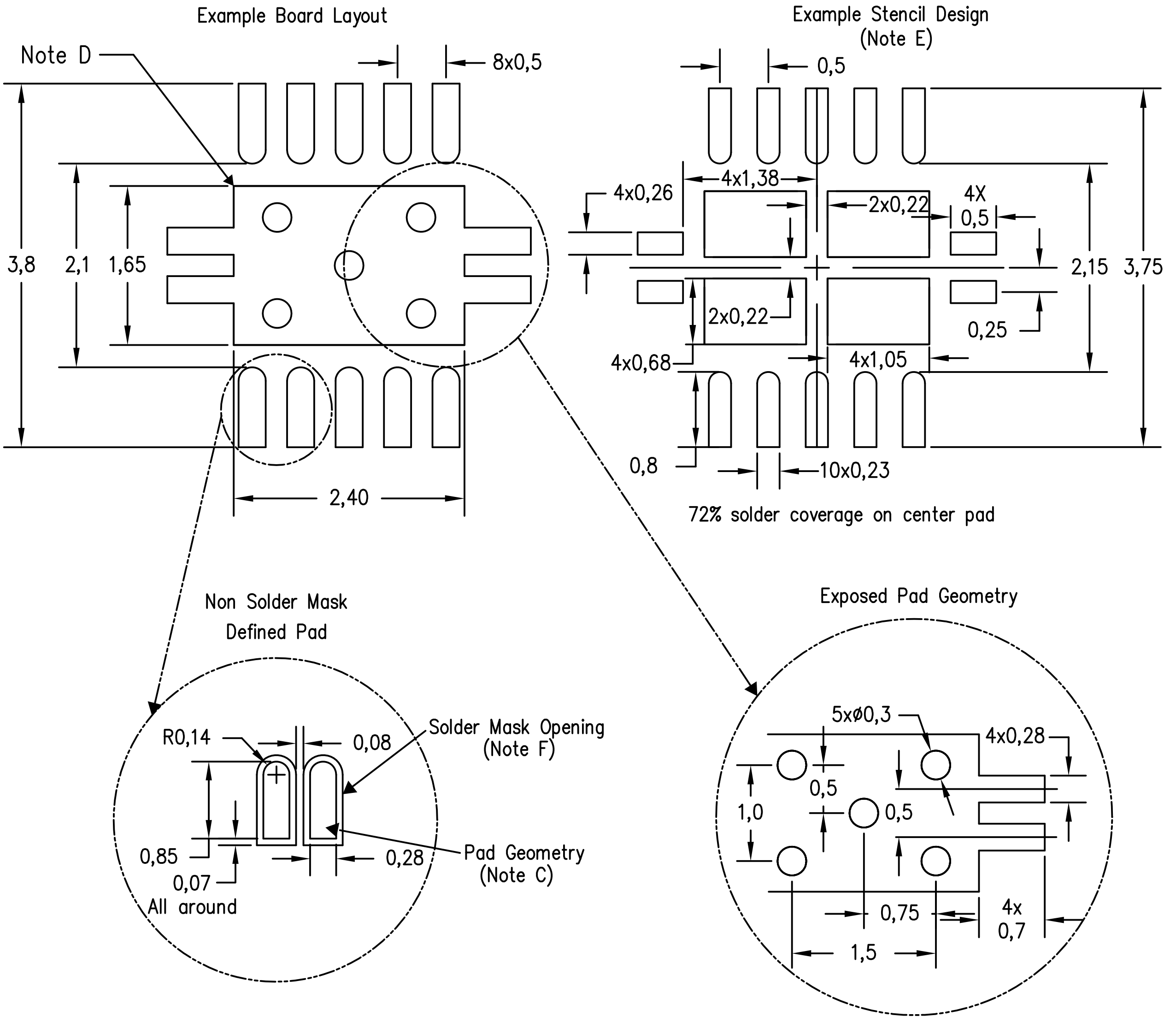


Exposed Thermal Pad Dimensions

4210391-2/N 01/14

NOTE: A. All linear dimensions are in millimeters

DSC (S-PWSON-N10) PLASTIC SMALL OUTLINE NO-LEAD



4210390-2/J 01/14

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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