ULTRALOW-NOISE, HIGH-PSRR, FAST RF 200-mA LOW-DROPOUT LINEAR REGULATORS

Check for Samples: TPS79301-Q1, TPS79318-Q1, TPS79325-Q1, TPS79328-Q1, TPS793285-Q1, TPS79330-Q1, TPS79333-Q1

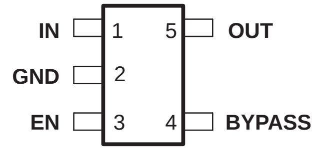
FEATURES

- **Qualified For Automotive Applications**
- **200-mA Low-Dropout Regulator With EN**
- **Available in 1.8-V, 2.5-V, 2.8-V, 2.85-V, 3-V, 3.3-V, 4.75-V, and Adjustable Options**
- **High PSRR (70 dB at 10 kHz)**
- **Ultralow Noise (32 μV)**
- **Fast Start-Up Time (50 μs)**
- **Stable With a 2.2-μF Ceramic Capacitor**
- **Excellent Load/Line Transient**
- **Very Low Dropout Voltage (112 mV at Full Load, TPS79330)**
- **5-Pin SOT23 (DBV) Package**

APPLICATIONS

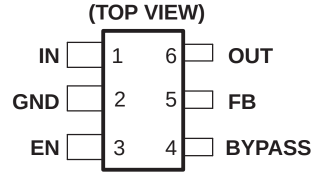
- **VCOs**
- **RF**
- **Bluetooth™**

DBV PACKAGE (TOP VIEW)



Fixed Option

DBV PACKAGE (TOP VIEW)



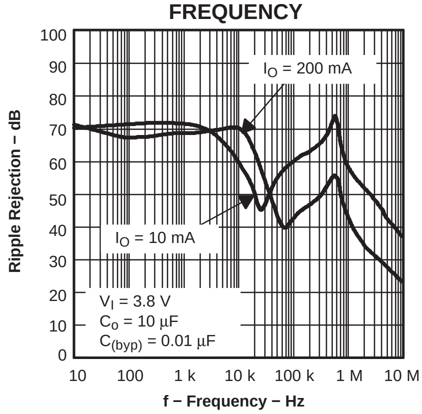
Adjustable Option

DESCRIPTION

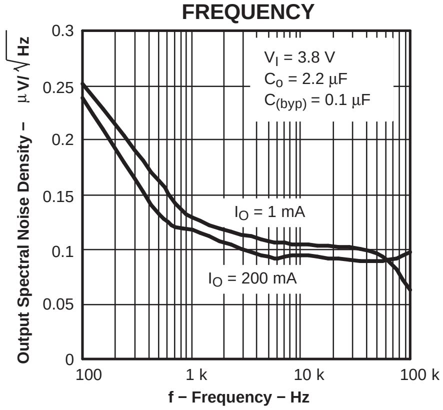
The TPS793xx family of low-dropout (LDO) low-power linear voltage regulators features high power-supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in a small-outline SOT23 package. Each device in the family is stable, with a small 2.2-μF ceramic capacitor on the output. The TPS793xx family uses an advanced, proprietary, BiCMOS fabrication process to yield extremely low dropout voltages (e.g., 112 mV at 200 mA, TPS79330). Each device achieves fast start-up times (approximately 50 μs with a 0.001-μF bypass capacitor), while consuming very low quiescent current (170 μA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 μA. The TPS79328 exhibits approximately 32 μV_{RMS} of output voltage noise with a 0.1-μF bypass capacitor. Applications with analog components that are noise sensitive, such as portable RF electronics, benefit from the high PSRR and low-noise features, as well as the fast response time.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TPS79328
RIPPLE REJECTION
vs
FREQUENCY



TPS79328
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY



ORDERING INFORMATION(1)

T_A	OUTPUT VOLTAGE	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	1.2 to 5.5 V	SOT23 – DBV	Reel of 3000	TPS79301DBVRQ1	PGV1
	1.8 V			TPS79318DBVRQ1	PHH1
	2.5 V			TPS79325DBVRQ1	PGW1
	2.8 V			TPS79328DBVRQ1	PGX1
	2.85 V			TPS793285QDBVRQ1	PHI1
	3 V			TPS79330QDBVRQ1	PGY1
	3.3 V			TPS79333DBVRQ1	PHU1
	4.75 V			TPS793475QDBVRQ1(3)	PHJ1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) Product preview

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Input voltage range[2]		–0.3	6	V
	Voltage range at EN		–0.3	V_I + 0.3	V
	Voltage on OUT		–0.3	6	V
	Peak output current		Internally limited		
	ESD rating	Human-Body Model (HBM)		2000	V
		Charged-Device Model (CDM)		250	
	Continuous total power dissipation		See Dissipation Rating Table		
T_J	Operating junction temperature range		–40	150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le$ 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low K[1]	DBV	63.75°C/W	256°C/W	3.906 mW/°C	391 mW	215 mW	156 mW
High K[2]	DBV	63.75°C/W	178.3°C/W	5.609 mW/°C	561 mW	308 mW	224 mW

(1) The JEDEC low K (1s) board design used to derive this data was a 3-in × 3-in, two layer board with 2-oz copper traces on top of the board.
(2) The JEDEC high K (2s2p) board design used to derive this data was a 3-in × 3-in, multilayer board with 1-oz internal power and ground planes and 2-oz copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, EN = V_I, T_J = –40 to 125°C, V_I = $V_{O(typ)}$ + 1 V, I_O = 1 mA, C_o = 10 μF, $C_{(byp)}$ = 0.01 μF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I Input voltage (1)				2.7		5.5	V
I_O Continuous output current				0		200	mA
T_J Operating junction temperature				–40		125	°C
Output voltage	TPS79301-Q1	0 μA < I_O < 200 mA		V_{FB}		5.5 – V_{FB}	V
	TPS79318-Q1	T_J = 25°C			1.8		
		0 μA < I_O < 200 mA,	2.8 V < V_I < 5.5 V	1.764		1.836	
	TPS79325-Q1	T_J = 25°C			2.5		
		0 μA < I_O < 200 mA,	3.5 V < V_I < 5.5 V	2.45		2.55	
	TPS79328-Q1	T_J = 25°C			2.8		
		0 μA < I_O < 200 mA,	3.8 V < V_I < 5.5 V	2.744		2.856	
	TPS793285-Q1	T_J = 25°C			2.85		
		0 μA < I_O < 200 mA,	3.85 V < V_I < 5.5 V	2.793		2.907	
	TPS79330-Q1	T_J = 25°C			3		
		0 μA < I_O < 200 mA,	4 V < V_I < 5.5 V	2.94		3.06	
	TPS79333-Q1	T_J = 25°C			3.3		
		0 μA < I_O < 200 mA,	4.3 V < V_I < 5.5 V	3.234		3.366	
	TPS793475-Q1	T_J = 25°C			4.75		
		0 μA < I_O < 200 mA,	5.25 V < V_I < 5.5 V	4.655		4.845	
Quiescent current (GND current)		0 μA < I_O < 200 mA,	T_J = 25°C		170		μA
		0 μA < I_O < 200 mA				220	
Load regulation		0 μA < I_O < 200 mA,	T_J = 25°C		5		mV
Output voltage line regulation ($\Delta V_O/V_O$)		V_O + 1 V < V_I ≤ 5.5 V,	T_J = 25°C		0.05		%/V
		V_O + 1 V < V_I ≤ 5.5 V				0.12	
Output noise voltage	TPS79328-Q1	BW = 200 Hz to 100 kHz, I_O = 200 mA, T_J = 25°C	$C_{(byp)}$ = 0.001 μF		55		μV_{RMS}
			$C_{(byp)}$ = 0.0047 μF		36		
			$C_{(byp)}$ = 0.01 μF		33		
			$C_{(byp)}$ = 0.1 μF		32		
Time, start-up	TPS79328-Q1	R_L = 14 Ω, C_o = 1 μF, T_J = 25°C	$C_{(byp)}$ = 0.001 μF		50		μs
			$C_{(byp)}$ = 0.0047 μF		70		
			$C_{(byp)}$ = 0.01 μF		100		
Output current limit		V_O = 0 V		285		600	mA
Standby current (2)		EN = 0 V,	2.7 V < V_I < 5.5 V		0.07	1	μA
High-level enable input voltage		2.7 V < V_I < 5.5 V		2			V
Low-level enable input voltage		2.7 V < V_I < 5.5 V				0.7	V
Input current (EN)		EN = 0		–1		1	μA
Input current (FB)	TPS79301-Q1	FB = 1.8 V				1	μA
Internal reference, V_{FB}	TPS79301-Q1			1.201	1.225	1.250	V
Power-supply ripple rejection	TPS79328-Q1	f = 100 Hz, T_J = 25°C,	I_O = 10 mA		70		dB
			I_O = 200 mA		68		
		f = 10 kHz, T_J = 25°C,	I_O = 200 mA		70		
		f = 100 kHz, T_J = 25°C,			43		

(1) Minimum V_{IN} is 2.7V or VOUT + VDO, whichever is greater.
(2) For adjustable versions, this parameter applies only after V_{IN} is applied; then V_{EN} transitions high to low.

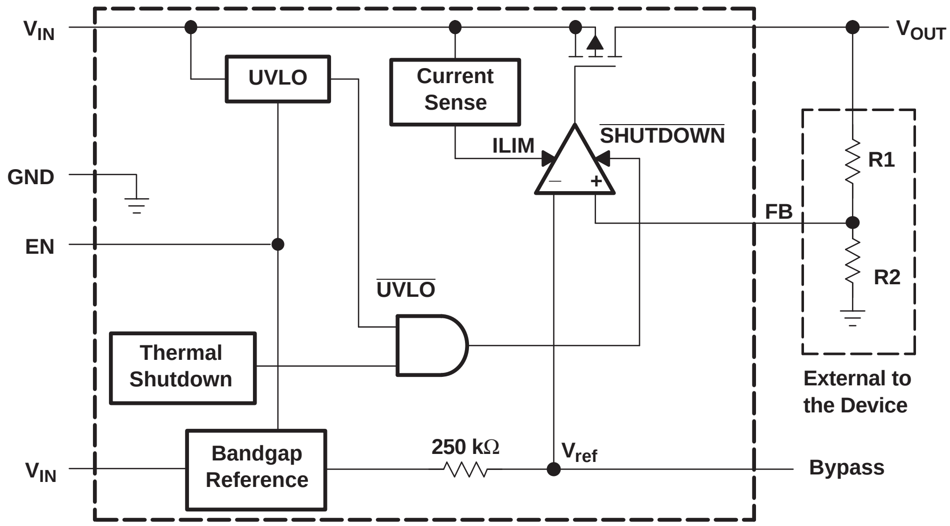
ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range, EN = V_I, T_J = –40 to 125°C, V_I = $V_{O(typ)}$ + 1 V, I_O = 1 mA, C_o = 10 μF, $C_{(byp)}$ = 0.01 μF (unless otherwise noted)

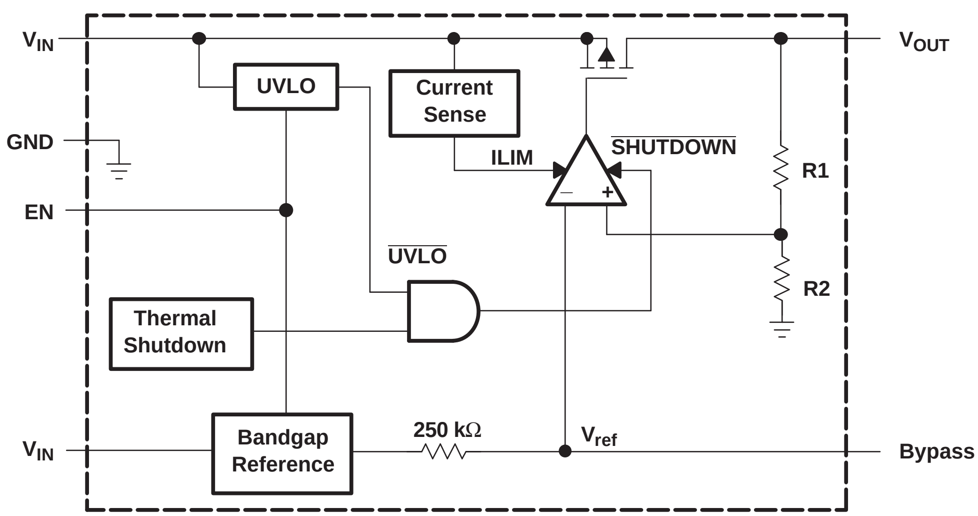
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Dropout voltage(3)	TPS79328-Q1	I_O = 200 mA,	T_J = 25°C		120		mV
		I_O = 200 mA				200	
	TPS793285-Q1	I_O = 200 mA,	T_J= 25°C		120		
		I_O = 200 mA				200	
	TPS79330-Q1	I_O = 200 mA,	T_J = 25°C		112		
		I_O = 200 mA				200	
	TPS79333-Q1	I_O = 200 mA,	T_J = 25°C		102		
		I_O = 200 mA				180	
	TPS793475-Q1	I_O = 200 mA,	T_J = 25°C		77		
		I_O = 200 mA				125	
UVLO threshold		V_{CC} rising		2.25		2.65	V
UVLO hysteresis		T_J = 25°C	V_{CC} rising		100		mV

(3) Dropout is not measured for the TPS79318-Q1 and TPS79325-Q1 since minimum V_{IN} = 2.7 V.

FUNCTIONAL BLOCK DIAGRAM – ADJUSTABLE VERSION



FUNCTIONAL BLOCK DIAGRAM – FIXED VERSION



TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	ADJ	FIXED		
BYPASS	4	4		An external bypass capacitor, connected to this terminal, in conjunction with an internal resistor, creates a low-pass filter to further reduce regulator noise.
EN	3	3	I	Enable input that enables or shuts down the device. When EN goes to a logic high, the device is enabled. When the device goes to a logic low, the device is in shutdown mode.
FB	5	N/A	I	Feedback input voltage for the adjustable device
GND	2	2		Regulator ground
IN	1	1	I	Input to the device
OUT	6	5	O	Regulated output of the device

TYPICAL CHARACTERISTICS

TPS79328
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

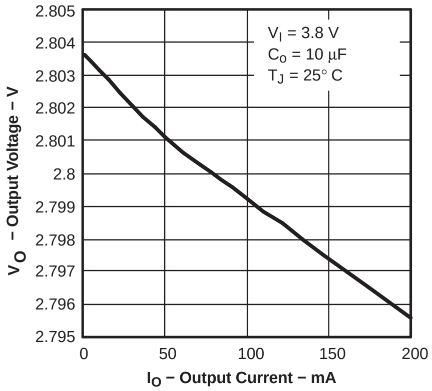


Figure 1.

TPS79328
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

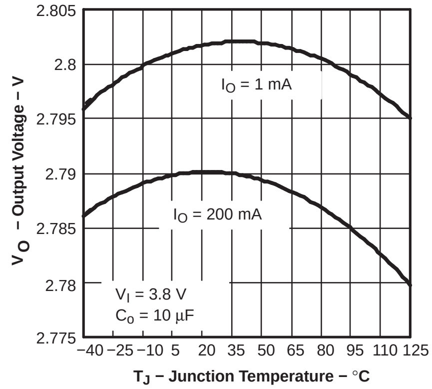


Figure 2.

TPS79328
GROUND CURRENT
vs
JUNCTION TEMPERATURE

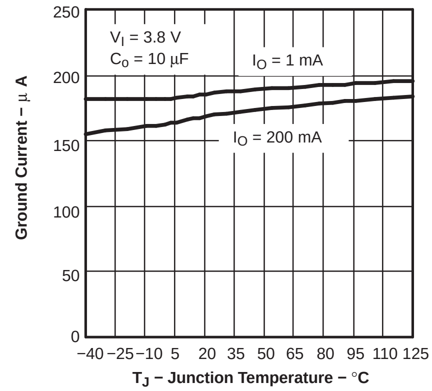


Figure 3.

TPS79328
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

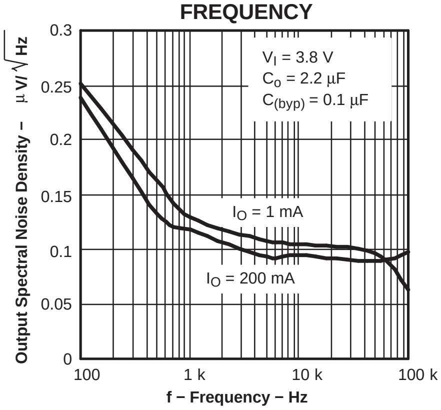


Figure 4.

TPS79328
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

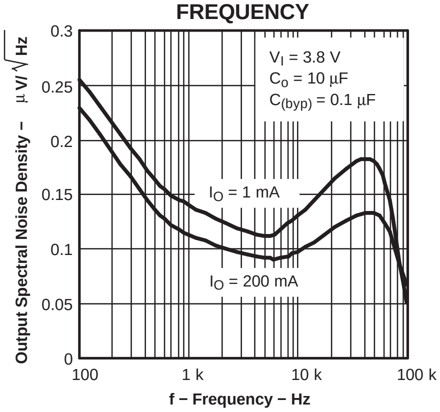


Figure 5.

TPS79328
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

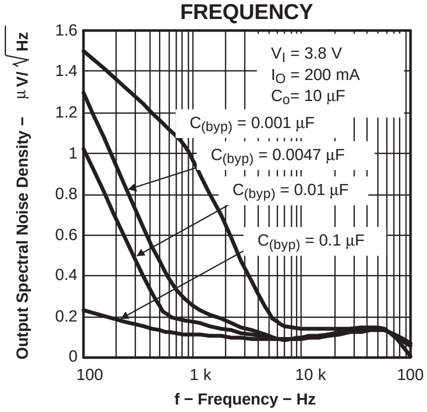


Figure 6.

ROOT MEAN SQUARED OUTPUT NOISE
vs
BYPASS CAPACITANCE

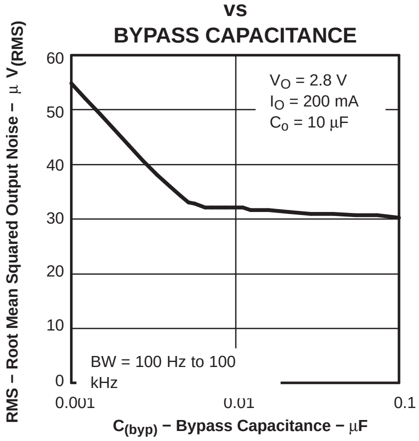


Figure 7.

OUTPUT IMPEDANCE
vs
FREQUENCY

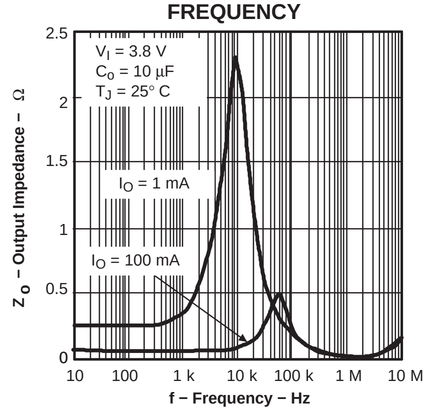


Figure 8.

TPS79328
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

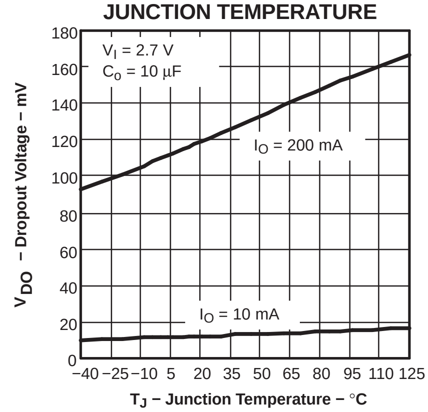


Figure 9.

TYPICAL CHARACTERISTICS (continued)

TPS79328
RIPPLE REJECTION
vs
FREQUENCY

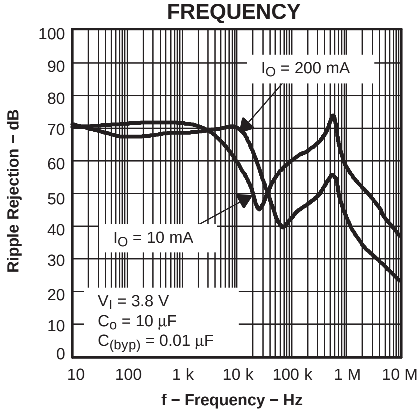


Figure 10.

TPS79328
RIPPLE REJECTION
vs
FREQUENCY

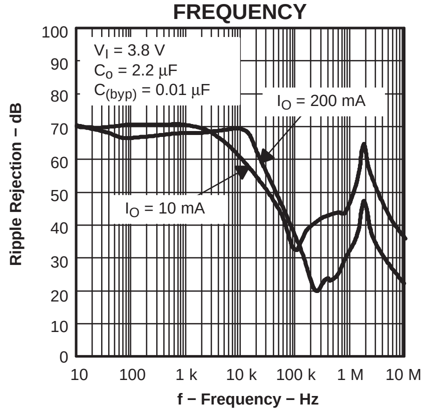


Figure 11.

TPS79328
RIPPLE REJECTION
vs
FREQUENCY

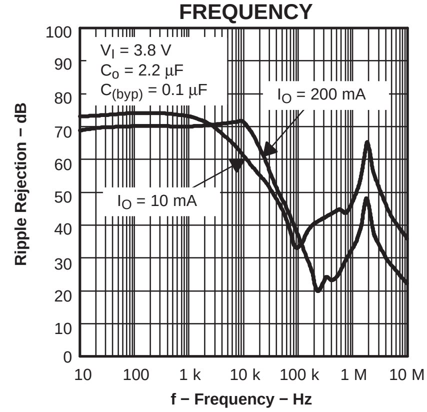


Figure 12.

TPS79328
OUTPUT VOLTAGE, ENABLE VOLTAGE
vs
TIME (START-UP)

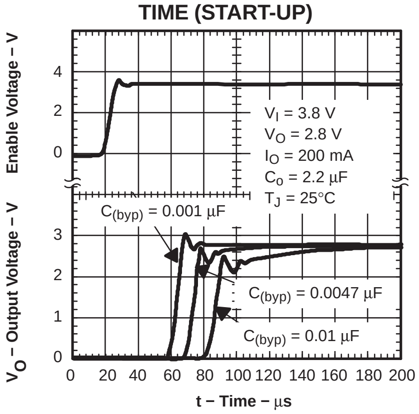


Figure 13.

TPS79328
LINE TRANSIENT RESPONSE

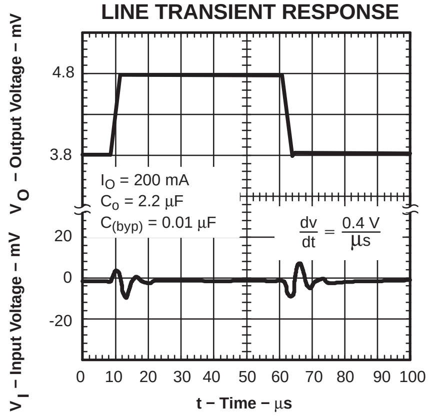


Figure 14.

TPS79328
LOAD TRANSIENT RESPONSE

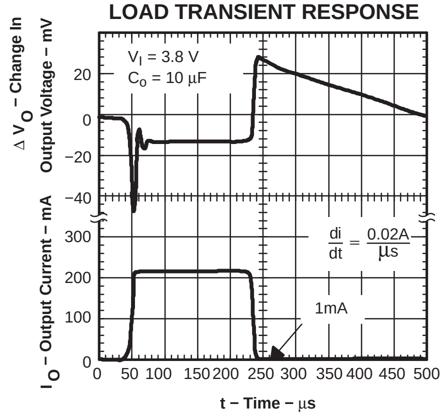


Figure 15.

POWER UP / POWER DOWN

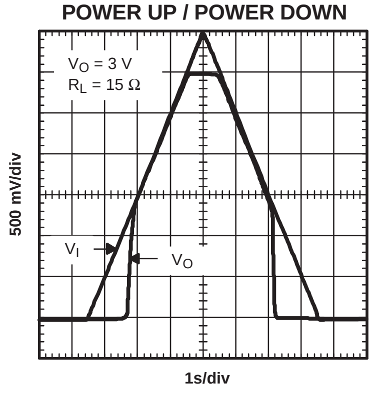


Figure 16.

DC DROPOUT VOLTAGE
vs
OUTPUT CURRENT

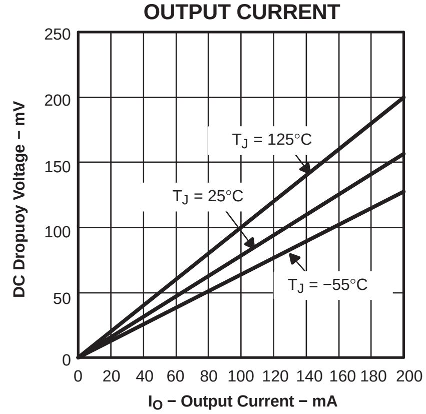


Figure 17.

TPS79301
DROPOUT VOLTAGE
vs
INPUT VOLTAGE

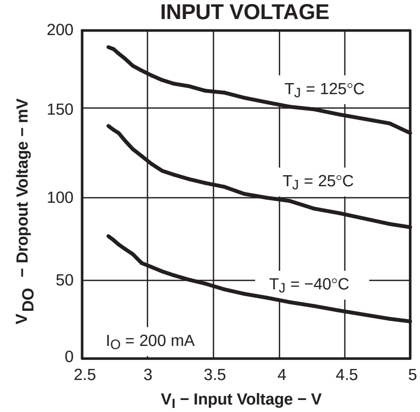


Figure 18.

TYPICAL CHARACTERISTICS (continued)

MINIMUM REQUIRED INPUT VOLTAGE vs OUTPUT VOLTAGE

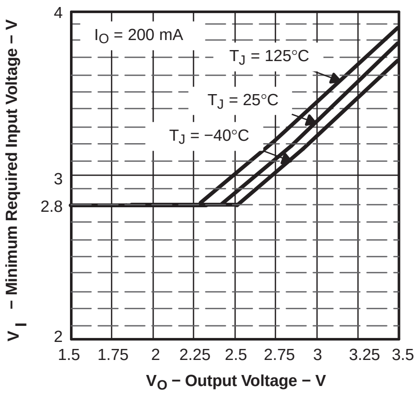


Figure 19.

TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

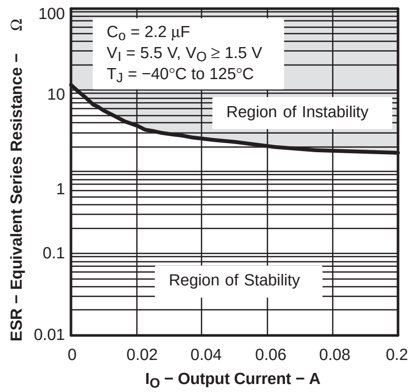


Figure 20.

TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

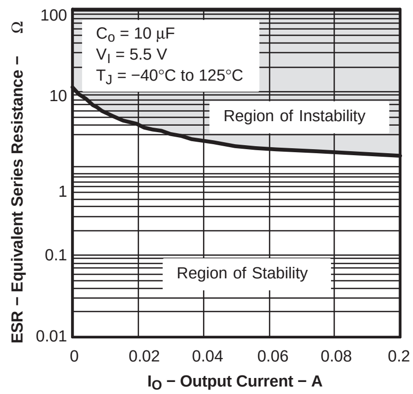


Figure 21.

APPLICATION INFORMATION

The TPS793xx family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (170 μA typically), and enable-input to reduce supply currents to less than 1 μA when the regulator is turned off.

A typical application circuit is shown in Figure 22.

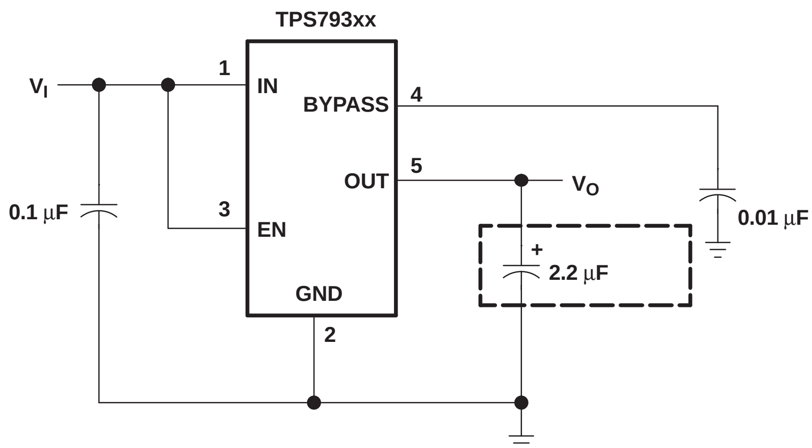


Figure 22. Typical Application Circuit

External Capacitor Requirements

A 0.1-μF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS793xx, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all LDOs, the TPS793xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 2.2-μF. Any 2.2-μF or larger ceramic capacitor is suitable, provided the capacitance does not vary significantly over temperature.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS793xx has a BYPASS pin that is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the BYPASS pin, creates a low pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the BYPASS pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus, creating an output error. Therefore, the bypass capacitor must have minimal leakage current.

For example, the TPS79328 exhibits only 32 μV_{RMS} of output voltage noise using a 0.1-μF ceramic bypass capacitor and a 2.2-μF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases due to the RC time constant at the BYPASS pin that is created by the internal 250-kΩ resistor and external capacitor.

Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac measurements like PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Power Dissipation and Junction Temperature

Specified regulator operation is ensured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum power dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (1)$$

Where:

$T_J$max = Maximum allowable junction temperature

$R\theta_{JA}$ = Thermal resistance, junction to ambient, for the package, see the dissipation rating table

T_A = Ambient temperature

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O \quad (2)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

Programming the TPS79301 Adjustable LDO Regulator

The output voltage of the TPS79301 adjustable regulator is programmed using an external resistor divider as shown in Figure 23. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

Where:

V_{ref} = 1.2246 V typical (the internal reference voltage)

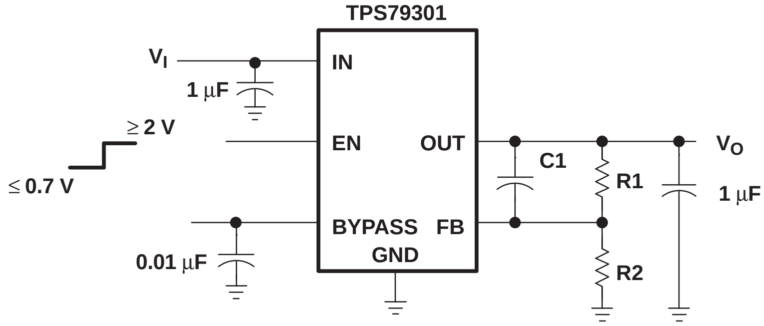
Resistors R1 and R2 should be chosen for approximately 50-μA divider current. Lower-value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R1/R2 creates an offset voltage that artificially increases/decreases the feedback voltage and, thus, erroneously decreases/increases V_O. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 μA, C1 = 15 pF for stability, and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (4)$$

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB. For voltages <1.8 V, the value of this capacitor should be 100 pF. For voltages >1.8 V, the approximate value of this capacitor can be calculated as:

$$C1 = \frac{(3 \text{ x } 10^{-7}) \text{ x } (R1 + R2)}{(R1 \text{ x } R2)} \quad (5)$$

The suggested value of this capacitor for several resistor ratios is shown in the table below. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage <1.8 V is chosen, then the minimum recommended output capacitor is 4.7 μF instead of 2.2 μF.



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	C1
2.5 V	31.6 kΩ	30.1 kΩ	22 pF
3.3 V	51 kΩ	30.1 kΩ	15 pF
3.6 V	59 kΩ	30.1 kΩ	15 pF

Figure 23. TPS79301 Adjustable LDO Regulator Programming

Regulator Protection

The TPS793xx features internal current limiting and thermal protection. During normal operation, the TPS793xx limits output current to approximately 400 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

The TPS793xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS79301DBVRG4Q1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGV1	Samples
TPS79301DBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGV1	Samples
TPS79318DBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHH1	Samples
TPS79318DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHH1	Samples
TPS79325DBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGW1	Samples
TPS79325DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGW1	Samples
TPS793285QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHI1	Samples
TPS79328QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGX1	Samples
TPS79330QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGY1	Samples
TPS79333DBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHU1	Samples
TPS79333DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHU1	Samples
TPS793475DBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHJ1	Samples
TPS793475DBVRQ1	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS79301-Q1, TPS79318-Q1, TPS79325-Q1, TPS79328-Q1, TPS793285-Q1, TPS79330-Q1, TPS79333-Q1, TPS793475-Q1 :

- Catalog: TPS79301, TPS79318, TPS79325, TPS79328, TPS793285, TPS79330, TPS79333, TPS793475

- Enhanced Product: TPS79301-EP, TPS79318-EP, TPS79325-EP, TPS79333-EP, TPS793475-EP

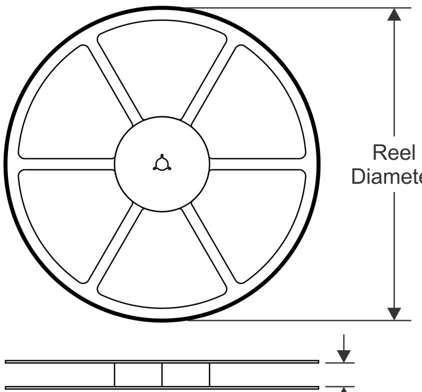
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

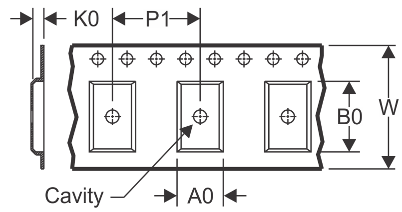
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

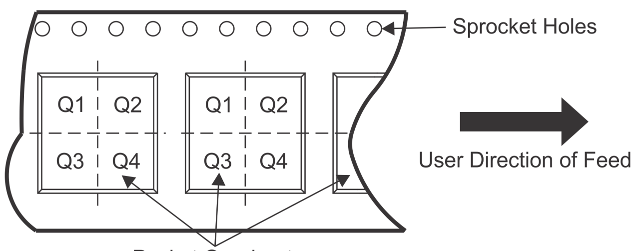


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

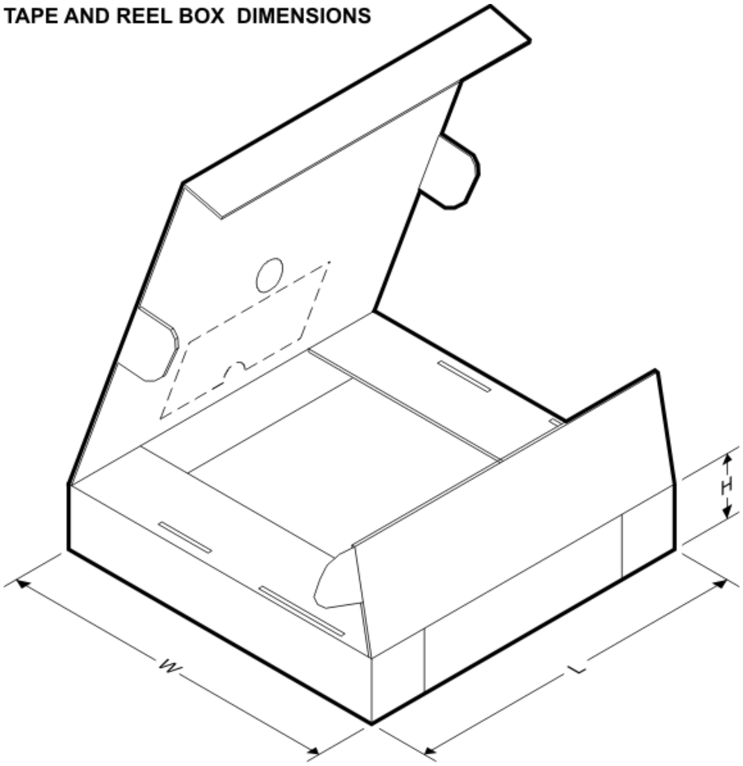
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79328QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79330QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

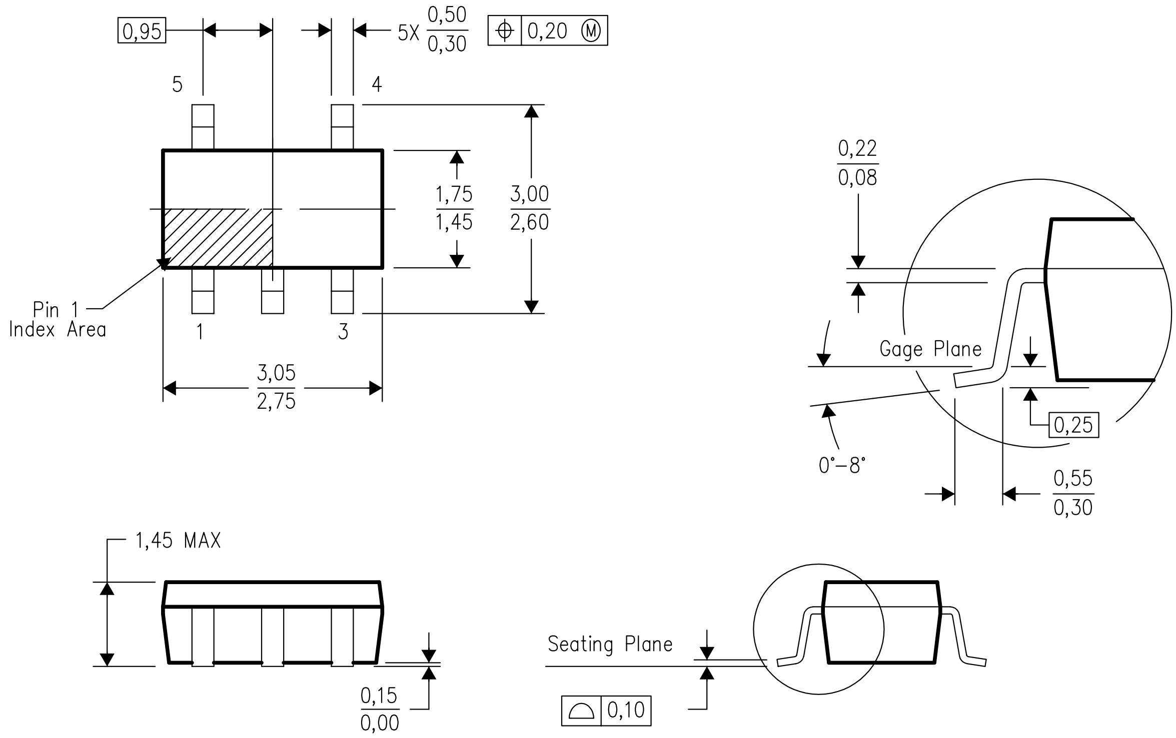
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79328QDBVRQ1	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS79330QDBVRQ1	SOT-23	DBV	5	3000	203.0	203.0	35.0

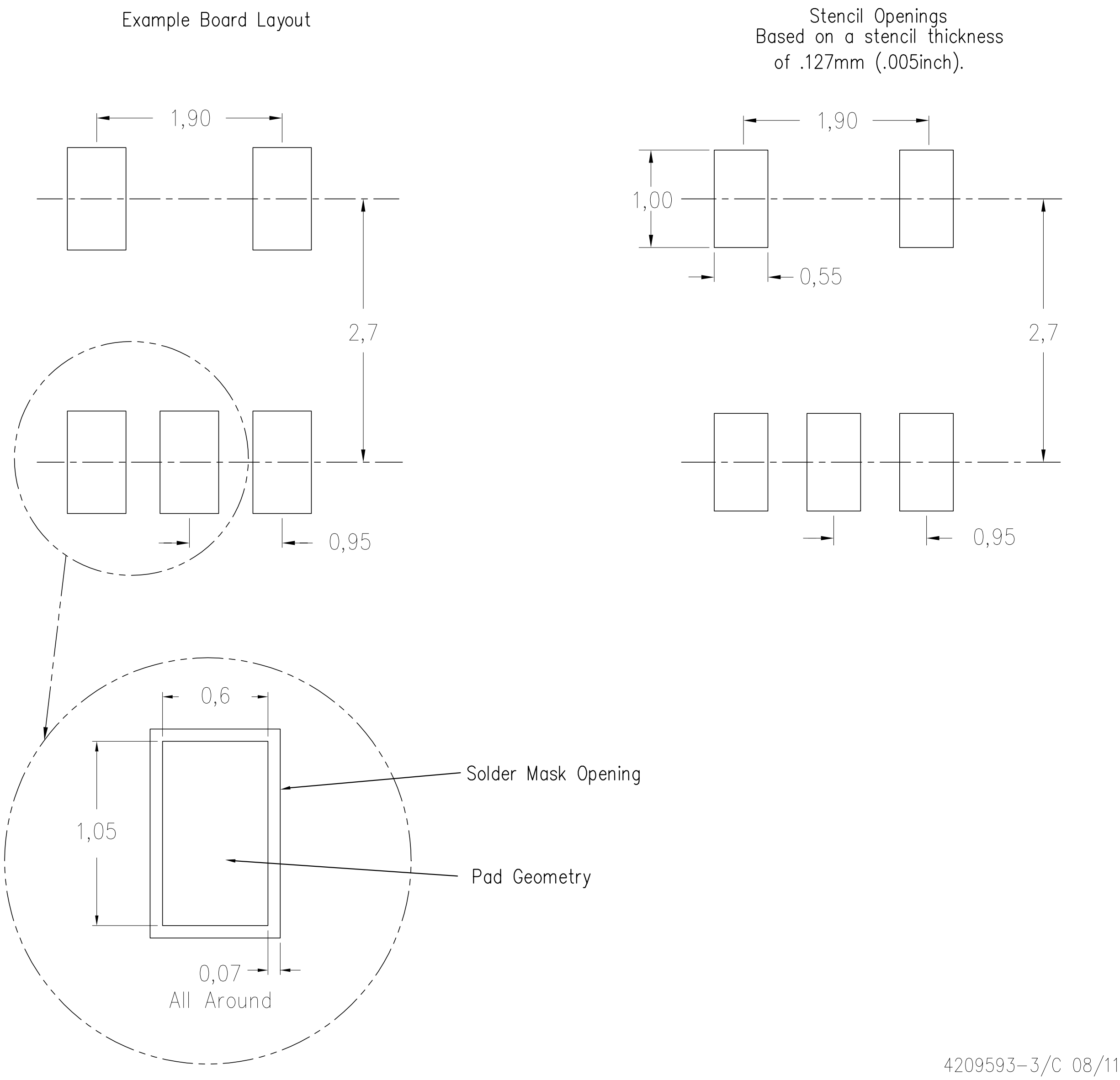
DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5) PLASTIC SMALL OUTLINE

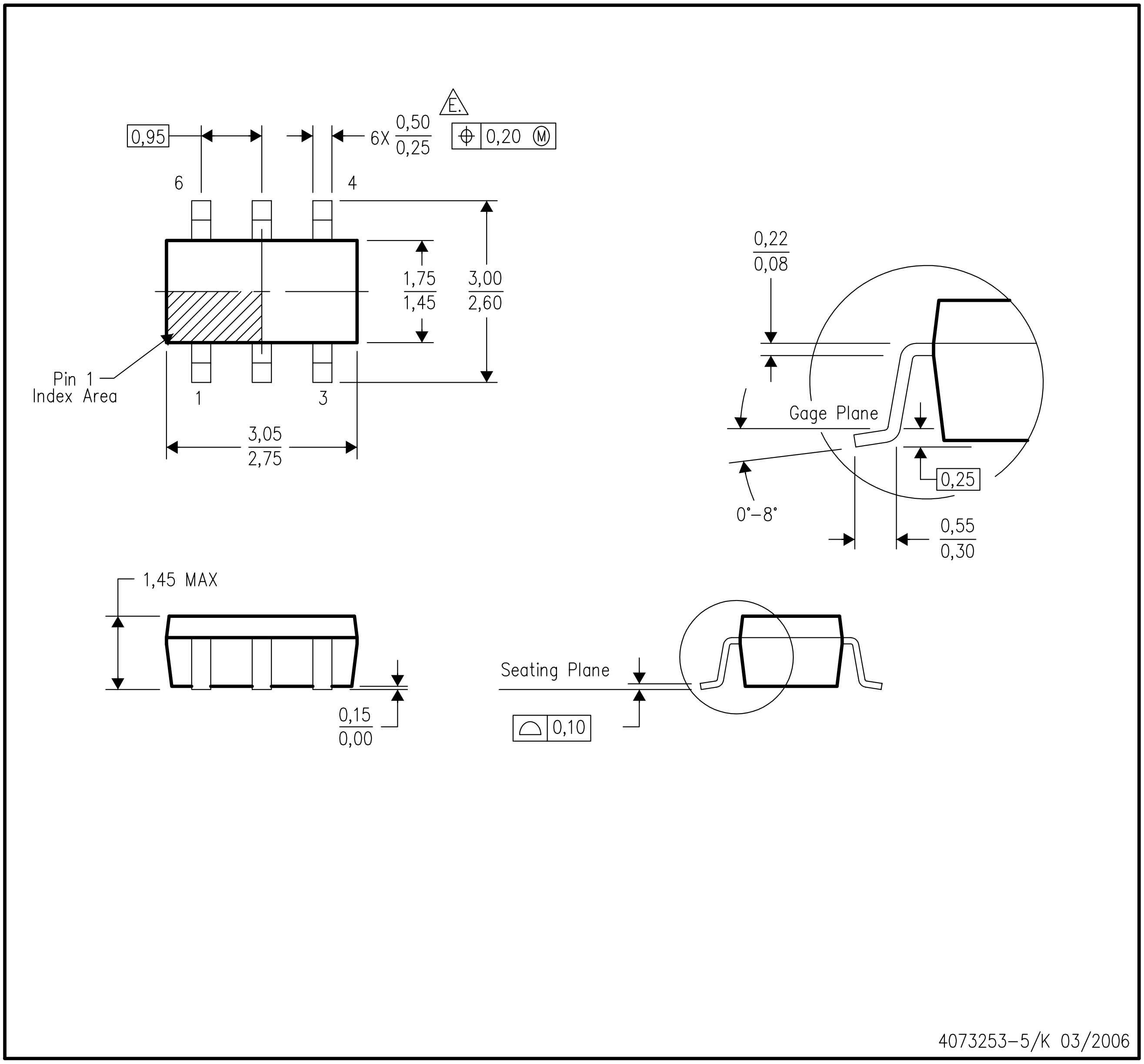


4209593-3/C 08/11

NOTES:

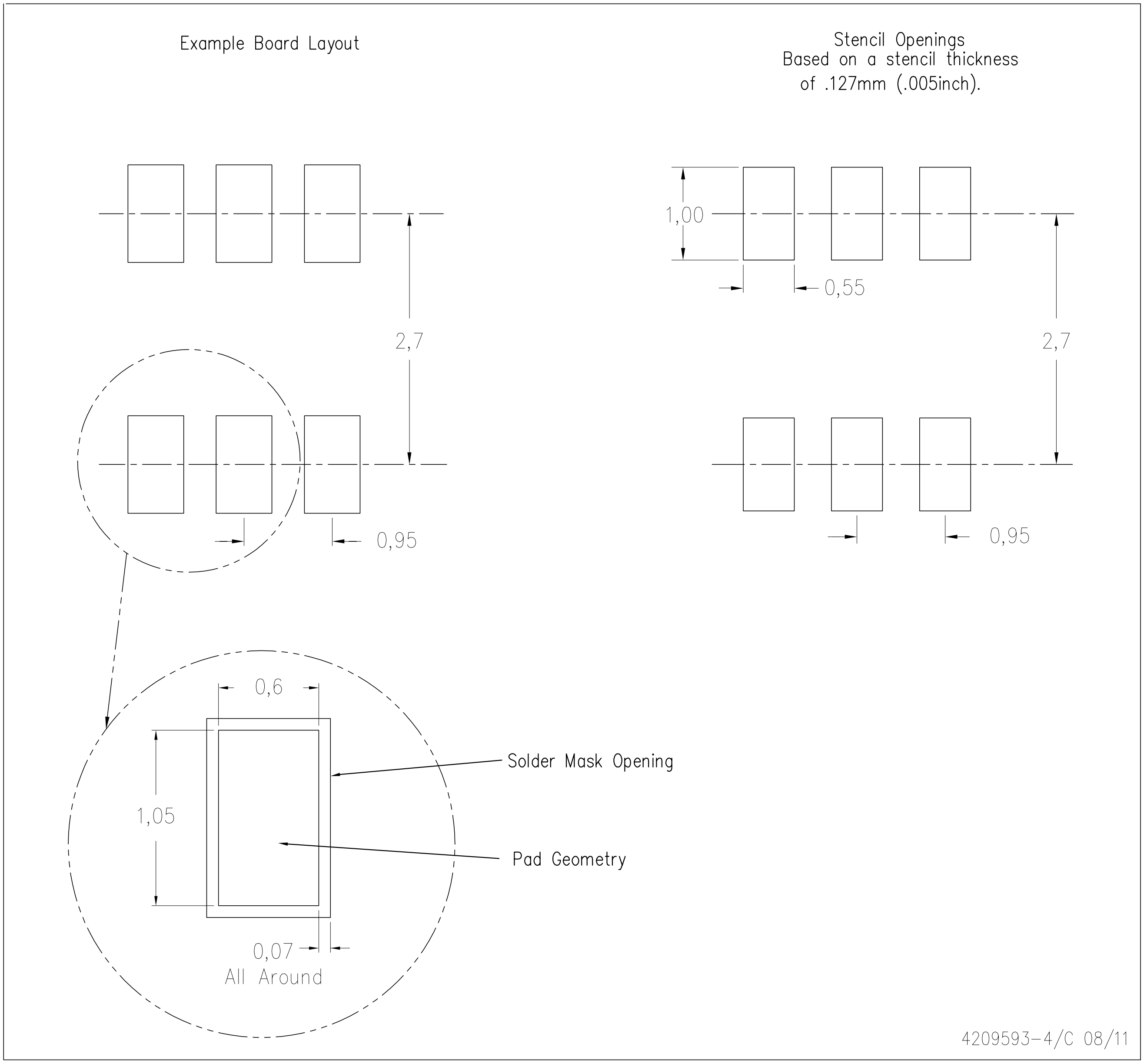
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265