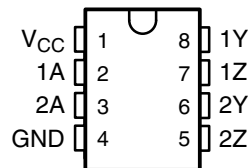


# uA9638C DUAL HIGH-SPEED DIFFERENTIAL LINE DRIVER

SLLS112C – OCTOBER 1980 – REVISED APRIL 1994

- **Meets or Exceeds ANSI Standard EIA/TIA-422-B**
- **Operates From a Single 5-V Power Supply**
- **Drives Loads as Low as 50  $\Omega$  up to 15 Mbps**
- **TTL- and CMOS-Input Compatibility**
- **Output Short-Circuit Protection**
- **Interchangeable With National Semiconductor™ DS9638**

**D OR P PACKAGE  
(TOP VIEW)**



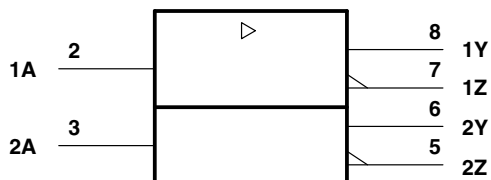
## description

The uA9638C is a dual high-speed differential line driver designed to meet ANSI Standard EIA/TIA-422-B. The inputs are TTL and CMOS compatible and have input clamp diodes. Schottky-diode-clamped transistors are used to minimize propagation delay time. This device operates from a single 5-V power supply and is supplied in an 8-pin package.

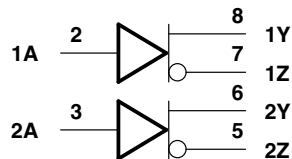
The uA9638 provides the current needed to drive low-impedance loads at high speeds. Typically used with twisted-pair cabling and differential receiver(s), base-band data transmission can be accomplished up to and exceeding 15 Mbps in properly designed systems. The uA9637A dual line receiver is commonly used as the receiver. For even faster switching speeds in the same pin configuration, see the SN75ALS191.

The uA9638C is characterized for operation from 0°C to 70°C.

## logic symbol†



## logic diagram



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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**TEXAS  
INSTRUMENTS**

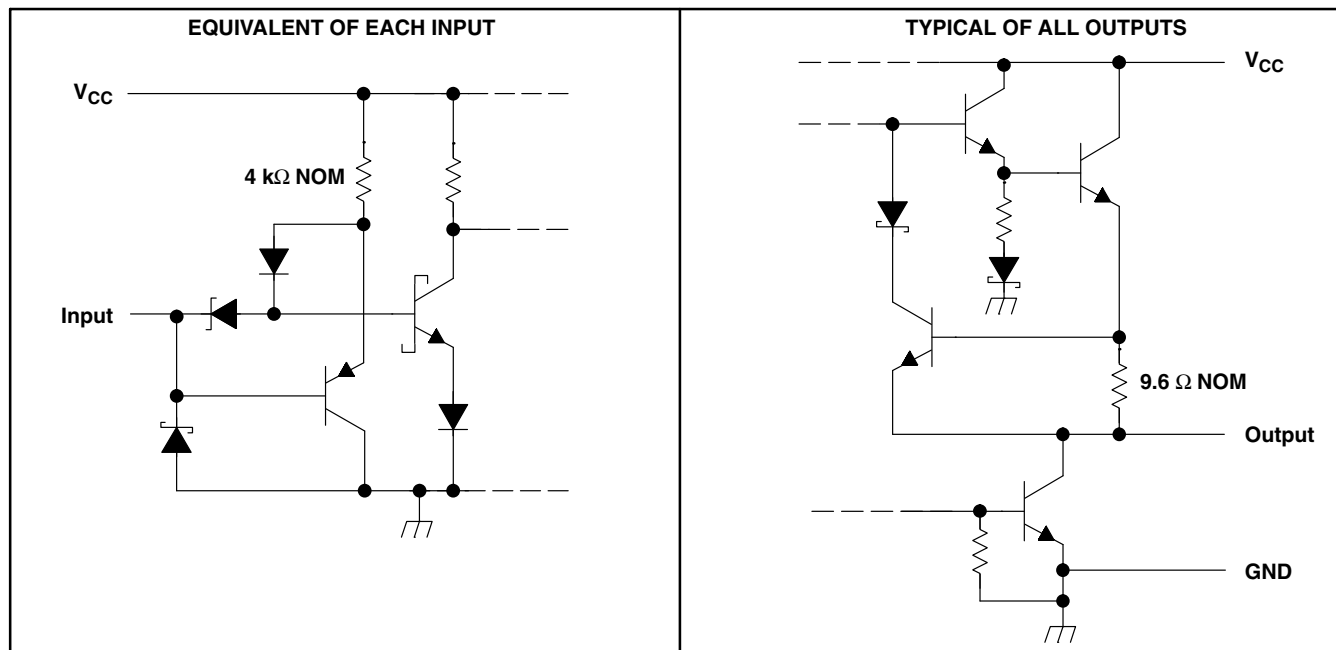
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# uA9638C DUAL HIGH-SPEED DIFFERENTIAL LINE DRIVER

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## schematics of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|  |       |                              |
|--|-------|------------------------------|
| Supply voltage range, V <sub>CC</sub> (see Note 1)   | ..... | -0.5 V to 7 V                |
| Input voltage range, V <sub>I</sub>                  | ..... | -0.5 V to 7 V                |
| Continuous total power dissipation                   | ..... | See Dissipation Rating Table |
| Operating free-air temperature range, T <sub>A</sub> | ..... | 0°C to 70°C                  |
| Storage temperature range, T <sub>stg</sub>          | ..... | -65°C to 150°C               |
| Lead temperature 1,6 mm (1/16 inch) from 10 seconds  | ..... | 260°C                        |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values except differential output voltages are with respect to network GND.

DISSIPATION RATING TABLE

| PACKAGE | T <sub>A</sub> = 25°C<br>POWER RATING | DERATING FACTOR<br>ABOVE T <sub>A</sub> = 25°C | T <sub>A</sub> = 70°C<br>POWER RATING |
|---------|---------------------------------------|--|---------------------------------------|
| D       | 725 mW                                | 5.8 mW/°C                                      | 464 mW                                |
| P       | 1000 mW                               | 8.0 mW/°C                                      | 640 mW                                |

## recommended operating conditions

|  | MIN  | NOM | MAX  | UNIT |
|--|------|-----|------|------|
| Supply voltage, V <sub>CC</sub>                | 4.75 | 5   | 5.25 | V    |
| High-level input voltage, V <sub>IH</sub>      | 2    |     |      | V    |
| Low-level input voltage, V <sub>IL</sub>       |      |     | 0.8  | V    |
| High-level output current, I <sub>OH</sub>     |      |     | -50  | mA   |
| Low-level output current, I <sub>OL</sub>      |      |     | 50   | mA   |
| Operating free-air temperature, T <sub>A</sub> | 0    |     | 70   | °C   |



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# uA9638C DUAL HIGH-SPEED DIFFERENTIAL LINE DRIVER

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## electrical characteristics over operating free-air temperature range (unless otherwise noted)

| PARAMETER        |   | TEST CONDITIONS   |                                      |                           | MIN                   | TYP† | MAX        | UNIT          |   |
|------------------|---|---|--------------------------------------|---------------------------|-----------------------|------|------------|---------------|---|
| $V_{IK}$         | Input clamp voltage                                 | $V_{CC} = 4.75\text{ V}$ , $I_I = -18\text{ mA}$            |                                      |                           | -1                    | -1.2 |            | V             |   |
| $V_{OH}$         | High-level output voltage                           | $V_{CC} = 4.75\text{ V}$ ,<br>$V_{IL} = 0.8\text{ V}$       | $V_{IH} = 2\text{ V}$ ,              | $I_{OH} = -10\text{ mA}$  | 2.5                   | 3.5  |            | V             |   |
|                  |   |   |                                      | $I_{OH} = -40\text{ mA}$  | 2                     |      |            |               |   |
| $V_{OL}$         | Low-level output voltage                            | $V_{CC} = 4.75\text{ V}$ ,<br>$I_{OL} = 40\text{ mA}$       | $V_{IH} = 2\text{ V}$ ,              | $V_{IL} = 0.8\text{ V}$ , |                       |      | 0.5        | V             |   |
| $ V_{OD1} $      | Magnitude of differential output voltage            | $V_{CC} = 5.25\text{ V}$ , $I_O = 0$                        |                                      |                           |                       |      | $2V_{OD2}$ | V             |   |
| $ V_{OD2} $      | Magnitude of differential output voltage            |   |                                      |                           | 2                     |      |            | V             |   |
| $\Delta V_{OD} $ | Change in magnitude of differential output voltage‡ | $V_{CC} = 4.75\text{ V to }5.25\text{ V}$ ,<br>See Figure 1 |                                      |                           | $R_L = 100\ \Omega$ , |      |            | $\pm 0.4$     | V |
| $V_{OC}$         | Common-mode output voltage§                         |   |                                      |                           |                       |      |            | 3             | V |
| $\Delta V_{OC} $ | Change in magnitude of common-mode output voltage‡  |   |                                      |                           |                       |      |            | $\pm 0.4$     | V |
| $I_O$            | Output current with power off                       | $V_{CC} = 0$  | $V_O = 6\text{ V}$                   |                           | 0.1                   | 100  |            | $\mu\text{A}$ |   |
|                  |   |   | $V_O = -0.25\text{ V}$               |                           | -0.1                  | -100 |            |               |   |
|                  |   |   | $V_O = -0.25\text{ V to }6\text{ V}$ |                           | $\pm 100$             |      |            |               |   |
| $I_I$            | Input current                                       | $V_{CC} = 5.25\text{ V}$ , $V_I = 5.5\text{ V}$             |                                      |                           |                       |      | 50         | $\mu\text{A}$ |   |
| $I_{IH}$         | High-level input current                            | $V_{CC} = 5.25\text{ V}$ , $V_I = 2.7\text{ V}$             |                                      |                           |                       |      | 25         | $\mu\text{A}$ |   |
| $I_{IL}$         | Low-level input current                             | $V_{CC} = 5.25\text{ V}$ , $V_I = 0.5\text{ V}$             |                                      |                           |                       |      | -200       | $\mu\text{A}$ |   |
| $I_{OS}$         | Short-circuit output current¶                       | $V_{CC} = 5.25\text{ V}$ , $V_O = 0$                        |                                      |                           | -50                   |      | -150       | mA            |   |
| $I_{CC}$         | Supply current (both drivers)                       | $V_{CC} = 5.25\text{ V}$ , No load, All inputs at 0 V       |                                      |                           | 45                    |      | 65         | mA            |   |

† All typical values are at  $V_{CC} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

‡  $\Delta|V_{OD}|$  and  $\Delta|V_{OC}|$  are the changes in magnitude of  $V_{OD}$  and  $V_{OC}$ , respectively, that occur when the input is changed from a high level to a low level or vice versa.

§ In Standard EIA-422-A,  $V_{OC}$ , which is the average of the two output voltages with respect to ground, is called output offset voltage,  $V_{OS}$ .

¶ Only one output at a time should be shorted, and duration of the short circuit should not exceed one second.

## switching characteristics, $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$

| PARAMETER   |                                     | TEST CONDITIONS        |                       |              | MIN | TYP | MAX | UNIT |
|-------------|-------------------------------------|------------------------|-----------------------|--------------|-----|-----|-----|------|
| $t_{d(OD)}$ | Differential output delay time      | $C_L = 15\text{ pF}$ , | $R_L = 100\ \Omega$ , | See Figure 2 |     | 10  | 20  | ns   |
| $t_{t(OD)}$ | Differential output transition time |                        |                       |              |     | 10  | 20  | ns   |
| $t_{sk(o)}$ | Output skew                         | See Figure 2           |                       |              |     | 1   |     | ns   |



# uA9638C DUAL HIGH-SPEED DIFFERENTIAL LINE DRIVER

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## PARAMETER MEASUREMENT INFORMATION

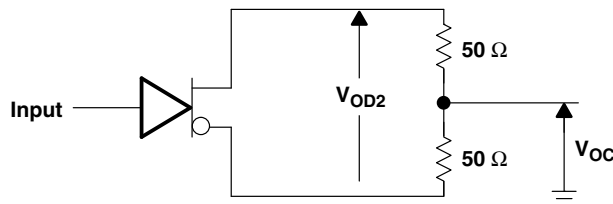
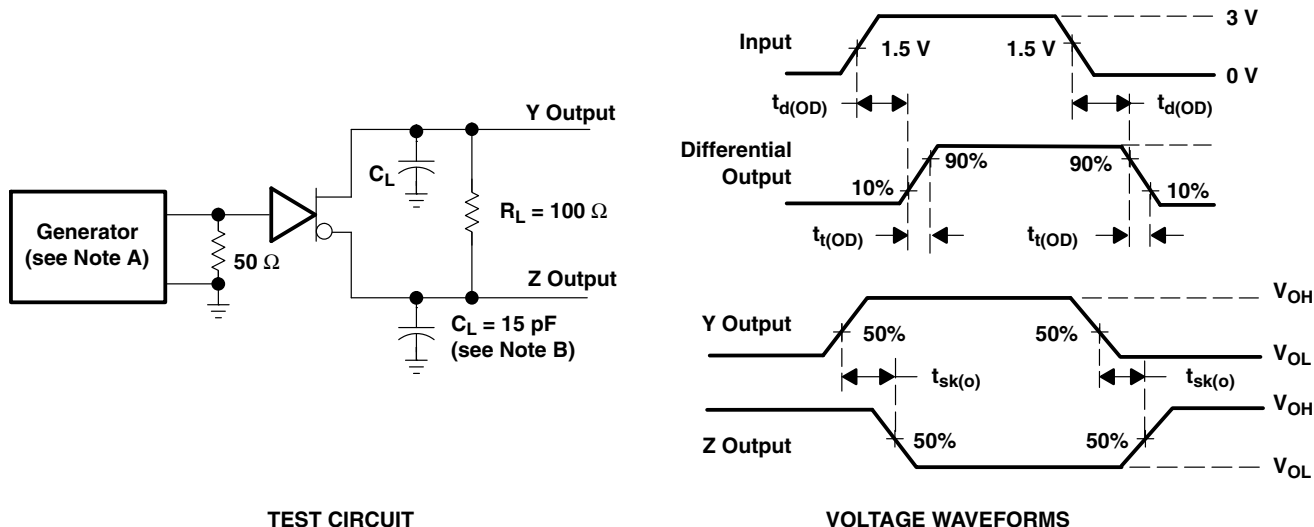


Figure 1. Differential and Common-Mode Output Voltages



### TEST CIRCUIT

### VOLTAGE WAVEFORMS

NOTES: A. The input pulse generator has the following characteristics:  $Z_O = 50 \Omega$ ,  $PRR \leq 500 \text{ kHz}$ ,  $t_w = 100 \text{ ns}$ ,  $t_r = \leq 5 \text{ ns}$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| UA9638CD         | ACTIVE        | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | 0 to 70      | 9638C                   | <a href="#">Samples</a> |
| UA9638CDE4       | ACTIVE        | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | 0 to 70      | 9638C                   | <a href="#">Samples</a> |
| UA9638CDG4       | ACTIVE        | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | 0 to 70      | 9638C                   | <a href="#">Samples</a> |
| UA9638CDR        | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | 0 to 70      | 9638C                   | <a href="#">Samples</a> |
| UA9638CDRG4      | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | 0 to 70      | 9638C                   | <a href="#">Samples</a> |
| UA9638CP         | ACTIVE        | PDIP         | P               | 8    | 50          | Pb-Free (RoHS)          | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | UA9638CP                | <a href="#">Samples</a> |
| UA9638CPE4       | ACTIVE        | PDIP         | P               | 8    | 50          | Pb-Free (RoHS)          | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | UA9638CP                | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

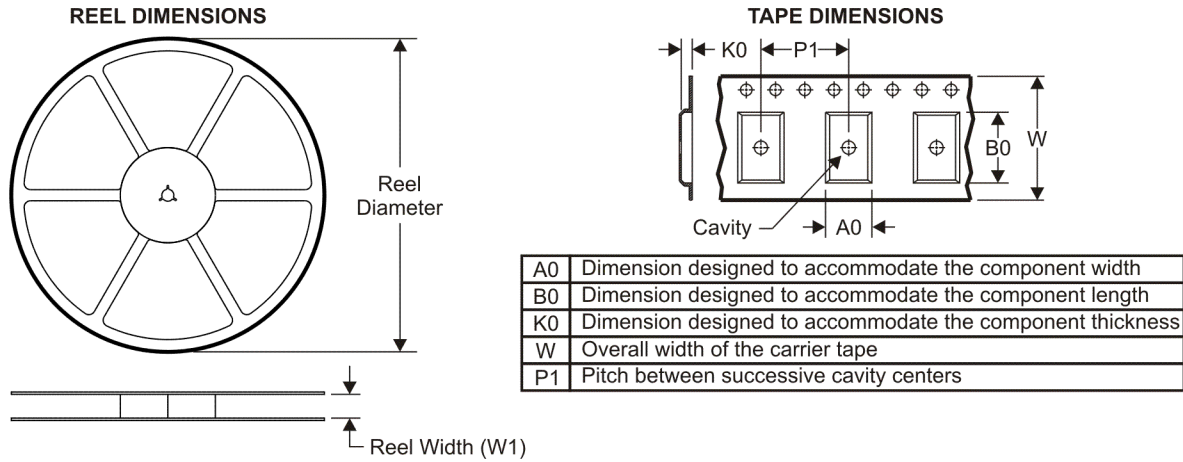
<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

| Device    | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| UA9638CDR | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

| Device    | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| UA9638CDR | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |



P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

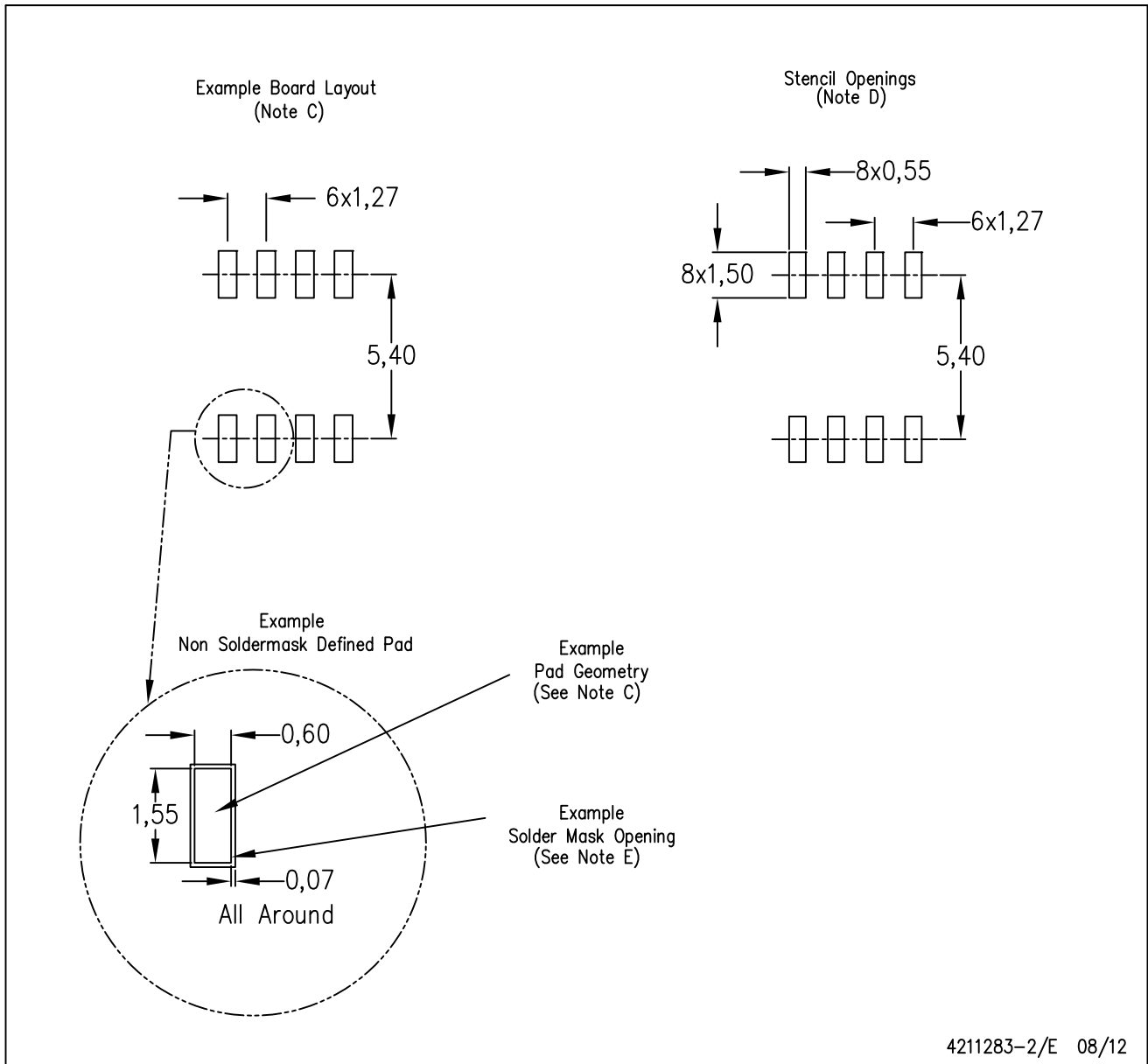
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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