# High Gain Adjust Range, Wideband, VARIABLE GAIN AMPLIFIER

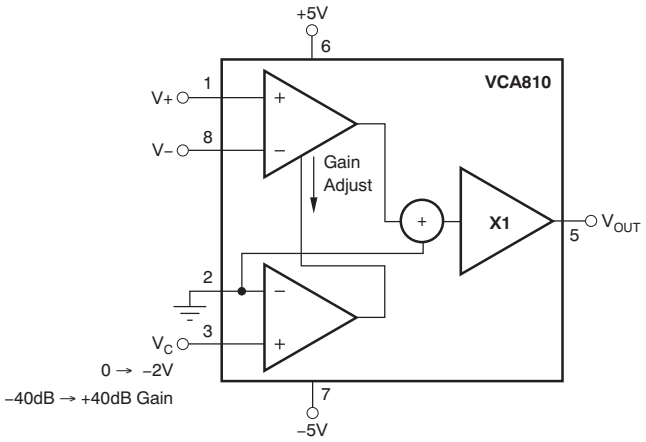
**Check for Samples: VCA810**

## FEATURES

- **HIGH GAIN ADJUST RANGE: ±40dB**
- **DIFFERENTIAL IN/SINGLE-ENDED OUT**
- **LOW INPUT NOISE VOLTAGE: 2.4nV/√Hz**
- **CONSTANT BANDWIDTH vs GAIN: 35MHz**
- **HIGH dB/V GAIN LINEARITY: ±0.3dB**
- **GAIN CONTROL BANDWIDTH: 25MHz**
- **LOW OUTPUT DC ERROR: < ±40mV**
- **HIGH OUTPUT CURRENT: ±60mA**
- **LOW SUPPLY CURRENT: 24.8mA (max for −40°C to +85°C temperature range)**

## APPLICATIONS

- **OPTICAL RECEIVER TIME GAIN CONTROL**
- **SONAR SYSTEMS**
- **VOLTAGE-TUNABLE ACTIVE FILTERS**
- **LOG AMPLIFIERS**
- **PULSE AMPLITUDE COMPENSATION**
- **AGC RECEIVERS WITH RSSI**
- **IMPROVED REPLACEMENT FOR VCA610**




## DESCRIPTION

The VCA810 is a dc-coupled, wideband, continuously variable, voltage-controlled gain amplifier. It provides a differential input to single-ended output conversion with a high-impedance gain control input used to vary the gain over a –40dB to +40dB range linear in dB/V.

Operating from ±5V supplies, the gain control voltage for the VCA810 will adjust the gain from –40dB at 0V input to +40dB at –2V input. Increasing the control voltage above ground will attenuate the signal path to greater than 80dB. Signal bandwidth and slew rate remain constant over the entire gain adjust range. This 40dB/V gain control is accurate within ±1.5dB (±0.9dB for high grade), allowing the gain control voltage in an AGC application to be used as a Received Signal Strength Indicator (RSSI) with ±1.5dB accuracy.

Excellent common-mode rejection and common-mode input range at the two high-impedance inputs allow the VCA810 to provide a differential receiver operation with gain adjust. The output signal is referenced to ground. Zero differential input voltage gives a 0V output with a small dc offset error. Low input noise voltage ensures good output SNR at the highest gain settings.

In applications where pulse edge information is critical, and the VCA810 is being used to equalize varying channel loss, minimal change in group delay over gain setting will retain excellent pulse edge information.

An improved output stage provides adequate output current to drive the most demanding loads. While principally intended to drive analog-to-digital converters (ADCs) or second-stage amplifiers, the ±60mA output current will easily drive doubly-terminated 50Ω lines or a passive post-filter stage over the ±1.7V output voltage range.

### VCA810 RELATED PRODUCTS

| SINGLES | DUALS | GAIN ADJUST RANGE (dB) | INPUT NOISE (nV/√Hz) | SIGNAL BANDWIDTH (MHz) |
|---|---|---|---|---|
| VCA811 | — | 80 | 2.4 | 80 |
| — | VCA2612 | 45 | 1.25 | 80 |
| — | VCA2613 | 45 | 1 | 80 |
| — | VCA2614 | 45 | 3.6 | 40 |
| — | VCA2616 | 45 | 3.3 | 40 |
| | VCA2618 | 45 | 5.5 | 30 |

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION(1)

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|---|---|---|---|---|---|---|
| VCA810ID | SO-8 | D | –40°C to +85°C | VCA810 | VCA810ID | Rails, 75 |
| | | | | | VCA810IDR | Tape and Reel, 2500 |
| VCA810AID | SO-8 | D | –40°C to +85°C | VCA810A(2) | VCA810AID | Rails, 75 |
| | | | | | VCA810AIDR | Tape and Reel, 2500 |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.
(2) The ***A*** indicating high grade appears opposite the pin 1 marking indicator.

## ABSOLUTE MAXIMUM RATINGS(1)

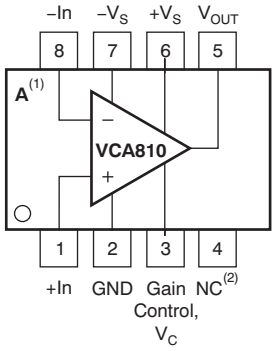
Over operating free-air temperature range, unless otherwise noted.

| | | VCA810 | UNIT |
|---|---|---|---|
| Power supply | | ±6.5 | V |
| Internal power dissipation | | See Thermal Analysis section | |
| Differential input voltage | | $\pm V_S$ | V |
| Input common-mode voltage range | | $\pm V_S$ | V |
| Storage temperature range, D package | | –65 to +125 | °C |
| Junction temperature ($T_J$) | | +150 | °C |
| ESD ratings | Human body model (HBM) | 2000 | V |
| | Charge device model (CDM) | 1500 | V |
| | Machine model | 200 | V |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

## PIN CONFIGURATIONS

**D PACKAGE**
**SO-8**
**(TOP VIEW)**




(1) High grade version indicator.
(2) NC = Not connected.

## ELECTRICAL CHARACTERISTICS: $V_S$ = ±5V

**Boldface** limits are tested at +25°C.
At $R_L$ = 500Ω, and $V_{IN}$ = single-ended input on V+ with V− at ground,, unless otherwise noted.

| PARAMETER | CONDITIONS | VCA810 | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | TYP | MIN/MAX OVER TEMPERATURE | | | | | |
| | | +25°C | +25°C(2) | 0°C to +70°C(3) | –40°C to +85°C(3) | UNITS | MIN/ MAX | TEST LEVEL(1) |
| **AC PERFORMANCE** | | | | | | | | |
| Small-signal bandwidth (see Figure 29) | −2V ≤ $V_C$ ≤ 0V | 35 | 30 | 29 | 29 | MHz | min | B |
| Large-signal bandwidth | $V_O$ = 2$V_{PP}$, −2 ≤ $V_C$ ≤ −1 | 35 | 30 | 29 | 29 | MHz | min | B |
| Frequency response peaking | $V_O$ < 500m$V_{PP}$, −2V ≤ $V_C$ ≤ 0V | 0.1 | 0.5 | 0.5 | 0.5 | dB | min | B |
| Slew rate | $V_O$ = 3.5V Step, −2 ≤ $V_C$ ≤ −1, 10% to 90% | 350 | 300 | 300 | 295 | V/µs | min | B |
| Settling time to 0.01% | $V_O$ = 1V Step, −2 ≤ $V_C$ ≤ −1 | 30 | 40 | 41 | 41 | ns | min | B |
| Rise-and-fall time | $V_O$ = 1V Step, −2 ≤ $V_C$ ≤ −1 | 10 | 12 | 12.1 | 12.1 | ns | min | B |
| Group delay | G = 0dB, $V_C$=−1V, f = 5MHz, $V_O$ = 500m$V_{PP}$ | 6.2 | | | | ns | typ | C |
| Group delay variation | $V_O$ < 500m$V_{PP}$, −2V ≤ $V_C$ ≤ 0V, f = 5MHz | 3.5 | | | | ns | typ | C |
| Harmonic distortion | | | | | | | | |
| Second harmonic | $V_O$ = 1$V_{PP}$, f = 1MHz, $V_C$ = −1V, G = 0dB | –71 | –51 | –50 | –49 | dBc | min | B |
| Third harmonic | $V_O$ = 1$V_{PP}$, f = 1MHz, $V_C$ = −1V, G = 0dB | −35 | –34 | –32 | –29 | dBc | min | B |
| Input voltage noise | $V_C$ = −2V | 2.4 | 2.8 | 3.4 | 3.5 | nV/√Hz | max | B |
| Input current noise | −2V ≤ $V_C$ ≤ 0V | 1.4 | 1.8 | 2.0 | 2.1 | pA/√Hz | max | B |
| Fully attenuated feedthrough | f ≤ 1MHz, $V_C$ > +200mV | −80 | −70 | | | dB | max | B |
| Overdrive recovery | $V_{IN}$ = 2V to 0V, $V_C$ = −2V, G = 40dB | 100 | 150 | | | ns | min | B |
| **DC PERFORMANCE** | Single-ended or differential input | | | | | | | |
| Output offset voltage (both inputs grounded)(4) | −2V ≤ $V_C$ ≤ 0V | ±4 | **±22** | ±30 | ±32 | mV | max | A |
| Output offset voltage drift | | | | ±125 | ±125 | V/°C | max | B |
| Input offset voltage(4) | Both inputs grounded | ±0.1 | **±0.25** | ±0.30 | ±0.35 | mV | max | A |
| input offset voltage drift | | | | ±1 | ±1.2 | µV/°C | max | B |
| Input bias current | −2V ≤ $V_C$ ≤ 0V | −6 | **–10** | −12 | −14 | µA | max | A |
| Input bias current drift | | | | ±25 | ±30 | nA/°C | max | B |
| Input offset current | −2V ≤ $V_C$ ≤ 0V | ±100 | **±600** | ±700 | ±800 | nA | max | A |
| Input offset current drift | | | | ±1.4 | ±2.2 | nA/°C | max | B |
| **INPUT** | | | | | | | | |
| Common-mode input range | | ±2.4 | **±2.3** | ±2.3 | ±2.2 | V | min | A |
| Common-mode rejection ratio | $V_{CM}$ = 0.5V, $V_C$ = −2V, Input-referred | 95 | **85** | 83 | 80 | dB | min | A |
| Input impedance | $V_{CM}$ = 0V, Single-ended | 1\|\| 1 | | | | MΩ \|\| pF | typ | C |
| | $V_{CM}$ = 0V, Differential | > 10 \|\| < 2 | | | | MΩ \|\| pF | typ | C |
| Differential input range(5) | $V_C$ = 0V, $V_{CM}$ = 0V | 3 | | | | $V_{PP}$ | typ | C |
| **OUTPUT** | | | | | | | | |
| Voltage output swing | $V_C$ = −2V, $R_L$ = 100Ω | ±1.8 | **±1.7** | ±1.4 | ±1.3 | V | min | A |
| | $V_C$ = −2V, $R_L$ = 100Ω | ±1.7 | **±1.6** | ±1.3 | ±1.2 | V | min | A |
| Output current | $V_O$ = 0V | ±60 | **±40** | ±35 | ±32 | mA | min | A |
| Output short-circuit current | $V_O$ = 0V | ±120 | | | | mA | typ | C |
| Output impedance | $V_O$ = 0V, f < 100kHz | 0.2 | | | | Ω | typ | C |

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value; only for information.
(2) Junction temperature = ambient for +25°C tested specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +30°C at high temperature limit for over temperature specifications.
(4) Total output offset is: (Output Offset Voltage ± Input Offset Voltage x Gain).
(5) Maximum input at minimum gain for < 1dB gain compression.

## ELECTRICAL CHARACTERISTICS: $V_S$ = ±5V (continued)

**Boldface** limits are tested at +25°C.

At $R_L$ = 500Ω, and $V_{IN}$ = single-ended input on V+ with V− at ground,, unless otherwise noted.

| | | VCA810 | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | TYP | MIN/MAX OVER TEMPERATURE | | | | | |
| PARAMETER | CONDITIONS | +25°C | +25°C[2] | 0°C to +70°C[3] | –40°C to +85°C[3] | UNITS | MIN/ MAX | TEST LEVEL[1] |
| **GAIN CONTROL ($V_C$, Pin 3)** | Single-ended or differential input | | | | | | | |
| Specified gain range | $\Delta V_C/\Delta dB$ = 25mV/dB | ±40 | | | | dB | typ | C |
| Maximum control voltage | G = −40dB | 0 | | | | V | typ | C |
| Minimum control voltage | G = +40dB | –2 | | | | V | typ | C |
| Gain accuracy | $-1.8V \le V_C \le -0.2V$ | ±0.4 | **±1.5** | ±2.5 | ±3.5 | dB | max | A |
| | $V_C < -1.8V$, $V_C > -0.2V$ | ±0.5 | **±2.2** | ±3.7 | ±4.7 | dB | max | A |
| Gain drift | $-1.8V \le V_C \le -0.2V$ | | | ±0.02 | ±0.03 | dB/°C | max | B |
| | $V_C < -1.8V$, $V_C > -0.2V$ | | | ±0.03 | ±0.04 | dB/°C | max | B |
| Gain control slope | | –40 | | | | db/V | typ | C |
| Gain control linearity[6] | $-1.8V \le V_C \le 0V$ | ±0.3 | ±1 | ±1.1 | ±1.2 | dB | max | A |
| | $V_C < -1.8V$ | ±0.7 | **±1.6** | ±2.5 | ±3.2 | dB | max | A |
| Gain control bandwidth | | 25 | 20 | 19 | 19 | MHz | min | B |
| Gain control slew rate | 80dB Gain Step | 900 | | | | dB/ns | typ | C |
| Gain settling time | 1%, 80dB Step | 0.8 | | | | µs | typ | C |
| Input bias current | $V_C$ = −1V | –1.5 | **–3.5** | –4.5 | –8 | µA | max | A |
| Gain + Power-supply rejection ratio | $V_C$ = −2V, G = +40dB, $+V_S$ = 5V ±0.5V | 0.5 | **1.5** | 1.8 | 2 | dB/V | max | A |
| Gain – Power-supply rejection ratio | $V_C$ = −2V, G = +40dB, $–V_S$ = –5V ±0.5V | 0.7 | **1.5** | 1.8 | 2 | dB/V | max | A |
| **POWER SUPPLY** | | | | | | | | |
| Specified operating voltage | | ±5 | | | | V | typ | C |
| Minimum operating voltage | | | **±4** | ±4 | ±4 | V | min | A |
| Maximum operating voltage | | | **±6** | ±6 | ±6 | V | max | A |
| Positive supply quiescent current | | | | | | | | |
| Maximum quiescent current | $+V_S$ = +5V, G = −40dB | 10 | **12.5** | 12.6 | 12.7 | mA | min | A |
| Minimum quiescent current | $+V_S$ = +5V, G = −40dB | 10 | **7.5** | 7.2 | 7.1 | mA | max | A |
| Maximum quiescent current | $+V_S$ = +5V, G = +40dB | 18 | **20.5** | 22 | 22.3 | mA | min | A |
| Minimum quiescent current | $+V_S$ = +5V, G = +40dB | 18 | **15.5** | 14.5 | 13.5 | mA | max | A |
| Negative supply quiescent current[7] | | | | | | | | |
| Maximum quiescent current | $-V_S$ = −5V, G = −40dB | 12 | **14.5** | 14.6 | 14.7 | mA | max | A |
| Minimum quiescent current | $-V_S$ = −5V, G = −40dB | 12 | **9.5** | 9.4 | 9.3 | mA | min | A |
| Maximum quiescent current | $-V_S$ = −5V, G = +40dB | 20 | **22.5** | 24.5 | 24.8 | mA | max | A |
| Minimum quiescent current | $-V_S$ = −5V, G = +40dB | 20 | **17.5** | 16.5 | 16 | mA | min | A |
| Positive power-supply rejection ratio (+PSRR) | Input-referred, $V_C$ = −2V | 90 | **75** | 75 | 73 | dB | min | A |
| Negative power-supply rejection ratio (–PSRR) | Input-referred, $V_C$ = −2V | 85 | **70** | 70 | 68 | dB | min | A |
| **THERMAL CHARACTERISTICS** | | | | | | | | |
| Specified operating range, ID package | | –40 to +85 | | | | °C | typ | C |
| Thermal resistance, $\theta_{JA}$ | Junction-to-ambient | | | | | | | |
| D SO-8 | | 80 | | | | °C/W | typ | C |

(6) Maximum deviation from best line fit.

(7) Magnitude.

## HIGH GRADE DC SPECIFICATIONS: $V_S$ = ±5V (VCA810AID)

**Boldface** limits are tested at +25°C.

At $R_L$ = 500Ω, and $V_{IN}$ = single-ended input on V+ with V− at ground,, unless otherwise noted.

| | | VCA810AID | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | TYP | MIN/MAX OVER TEMPERATURE | | | | | |
| PARAMETER | CONDITIONS | +25°C | +25°C[2] | 0°C to +70°C[3] | –40°C to +85°C[3] | UNITS | MIN/ MAX | TEST LEVEL[1] |
| **DC PERFORMANCE** | Single-ended or differential input | | | | | | | |
| Output offset voltage | −2V < $V_C$ < 0V | ±4 | **±14** | ±24 | ±26 | mV | max | A |
| Input offset voltage | | ±0.1 | **±0.2** | ±0.25 | ±0.3 | mV | max | A |
| Input offset current | | ±100 | **±500** | ±600 | ±700 | mA | max | A |
| **GAIN CONTROL ($V_C$, Pin 3)** | Single-ended or differential input | | | | | | | |
| Gain accuracy | −1.8V ≤ $V_C$ ≤ −0.2V | ±0.4 | **±0.9** | ±1.9 | ±2.9 | dB | max | A |
| | $V_C$ < −1.8V, $V_C$ > −0.2V | ±0.5 | **±1.5** | ±3.0 | ±4.0 | dB | max | A |
| Gain control linearity[4] | −1.8V ≤ $V_C$ ≤ 0V | ±0.3 | **±0.6** | ±0.7 | ±0.8 | dB | max | A |
| | $V_C$ < −1.8V | ±0.7 | **±1.1** | ±1.9 | ±2.7 | dB/V | max | A |
| **POWER SUPPLY** | | | | | | | | |
| Positive supply quiescent current | | | | | | | | |
| Maximum quiescent current | +$V_S$ = +5V, G = −40dB | 10 | **11.5** | 11.6 | 11.7 | mA | min | A |
| Minimum quiescent current | +$V_S$ = +5V, G = −40dB | 10 | **8.5** | 8.2 | 8.1 | mA | max | A |
| Maximum quiescent current | +$V_S$ = +5V, G = +40dB | 18 | **19.5** | 21 | 21.3 | mA | min | A |
| Minimum quiescent current | +$V_S$ = +5V, G = +40dB | 18 | **16.5** | 15.5 | 14.5 | mA | max | A |
| Negative supply quiescent current[5] | | | | | | | | |
| Maximum quiescent current | −$V_S$ = −5V, G = −40dB | 12 | **14** | 14.1 | 14.2 | mA | min | A |
| Minimum quiescent current | −$V_S$ = −5V, G = −40dB | 12 | **10** | 9.9 | 9.8 | mA | max | A |
| Maximum quiescent current | −$V_S$ = −5V, G = +40dB | 20 | **22** | 24 | 24.3 | mA | min | A |
| Minimum quiescent current | −$V_S$ = −5V, G = +40dB | 20 | **18** | 17 | 16.5 | mA | max | A |

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value; only for information.
(2) Junction temperature = ambient for +25°C tested specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +30°C at high temperature limit for over temperature specifications.
(4) Maximum deviation from best line fit.
(5) Magnitude.

## TYPICAL CHARACTERISTICS: $V_S$ = ±5V

At $R_L$ = 500Ω and $V_{IN}$ = single-ended input on V+ with V− at ground, unless otherwise noted.

### SMALL−SIGNAL FREQUENCY RESPONSE

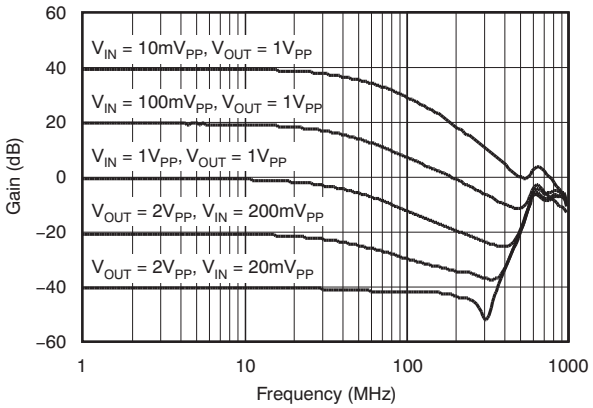



**Figure 1.**

### GAIN CONTROL FREQUENCY RESPONSE

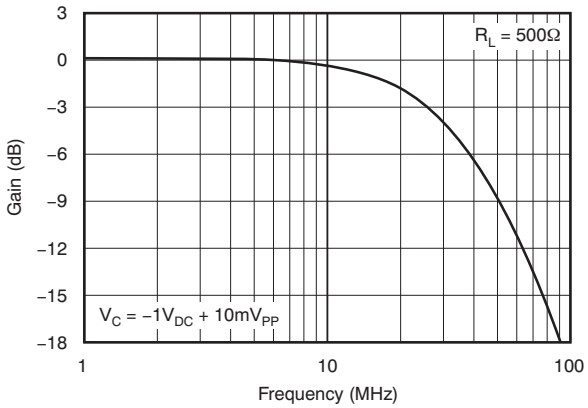



**Figure 2.**

### ATTENUATED PULSE RESPONSE

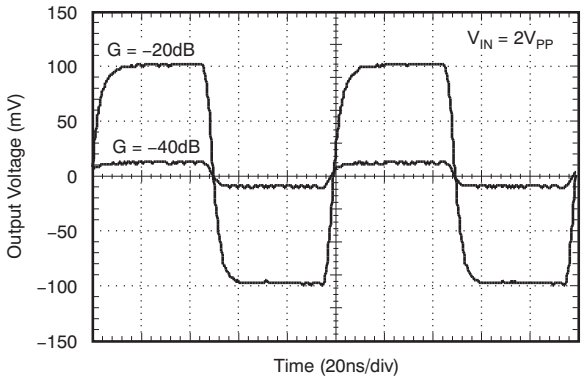



**Figure 3.**

### HIGH GAIN PULSE RESPONSE

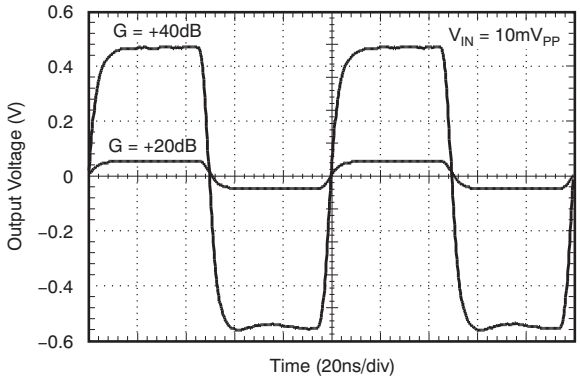



**Figure 4.**

### GAIN CONTROL PULSE RESPONSE

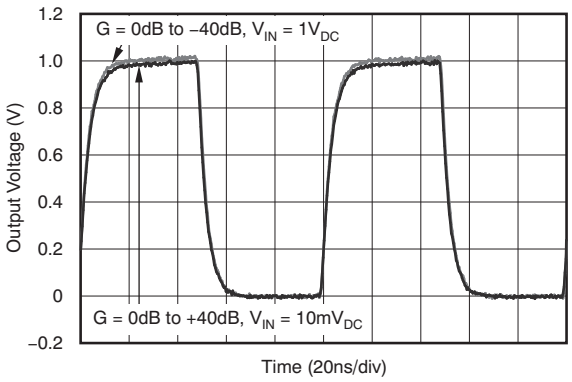



**Figure 5.**

### GAIN vs CONTROL VOLTAGE

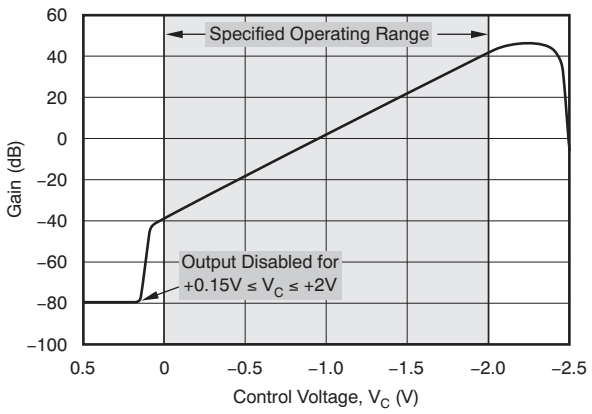



**Figure 6.**

## TYPICAL CHARACTERISTICS: $V_S$ = ±5V (continued)

At $R_L$ = 500Ω and $V_{IN}$ = single-ended input on V+ with V− at ground, unless otherwise noted.

**HARMONIC DISTORTION vs FREQUENCY**

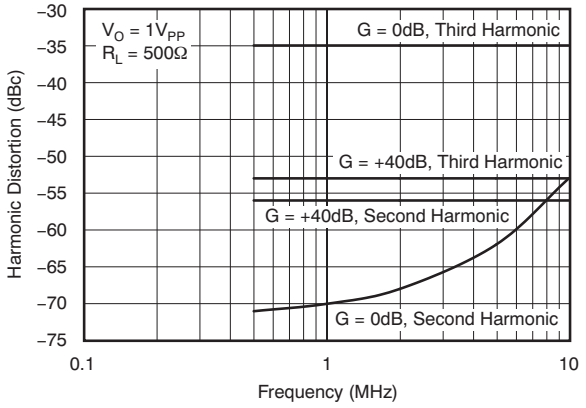



**Figure 7.**

**HARMONIC DISTORTION vs $R_{LOAD}$**

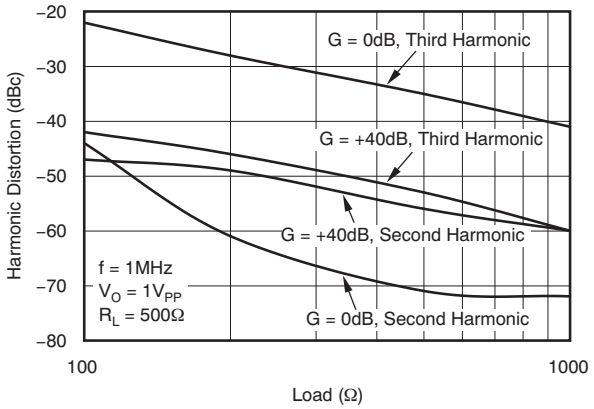



**Figure 8.**

**HARMONIC DISTORTION vs OUTPUT VOLTAGE**

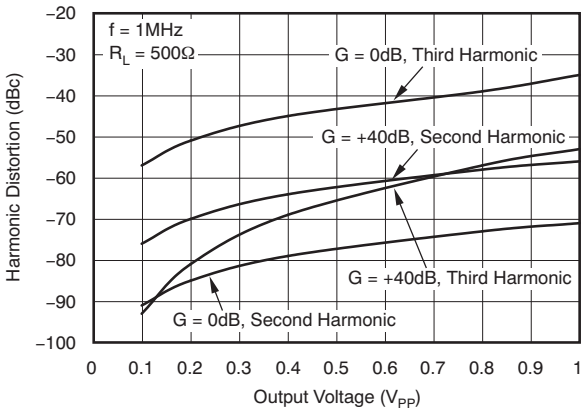



**Figure 9.**

**HARMONIC DISTORTION vs GAIN**

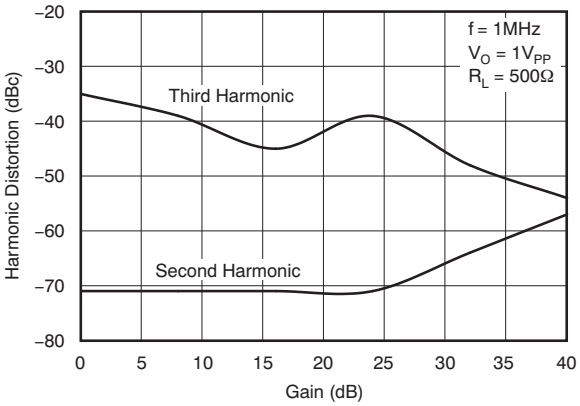



**Figure 10.**

**INPUT/OUTPUT RANGE vs GAIN**

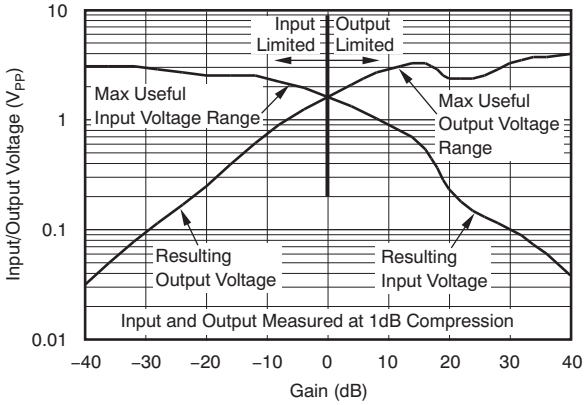



**Figure 11.**

**HARMONIC DISTORTION vs ATTENUATION**

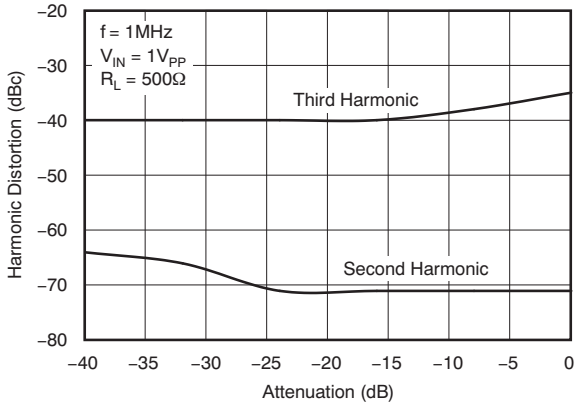



**Figure 12.**

## TYPICAL CHARACTERISTICS: $V_S$ = ±5V (continued)

At $R_L$ = 500Ω and $V_{IN}$ = single-ended input on V+ with V− at ground, unless otherwise noted.

**NOISE DENSITY vs CONTROL VOLTAGE**

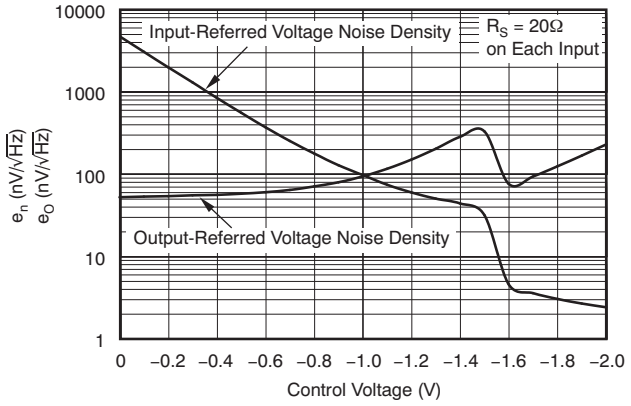



**Figure 13.**

**INPUT VOLTAGE AND CURRENT NOISE**

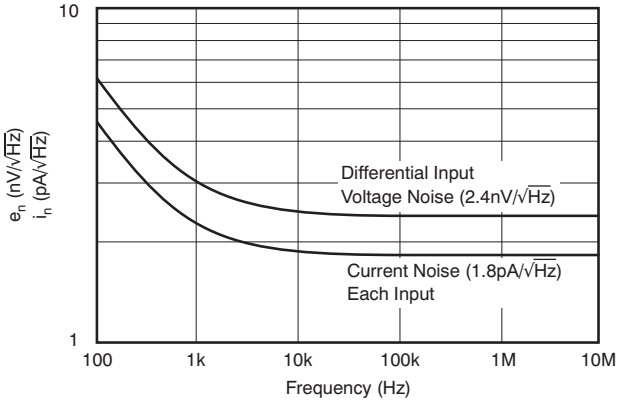



**Figure 14.**

**FULLY ATTENUATED ISOLATION vs FREQUENCY**

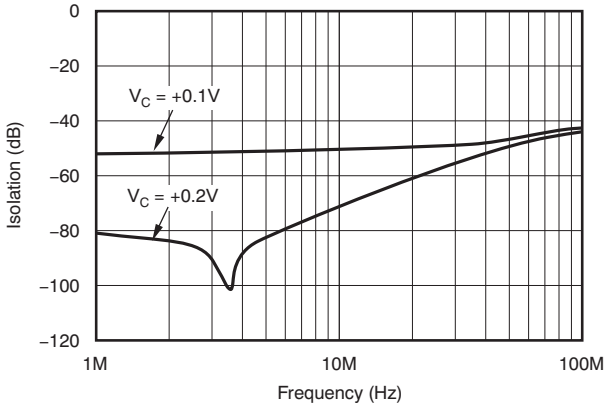



**Figure 15.**

**OUTPUT OFFSET VOLTAGE TOTAL ERROR BAND vs GAIN**

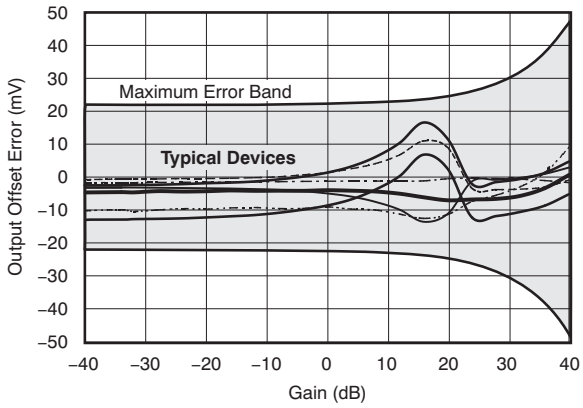



**Figure 16.**

**TYPICAL GAIN ERROR PLOT**

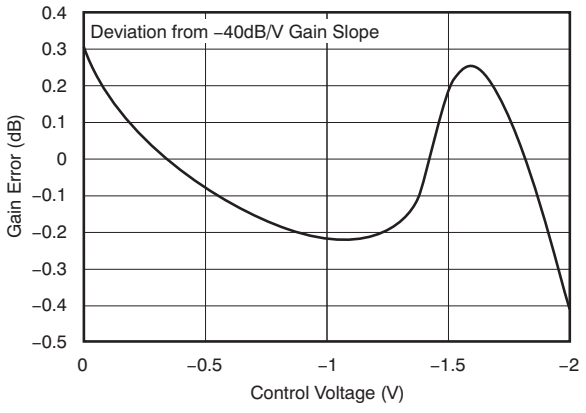



**Figure 17.**

**OUTPUT OFFSET VOLTAGE DISTRIBUTION**

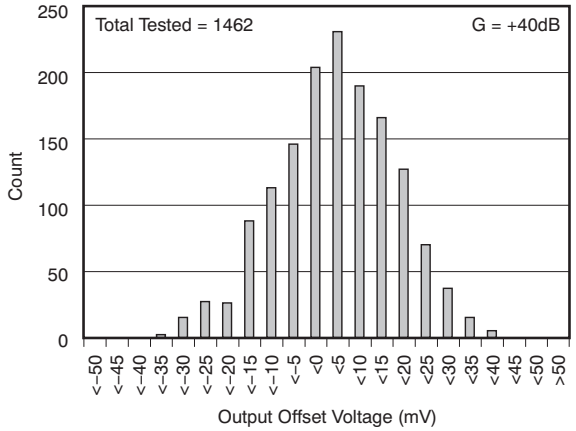



**Figure 18.**

## TYPICAL CHARACTERISTICS: $V_S$ = ±5V (continued)

At $R_L$ = 500Ω and $V_{IN}$ = single-ended input on V+ with V− at ground, unless otherwise noted.

**GROUP DELAY vs GAIN**

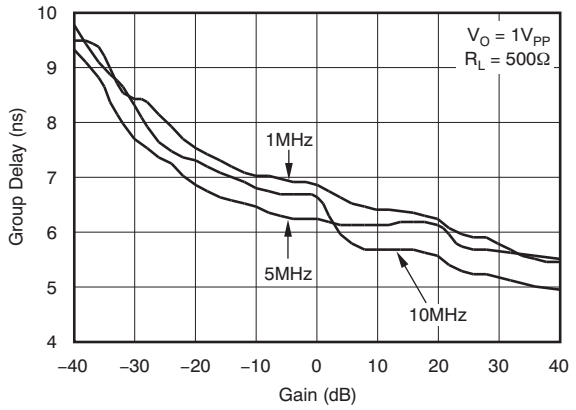



**Figure 19.**

**GROUP DELAY vs FREQUENCY**

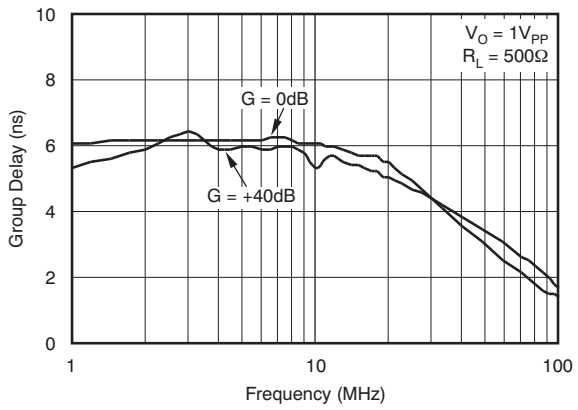



**Figure 20.**

**OVERDRIVE RECOVERY AT MAXIMUM GAIN**

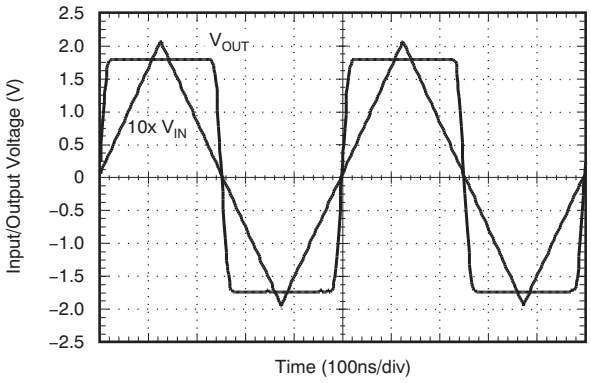



**Figure 21.**

**OVERDRIVE RECOVERY AT MAXIMUM ATTENUATION**

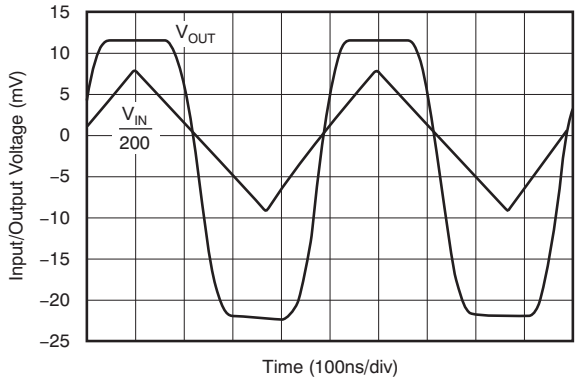



**Figure 22.**

**COMMON−MODE REJECTION RATIO AND POWER−SUPPLY REJECTION RATIO vs GAIN**

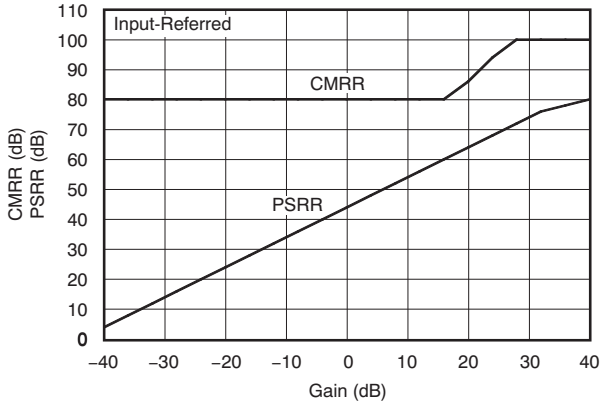



**Figure 23.**

**COMMON−MODE REJECTION RATIO AND POWER−SUPPLY REJECTION RATIO vs FREQUENCY**

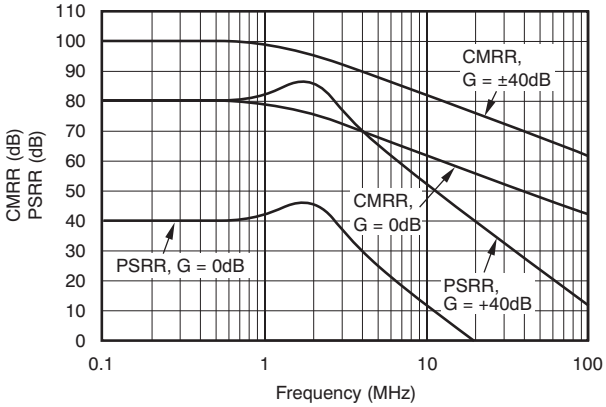



**Figure 24.**

## TYPICAL CHARACTERISTICS: $V_S$ = ±5V (continued)

At $R_L$ = 500Ω and $V_{IN}$ = single-ended input on V+ with V− at ground, unless otherwise noted.

**GAIN CONTROL +PSRR AT MAX GAIN**

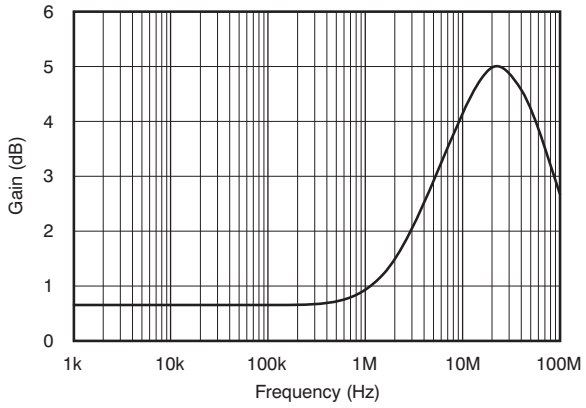



**Figure 25.**

**GAIN CONTROL −PSRR AT MAX GAIN**

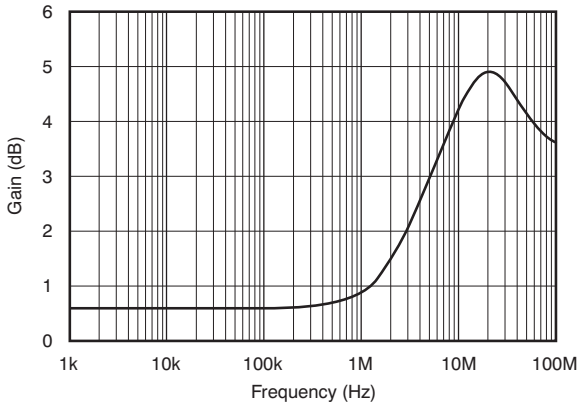



**Figure 26.**

**TYPICAL DC DRIFT vs TEMPERATURE**

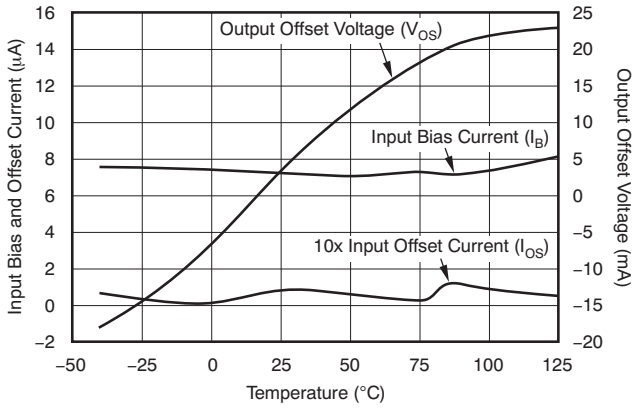



**Figure 27.**

**TYPICAL SUPPLY CURRENT vs CONTROL VOLTAGE**

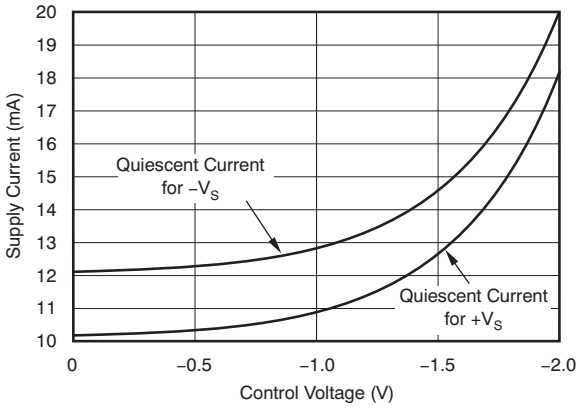



**Figure 28.**

# APPLICATION INFORMATION

## CIRCUIT DESCRIPTION

The VCA810 is a high gain adjust range, wideband, voltage amplifier with a voltage-controlled gain, as shown in Figure 29. The circuit's basic voltage amplifier responds to the control of an internal gain-control amplifier. At its input, the voltage amplifier presents the high impedance of a differential stage, permitting flexible input impedance matching. To preserve termination options, no internal circuitry connects to the input bases of this differential stage. For this reason, the user must provide dc paths for the input base currents from a signal source, either through a grounded termination resistor or by a direct connection to ground. The differential input stage also permits rejection of common-mode signals. At its output, the voltage amplifier presents a low impedance, simplifying impedance matching. An open-loop design produces wide bandwidth at all gain settings. A ground-referenced differential to single-ended conversion at the output retains the low output offset voltage.

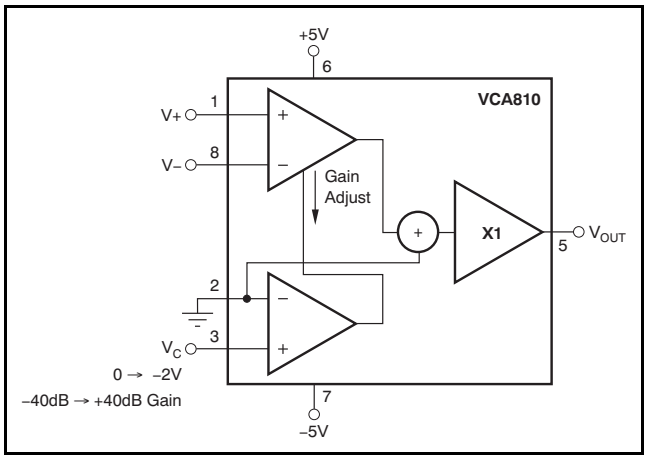



**Figure 29. Block Diagram of the VCA810**

A gain control voltage, $V_C$, controls the amplifier gain magnitude through a high-speed control circuit. Gain polarity can be either inverting or noninverting, depending upon the amplifier input driven by the input signal. The gain control circuit presents the high-input impedance of a noninverting op amp connection. The control voltage pin is referred to ground as shown in Figure 29. The control voltage $V_C$ varies the amplifier gain according to the exponential relationship:

$$G_{(V/V)} = 10^{-2(V_C + 1)}$$

This translates to the log gain relationship:

$$G_{(dB)} = -40 \bullet (V_C + 1)\text{dB}.$$

Thus, $G_{(dB)}$ varies linearly over the specified −40dB to +40dB range as $V_C$ varies from 0V to −2V. Optionally, making $V_C$ slightly positive (≥ +0.15V) effectively disables the amplifier, giving greater than 80dB of signal path attenuation at low frequencies.

Internally, the gain-control circuit varies the amplifier gain by varying the transconductance, $g_m$, of a bipolar transistor using the transistor bias current. Varying the bias currents of differential stages varies $g_m$ to control the voltage gain of the VCA810. A $g_m$-based gain adjust normally suffers poor thermal stability. The VCA810 includes circuitry to minimize this effect.

## VCA810 OPERATION

Figure 30 shows the circuit configuration used as the basis of the *Electrical Characteristics* and *Typical Characteristics*. Voltage swings reported in the specifications are taken directly at the input and output pins. For test purposes, the input impedance is set to 50Ω with a resistance to ground. A 25Ω resistance ($R_T$) is included on the V− input to get bias current cancellation. Proper supply bypassing is shown in Figure 30, and consists of two capacitors on each supply pin: one large electrolytic capacitor (2.2μF to 6.8μF), effective at lower frequencies, and one small ceramic capacitor (0.1μF) for high-frequency decoupling. For more information on decoupling, refer to the *Board Layout* section.

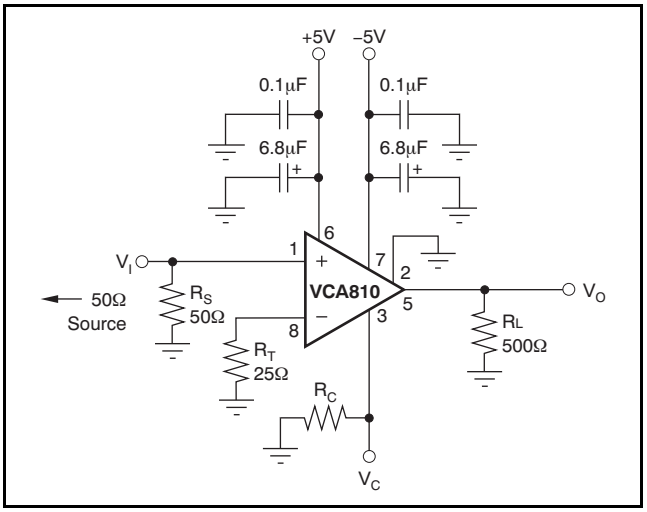



**Figure 30. Variable Gain, Specification and Test Circuit**

Notice that both inverting and noninverting inputs are connected to ground with a resistor ($R_S$ and $R_T$). Matching the dc source impedance looking out of each input will minimize input offset voltage error.

## RANGE-FINDING TGC AMPLIFIER

The block diagram in Figure 31 illustrates the fundamental configuration common to pulse-echo range finding systems. A photodiode preamp provides an initial gain stage to the photodiode.

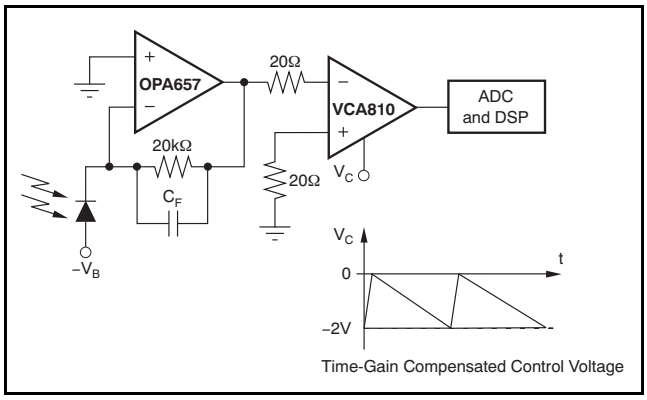



**Figure 31. Typical Range-Finding Application**

The control voltage $V_C$ varies the amplifier gain for a basic signal-processing requirement: compensation for distance attenuation effects, sometimes called *time-gain compensation* (TGC). Time-gain compensation increases the amplifier gain as the signal moves through the air to compensate for signal attenuation. For this purpose, a ramp signal applied to the VCA810 gain control input linearly increases the dB gain of the VCA810 with time.

## WIDE-RANGE AGC AMPLIFIER

The voltage-controlled gain feature of the VCA810 makes this amplifier ideal for precision AGC applications with control ranges as large as 60dB. The AGC circuit of Figure 32 adds an op amp and diode for amplitude detection, a hold capacitor to store the control voltage and resistors $R_1$ through $R_3$ that determine attack and release times. Resistor $R_4$ and capacitor $C_C$ phase-compensate the AGC feedback loop. The op amp compares the positive peaks of output $V_O$ with a dc reference voltage, $V_R$. Whenever a $V_O$ peak exceeds $V_R$, the OPA820 output swings positive, forward-biasing the diode and charging the holding capacitor. This charge drives the capacitor voltage in a positive direction, reducing the amplifier gain. $R_3$ and the $C_H$ largely determine the attack time of this AGC correction. Between gain corrections, resistor $R_1$ charges the capacitor in a negative direction, increasing the amplifier gain. $R_1$, $R_2$, and $C_H$ determine the release time of this action. Resistor $R_2$ forms a voltage divider with $R_1$, limiting the maximum negative voltage developed on $C_H$. This limit prevents input overload of the VCA810 gain control circuit.

Figure 33 shows the AGC response for the values shown in Figure 32.

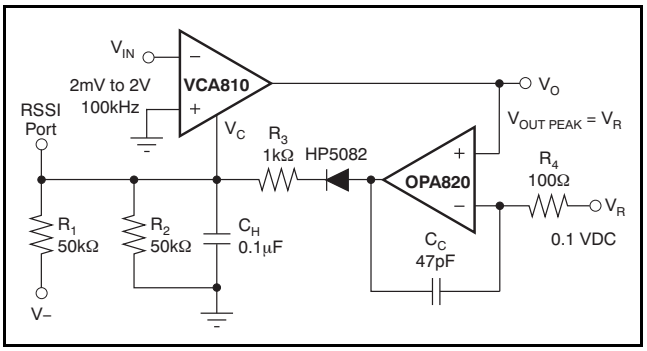



**Figure 32. 60dB Input Range AGC**

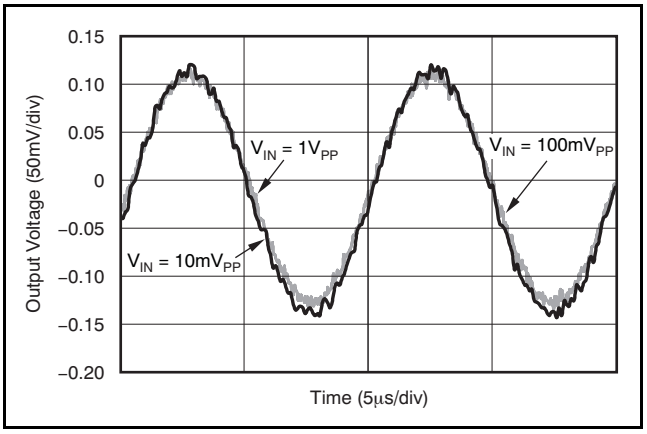



**Figure 33. AGC Output Voltage for 100kHz Sinewave at $10mV_{PP}$, $100mV_{PP}$, and $1V_{PP}$**

## STABILIZED WEIN-BRIDGE OSCILLATOR

Adding Wein-bridge feedback to the above AGC amplifier produces an amplitude-stabilized oscillator. As Figure 34 shows, this alternative requires the addition of just two resistors ($R_{W1}$, $R_{W2}$) and two capacitors ($C_{W1}$, $C_{W2}$).

Connecting the feedback network to the amplifier noninverting input introduces positive feedback to induce oscillation. The feedback factor displays a frequency dependence due to the changing impedances of the $C_W$ capacitors. As frequency increases, the decreasing impedance of the $C_{W2}$ capacitor increases the feedback factor. Simultaneously, the decreasing impedance of the $C_{W1}$ capacitor decreases this factor. Analysis shows that the maximum factor occurs at $f_W = \frac{1}{2\pi R_W C_W}$ Hz, making this the frequency most conducive to oscillation. At this frequency, the impedance magnitude of $C_W$ equals $R_W$, and inspection of the circuit shows that this condition produces a feedback factor of 1/3. Thus, self-sustaining oscillation requires a gain of three through the amplifier. The AGC circuitry establishes this gain level. Following initial circuit turn-on, $R_1$ begins charging $C_H$ negative, increasing the amplifier gain from its minimum. When this gain reaches three, oscillation begins at $f_W$; the continued charging effect of $R_1$ makes the oscillation amplitude grow. This growth continues until that amplitude reaches a peak value equal to $V_R$. Then, the AGC circuit counteracts the $R_1$ effect, controlling the peak amplitude at $V_R$ by holding the amplifier gain at a level of three. Making $V_R$ an ac signal, rather than a dc reference, produces amplitude modulation of the oscillator output.

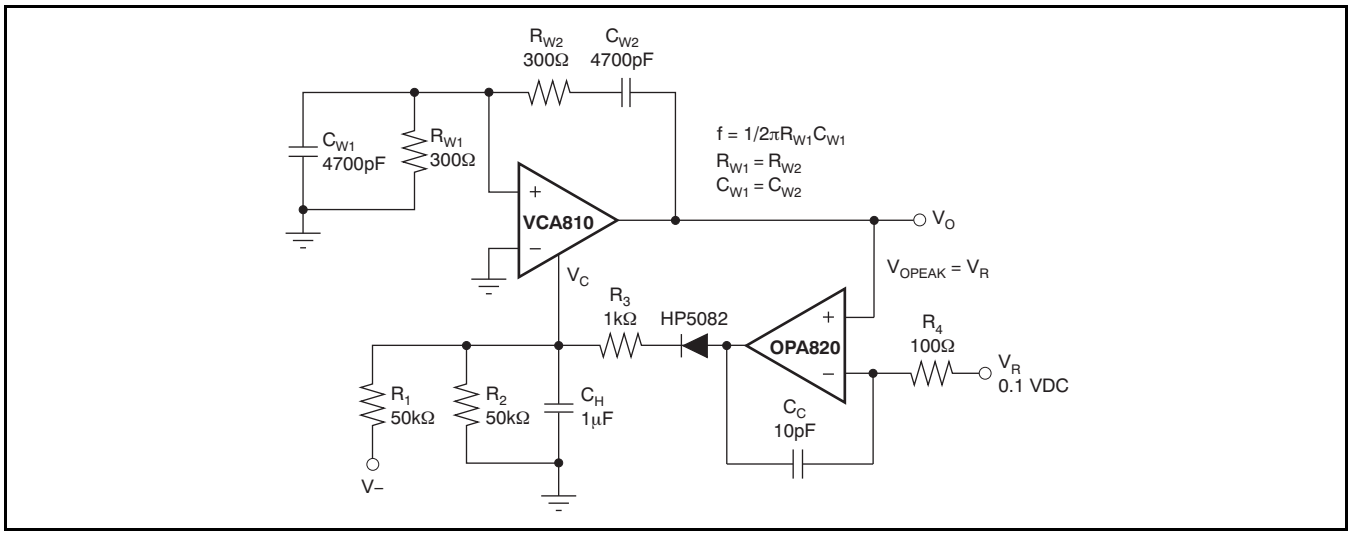



**Figure 34. Amplitude-Stabilized Oscillator**

## LOW-DRIFT WIDEBAND LOG AMP

The VCA810 can be used to provide a 2.5MHz (–3dB) log amp with low offset voltage and low gain drift. The exponential gain-control characteristic of the VCA810 permits simple generation of a temperature-compensated logarithmic response. Enclosing the exponential function in an op-amp feedback path inverts this function, producing the log response. Figure 35 shows the practical implementation of this technique. A dc reference voltage, $V_R$, sets the VCA810 inverting input voltage. This configuration makes the amplifier output voltage $V_{OA} = -GV_R$, where $G = 10^{-2\,(V_C + 1)}$.

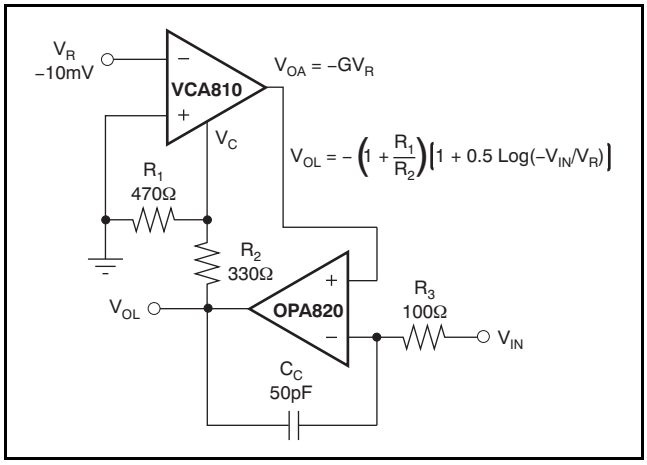



**Figure 35. Temperature-Compensated Log Response**

A second input voltage also influences $V_{OA}$ through control of gain G. The feedback op amp forces $V_{OA}$ to equal the input voltage $V_{IN}$ connected at the op amp inverting input. Any difference between these two signals drops across $R_3$, producing a feedback current that charges $C_C$. The resulting change in $V_{OL}$ adjusts the gain of the VCA810 to change $V_{OA}$.

At equilibrium:

$$V_{OA} = V_{IN} = -V_R \bullet 10^{-2\,(V_C + 1)} \quad (1)$$

The op amp forces this equality by supplying the gain control voltage, $V_C = \dfrac{R_1 \bullet V_{OL}}{R_1 + R_2}$.

Combining the last two expressions and solving for $V_{OL}$ yields the circuit's logarithmic response:

$$V_{OL} = -\left(1 + \frac{R_2}{R_1}\right) \bullet \left[1 + 0.5 \bullet \log\left(-\frac{V_{IN}}{V_R}\right)\right] \quad (2)$$

An examination of this result illustrates several circuit characteristics. First, the argument of the log term, $-V_{IN}/V_R$, reveals an option and a constraint. In Figure 35, $V_R$ represents a dc reference voltage. Optionally, making this voltage a second signal produces log-ratio operation. Either way, the log term's argument constrains the polarities of $V_R$ and $V_{IN}$. These two voltages must be of opposite polarities to ensure a positive argument. This polarity combination results when $V_R$ connects to the inverting input of the VCA810. Alternately, switching $V_R$ to the amplifier noninverting input removes the minus sign of the log term argument. Then, both voltages must be of the same polarity in order to produce a positive argument. In either case, the positive polarity requirement of the argument restricts $V_{IN}$ to a unipolar range. Figure 36 illustrates these constraints.

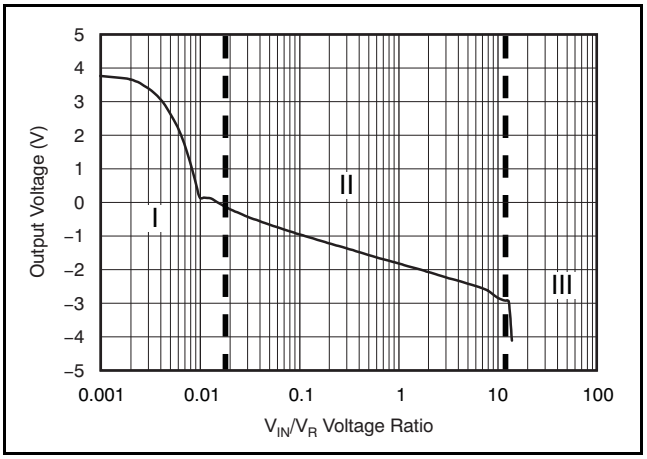



**Figure 36. Test Result for LOG Amp for $V_R$ = −100mV**

The above $V_{OL}$ expression reflects a circuit gain introduced by the presence of $R_1$ and $R_2$. This feature adds a convenient scaling control to the circuit. However, a practical matter sets a minimum level for this gain. The voltage divider formed by $R_1$ and $R_2$ attenuates the voltage supplied to the $V_C$ terminal by the op amp. This attenuation must be great enough to prevent any possibility of an overload voltage at the $V_C$ terminal. Such an overload saturates the VCA810 gain-control circuitry, reducing the amplifier's gain. For the feedback connection of Figure 35, this overload condition permits a circuit latch. To prevent this, choose $R_1$ and $R_2$ to ensure that the op amp cannot possibly deliver a more negative input than −2.5V to the $V_C$ terminal.

Figure 36 exhibits three zones of operation described below:

**Zone I:** $V_C$ > 0V. The VCA810 is operating in full attenuation (−80dB). The noninverting input of the OPA820 will see ~0V. $V_{OL}$ is going to be the integration of the input signal.

**Zone II:** −2V < $V_C$ < 0V. The VCA810 is in its normal operating mode, creating the log relationship in Equation 2.

**Zone III:** $V_C$ < −2V. The VCA810 control pin is out of range, and some measure should be taken so that it does not exceed –2.5V. A limiting action could be achieved by using a voltage limiting amplifier.

## LOW-DRIFT, WIDEBAND EXPONENTIAL AMP

A common use of the log amp above involves signal compounding. The inverse function, signal expanding, requires an exponential transfer function. The VCA810 produces this latter response directly, as shown in Figure 37. DC reference $V_R$ again sets the amplifier input voltage, and the input signal $V_{IN}$ now drives the gain control point. Resistors $R_1$ and $R_2$ attenuate this drive to prevent overloading the gain control input. Setting these resistors at the same values as in the preceding log amp produces an exponential amplifier with the inverse function of the log amp.

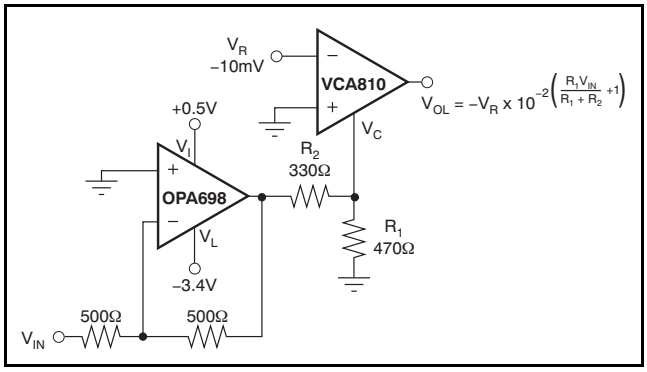



**Figure 37. Exponential Amplifier**

Testing the circuit given in Figure 37 gives the exponential response shown in Figure 38.

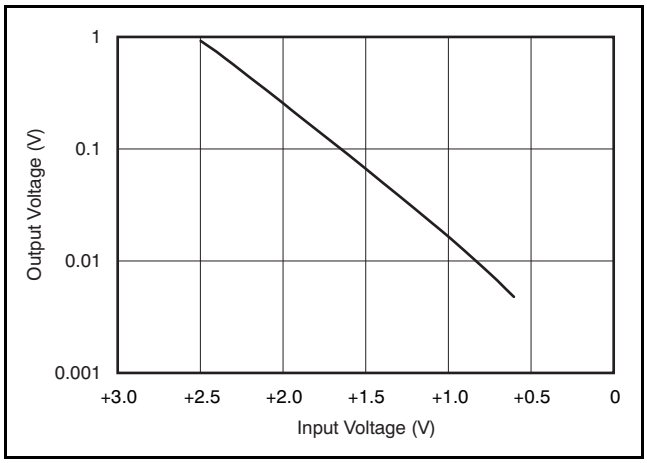



**Figure 38. Exponential Amplifier Response**

## VOLTAGE-CONTROLLED LOW-PASS FILTER

In the circuit of Figure 39, the VCA810 serves as the variable-gain element of a voltage-controlled low-pass filter. This section discusses how this implementation expands the circuit voltage swing capability over that normally achieved with the equivalent multiplier implementation. The circuit response pole responds to control voltage $V_C$ according to the relationship in Equation 3:

$$f_P = \frac{G}{2\pi R_2 C} \quad (3)$$

where $G = 10^{-2\,(V_C + 1)}$

With the components shown, the circuit provides a linear variation of the low-pass cutoff from 300Hz to 1MHz.

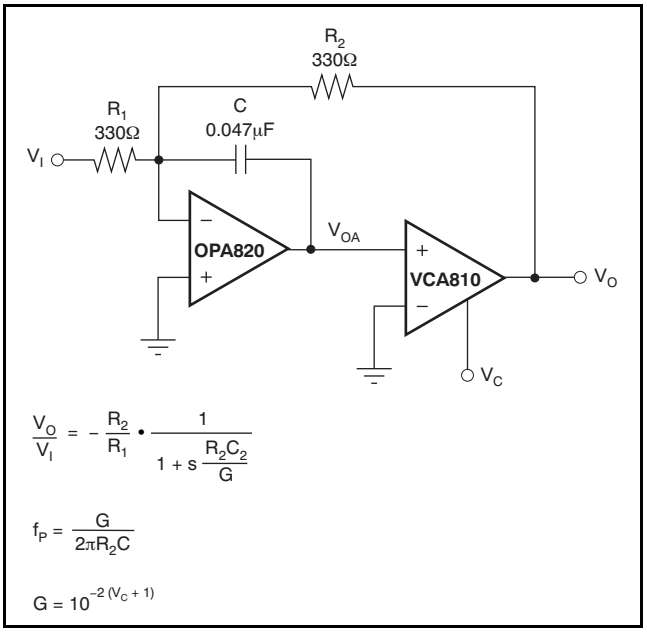



**Figure 39. Tunable Low-Pass Filter**

The response control results from amplification of the feedback voltage applied to $R_2$. First, consider the case where the VCA810 produces G = 1. Then, the circuit performs as if this amplifier were replaced by a short circuit. Visually doing so leaves a simple voltage amplifier with a feedback resistor bypassed by a capacitor. This basic circuit produces a response pole at $f_P = \frac{G}{2\pi R_2 C}$.

For G > 1, the circuit applies a greater voltage to $R_2$, increasing the feedback current this resistor supplies to the summing junction of the OPA820. The increased feedback current produces the same result as if $R_2$ had been decreased in value in the basic circuit described above. Decreasing the effective $R_2$ resistance moves the circuit pole to a higher frequency, producing the $f_P = \frac{G}{2\pi R_2 C}$ response control.

Finite loop gain and a signal-swing limitation set performance boundaries for the circuit. Both limitations occur when the VCA810 attenuates, rather than amplifies, the feedback signal. These two limitations reduce the circuit's utility at the lower extreme of the VCA810 gain range. For $-1 \le V_C \le 0$, this amplifier produces attenuating gains in the range from 0dB to −40dB. This range directly reduces the net gain in the circuit's feedback loop, increasing gain error effects. Additionally, this attenuation transfers an output swing limitation from the OPA820 output to the overall circuit's output. Note that OPA820 output voltage, $V_{OA}$, relates to $V_O$ through the expression, $V_O = G \bullet V_{OA}$. Thus, a G < 1 limits the maximum $V_O$ swing to a value less than the maximum $V_{OA}$ swing.

Figure 40 shows the low-pass frequency for different control voltages.

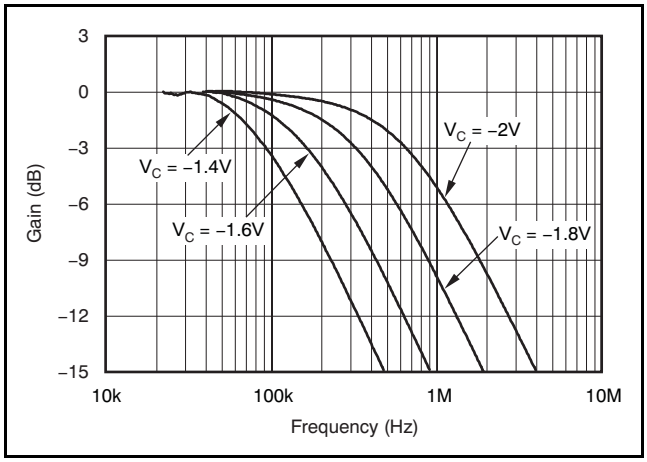



**Figure 40. Voltage-Controlled Low-Pass Filter Frequency Response**

## TUNABLE EQUALIZER

A circuit analogous to the above low-pass filter produces a voltage-controlled equalizer response. The gain control provided by the VCA810 of Figure 41 varies this circuit response zero from 1Hz to 10kHz, according to the relationship of Equation 4:

$$f_Z \approx \frac{G}{2\pi G R_1 C} \quad (4)$$

To visualize the circuit's operation, consider a circuit condition and an approximation that permit replacing the VCA810 and $R_3$ with short circuits. First, consider the case where the VCA810 produces G = 1. Replacing this amplifier with a short circuit leaves the operation unchanged. In this shorted state, the circuit is simply a voltage amplifier with an R-C bypass around $R_1$. The resistance of this bypass, $R_3$, serves only to phase-compensate the circuit, and practical factors make $R_3 << R_1$. Neglecting $R_3$ for the moment, the circuit becomes just a voltage amplifier with a capacitive bypass of $R_1$. This circuit produces a response zero at $f_Z \approx \frac{1}{2\pi R_1 C}$.

Adding the VCA810 as shown in Figure 41 permits amplification of the signal applied to capacitor C, and produces voltage control of the frequency $f_Z$. Amplified signal voltage on C increases the signal current conducted by the capacitor to the op amp feedback network. The result is the same as if C had been increased in value to $G_C$. Replacing C with this effective capacitance value produces the circuit control expression $f_Z \approx \frac{1}{2\pi R_1 G C}$.

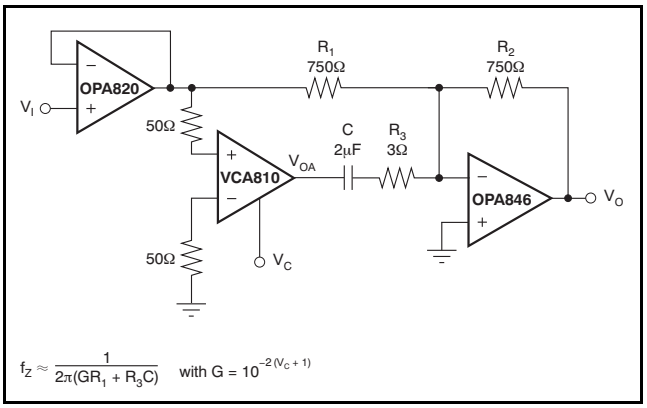



**Figure 41. Tunable Equalizer**

Another factor limits the high-frequency performance of the resulting high-pass filter: the finite bandwidth of the op amp. This limits the frequency duration of the equalizer response. Limitations such as bandwidth and stability are clearly shown in Figure 42.

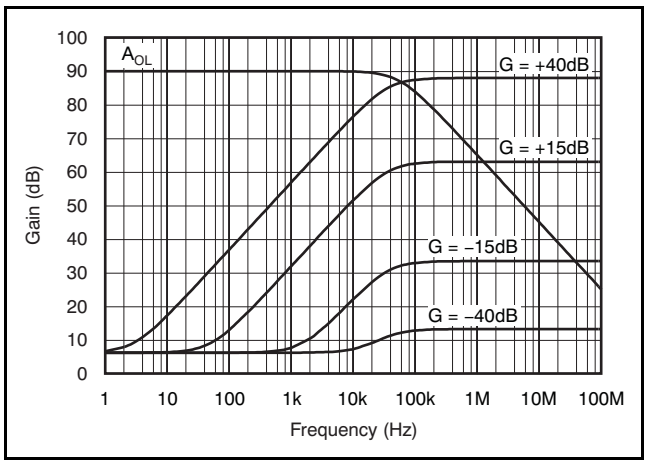



**Figure 42. Amplifier Noise Gain and $A_{OL}$ for Different Gain**

Other limitations of this circuit are stability versus VCA810 gain and input signal level for the circuit. Figure 42 also illustrates these two factors. As the VCA810 gain increases, the crossover slope between the $A_{OL}$ curve of the OPA846 and noise gain will be greater than 20dB/decade, rendering the circuit unstable. The signal level for high gain of the VCA810 will meet two limitations: the output voltage swings of both the VCA810 and the OPA846. The expression $V_{OA} = GV_I$ relates these two voltages. Thus, an output voltage limit $V_{OAL}$ constrains the input voltage to $V_I \le V_{OAL}/G$.

With the components shown, BW = 50kHz. This bandwidth provides an integrator response duration of four decades of frequency for $f_Z$ = 1Hz, dropping to one decade for $f_Z$ = 10kHz.

## VOLTAGE-CONTROLLED BAND-PASS FILTER

The variable gain of the VCA810 also provides voltage control over the center frequency of a band-pass filter. As shown in Figure 43, this filter follows from the state-variable configuration with the VCA810 replacing the inverter common to that configuration. Variation of the VCA810 gain moves the filter's center frequency through a 100:1 range following the relationship of Equation 5:

$$f_O = \frac{10^{-(V_C + 1)}}{2\pi RC} \quad (5)$$

As before, variable gain controls a circuit time constant to vary the filter response. The gain of the VCA810 amplifies or attenuates the signal driving the lower integrator of the circuit. This amplification alters the effective resistance of the integrator time constant, producing the response of Equation 6:

$$\frac{V_O}{V_I} = \frac{-\frac{s}{nRC}}{s^2 + \frac{s}{nRC} + \frac{G}{R^2C^2}} \quad (6)$$

Evaluation of this response equation reveals a passband gain of $A_O$ = –1, a bandwidth of BW = $1/(2\pi RC)$, and a selectivity of $Q = n \bullet 10^{-(V_C + 1)}$. Note that variation of control voltage $V_C$ alters Q but not bandwidth.

The gain provided by the VCA810 restricts the output swing of the filter. Output signal $V_O$ must be constrained to a level that does not drive the VCA810 output, $V_{OA}$, into its saturation limit. Note that these two outputs have voltage swings related by $V_{OA} = G_{VO}$. Thus, a swing limit $V_{OAL}$ imposes a circuit output limit of $V_{OL} \le V_{OAL}/G$.

See Figure 44 for the frequency response for two different gain conditions of the schematic shown in Figure 43. In particular, notice the center frequency shift and the selectivity of Q changing as the gain is increased.

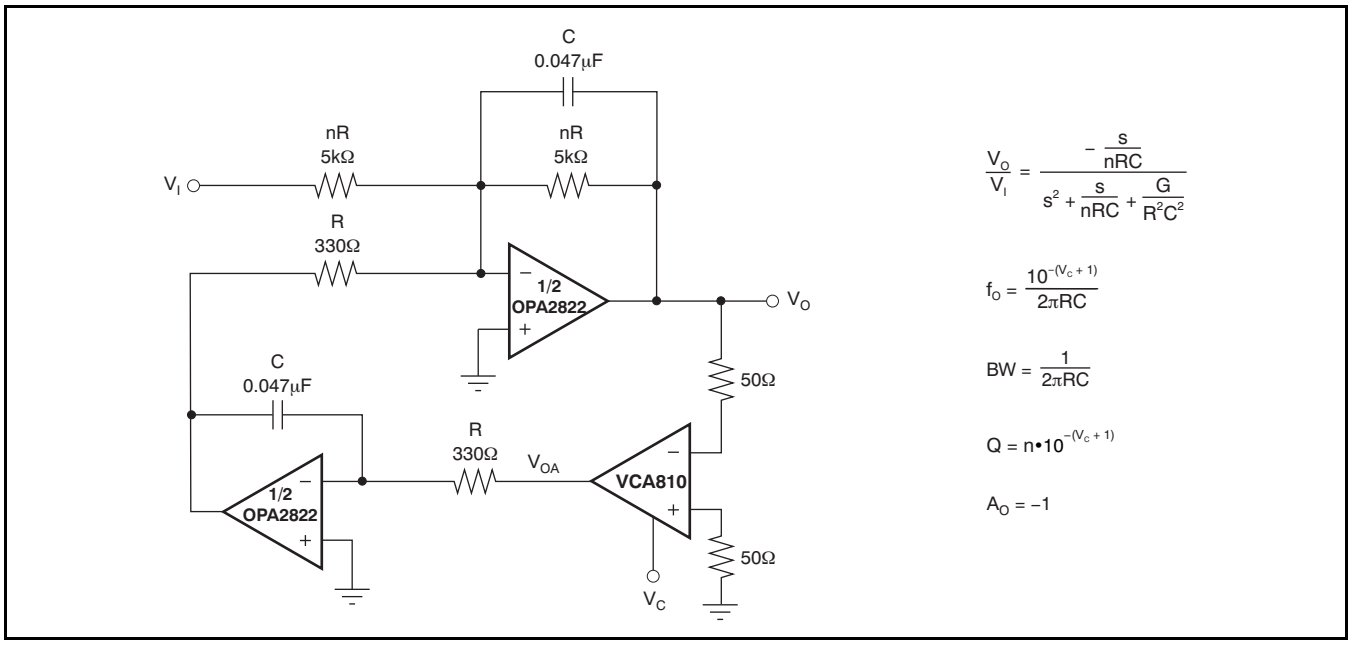



**Figure 43. Tunable Band-Pass Filter**

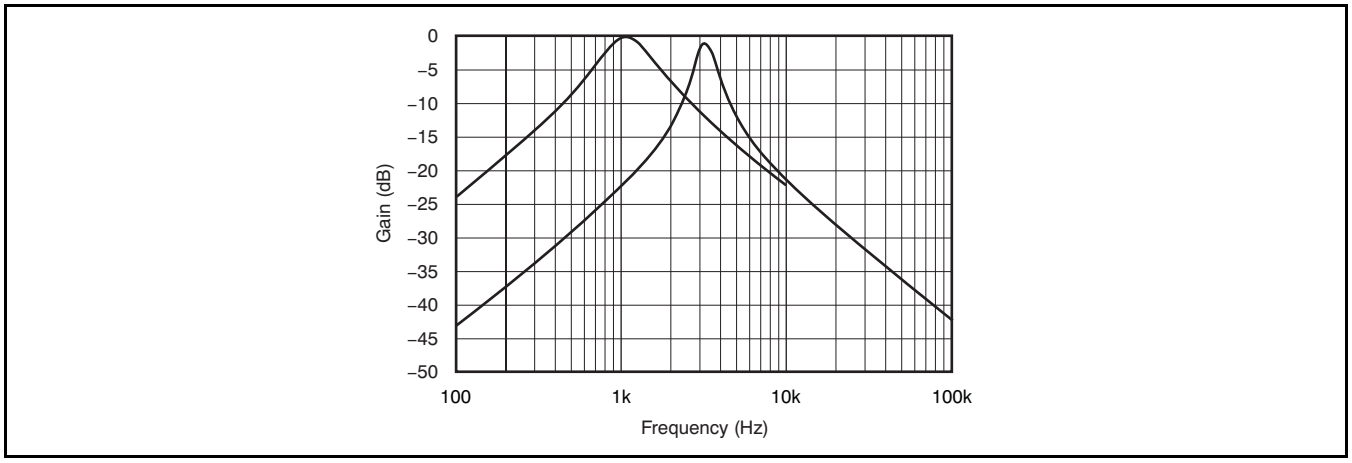



**Figure 44. Tunable Band-Pass Filter Response**

## DESIGN-IN TOOLS

### DEMONSTRATION BOARDS

A printed circuit board (PCB) is available to assist in the initial evaluation of circuit performance using the VCA810. This evaluation board (EVM) is available free, as an unpopulated PCB delivered with descriptive documentation. The summary information for this board is shown in Table 1.

**Table 1. EVM Ordering Information**

| PRODUCT | PACKAGE | BOARD PART NUMBER | LITERATURE REQUEST NUMBER |
|---|---|---|---|
| VCA810ID | SO-8 | DEM-VCA-SO-1A | SBOU025 |

Go to the Texas Instruments website (www.ti.com) to request an evaluation board through the VCA810 product folder.

## MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can play a major role in circuit performance. A SPICE model for the VCA810 is available through the TI web page. The applications group is also available for design assistance. The models available from TI predict typical small-signal ac performance, transient steps, dc performance, and noise under a wide variety of operating conditions. The models include the noise terms found in the electrical specifications of the relevant product data sheet.

# OPERATING SUGGESTIONS

## INPUT/OUTPUT RANGE

The VCA810's 80dB gain range allows the user to handle an exceptionally wide range of input signal levels. If the input and output voltage range specifications are exceeded, however, signal distortion and amplifier overdrive will occur. The VCA810 maximum input and output voltage range is best illustrated in the Typical Characteristics plot, *Input/Output Range vs Gain* (Figure 11). This chart plots input and output voltages versus gain in dB.

The maximum input voltage range is the largest at full attenuation (−40dB) and decreases as the gain increases. Similarly, the maximum useful output voltage range increases as the input decreases. We can distinguish three overloading issues as a result of the operating mode: high attenuation, mid-range gain-attenuation, and high gain.

From –40dB to –10dB, gain overdriving the input stage is the only method to overdrive the VCA810. Preventing this type of overdrive is achieved by limiting the input voltage range.

From –10dB to +40dB, overdriving can be prevented by limiting the output voltage range. There are two limiting mechanisms operating in this situation. From –10dB to +10dB, an internal stage is the limiting factor; from +10dB to +40dB, the output stage is the limiting factor.

Output overdriving occurs when either the maximum output voltage swing or output current is exceeded. The VCA810 high output current of ±60mA ensures that virtually all output overdrives will be limited by voltage swing rather than by current limiting. Table 2 summarizes these overdrive conditions.

**Table 2. Output Signal Compression**

| GAIN RANGE | LIMITING MECHANISM | TO PREVENT, OPERATE DEVICE WITHIN: |
|---|---|---|
| −40dB < G < −10dB | Input Stage Overdrive | Input Voltage Range |
| −10dB < G < +10dB | Internal Stage Overdrive | Output Voltage Range |
| +5dB < G < +40dB | Output Stage Overdrive | Output Voltage Range |

## OVERDRIVE RECOVERY

As shown in the Typical Characteristics plot, *Input/Output Range vs Gain* (Figure 11), the onset of overdrive occurs whenever the actual output begins to deviate from the ideal expected output. If possible, the user should operate the VCA810 within the linear regions shown in order to minimize signal distortion and overdrive delay time. However, instances of amplifier overdrive are quite common in automatic gain control (AGC) circuits, which involve the application of variable gain to input signals of varying levels. The VCA810 design incorporates circuitry that allows it to recover from most overdrive conditions in 200ns or less. Overdrive recovery time is defined as the time required for the output to return from overdrive to linear operation, following the removal of either an input or gain-control overdrive signal. The overdrive plots for maximum gain and maximum attenuation are shown in the *Typical Characteristics*.

## OUTPUT OFFSET ERROR

Several elements contribute to the output offset voltage error; among them are the input offset voltage, the output offset voltage, the input bias current and the input offset current. To simplify the following analysis, the output offset voltage error is dependent only on the output-offset voltage of the VCA810 and the input offset voltage. The output offset error can then be expressed as Equation 7:

$$V_{OS} = V_{OSO} + 10^{\left(\frac{G_{dB}}{20}\right)} \bullet V_{IOS} \quad (7)$$

Where:

- $V_{OS}$ = Output offset error
- $V_{OSO}$ = Output offset voltage
- $G_{dB}$ = VCA810 gain in dB
- $V_{IOS}$ = Input offset voltage

This is shown in Figure 45.

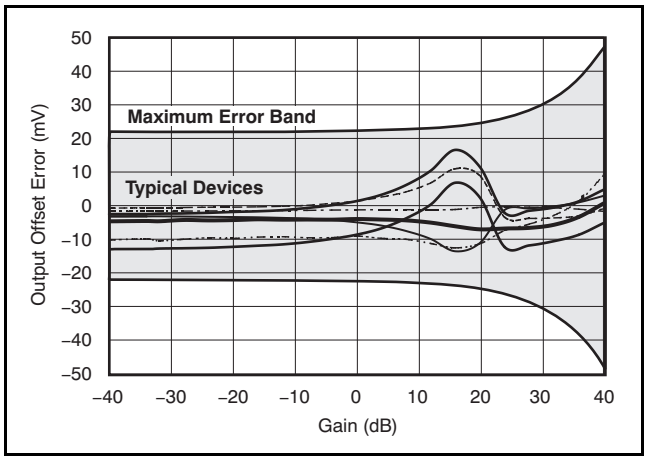



**Figure 45. Output Offset Error versus Gain**

The histogram *Output Offset Voltage at Maximum Gain* (Figure 18) in the Typical Characteristics curves shows the distribution for the output offset voltage at maximum gain.

## OFFSET ADJUSTMENT

Where desired, the offset of the VCA810 can be removed as shown in Figure 46. This circuit simply presents a dc voltage to one of the amplifier inputs to counteract the offset error voltage. For best offset performance, the trim adjustment should be made with the amplifier set at the maximum gain of the intended application. The offset voltage of the VCA810 varies with gain as shown in Figure 45, limiting the complete offset cancellation to one selected gain. Selecting the maximum gain optimizes offset performance for higher gains where high amplification of the offset effects produces the greatest output offset. Two features minimize the offset control circuit noise contribution to the amplifier input circuit. First, making the resistance of $R_2$ a low value minimizes the noise directly introduced by the control circuit. This approach reduces both the thermal noise of the resistor and the noise produced by the resistor with the amplifier input noise current. A second noise reduction results from capacitive bypass of the potentiometer output. This reduction filters out power-supply noise that would otherwise couple to the amplifier input.

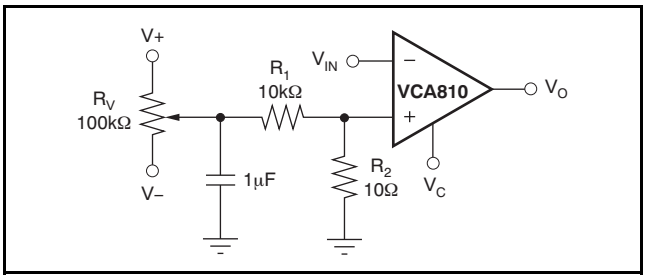



**Figure 46. Optional Offset Adjustment**

This filtering action diminishes as the wiper position approaches either end of the potentiometer, but practical conditions prevent such settings. Over its full adjustment range, the offset control circuit produces a ±5mV input offset correction for the values shown. However, the VCA810 only requires one-tenth of this range for offset correction, assuring that the potentiometer wiper will always be near the potentiometer center. With this setting, the resistance seen at the wiper remains high, which stabilizes the filtering function.

## GAIN CONTROL

The VCA810 gain is controlled by means of a unipolar negative voltage applied between ground and the gain control input, pin 3. If use of the output disable feature is required, a ground-referenced bipolar voltage is needed. Output disable occurs for $+0.15V \le V_C \le +2V$, and produces greater than 80dB of attenuation. The control voltage should be limited to +2V in disable mode, and –2.5V in gain mode in order to prevent saturation of internal circuitry. The VCA810 gain-control input has a –3dB bandwidth of 25MHz and varies with frequency, as shown in the *Typical Characteristics* curves. This wide bandwidth, although useful for many applications, can allow high-frequency noise to modulate the gain control input. In practice, this can be easily avoided by filtering the control input, as shown in Figure 47. $R_P$ should be no greater than 100Ω so as not to introduce gain errors by interacting with the gain control input bias current of 6μA.

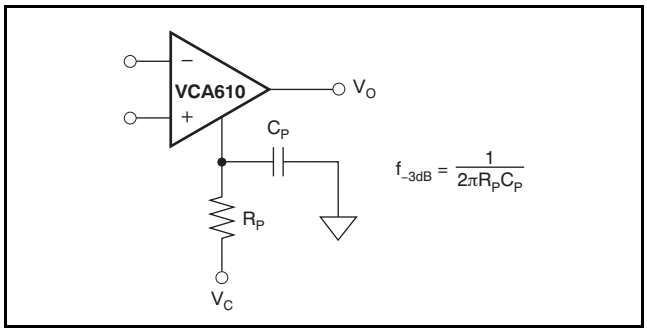



**Figure 47. Control Line Filtering**

## GAIN CONTROL AND TEEPLE POINT

When the VCA810 control voltage reaches −1.5V, also referred to as the *Teeple point*, the signal path undergoes major changes. From 0V to the Teeple point, the gain is controlled by one bank of amplifiers: a low-gain VCA. As the Teeple point is passed, the signal path is switched to a higher gain VCA. This gain-stage switching can be seen most clearly in the *Noise Density vs Control Voltage* Typical Characteristics curve (Figure 13). The output-referred voltage noise density increases proportionally to the control voltage and reaches a maximum value at the Teeple point. As the gain increases and the internal stages switch, the output-referred voltage noise density drops suddenly and restarts its proportional increase with the gain.

## NOISE PERFORMANCE

The VCA810 offers 2.4nV/√Hz input-referred voltage noise and 1.8 pA/√Hz input-referred current noise at a gain of +40dB. The input-referred voltage noise, and the input-referred current noise terms, combine to give low output noise under a wide variety of operating conditions. Figure 48 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

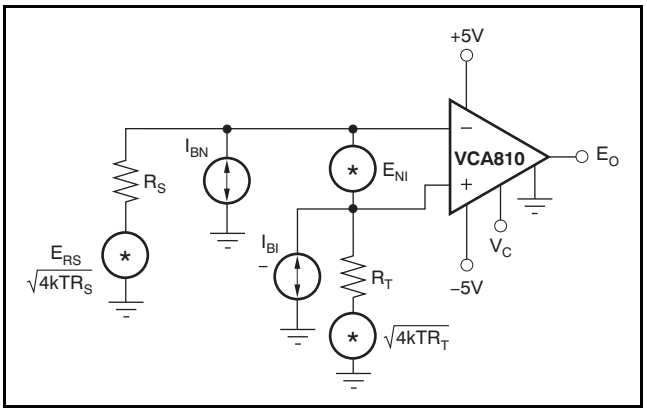



**Figure 48. VCA810 Noise Analysis Model**

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 8 shows the general form for the output noise voltage using the terms shown in Figure 48.

$$E_O = G_{(V/V)} \bullet \sqrt{E_{NI}^2 + (I_{BI}R_T)^2 + (I_{BN}R_S)^2 + 4kT(R_S + R_T)} \quad (8)$$

Dividing this expression by the gain will give the equivalent input-referred spot-noise voltage at the noninverting input as shown by Equation 9.

$$E_N = \sqrt{E_{NI}^2 + (I_{BI}R_T)^2 + (I_{BN}R_S)^2 + 4kT(R_S + R_T)} \quad (9)$$

Evaluating these two equations for the VCA810 circuit and component values shown in Figure 30 (maximizing gain) will give a total output spot-noise voltage of 272.3nV√Hz and a total equivalent input-referred spot-noise voltage of 2.72nV√Hz. This total input-referred spot-noise voltage is higher than the 2.4nV√Hz specification for the VCA810 alone. This reflects the noise added to the output by the input current noise times the input resistance $R_S$ and $R_T$. Keeping input impedance low is required to maintain low total equivalent input-referred spot-noise voltage.

## THERMAL ANALYSIS

The VCA810 will not require heatsinking or airflow in most applications. Maximum desired junction temperature would set the maximum allowed internal power dissipation as described in this section. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature ($T_J$) is given by Equation 10:

$$T_J = T_A + P_D \times \theta_{JA} \quad (10)$$

The total internal power dissipation ($P_D$) is the sum of quiescent power ($P_{DQ}$) and additional power dissipated in the output stage ($P_{DL}$) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. $P_{DL}$ depends on the required output signal and load; for a grounded resistive load, however, it is at a maximum when the output is fixed at a voltage equal to one-half of either supply voltage (for equal bipolar supplies). Under this worst-case condition, $P_{DL} = V_S{}^2/(4 \bullet R_L)$, where $R_L$ is the resistive load.

Note that it is the power in the output stage and not in the load that determines internal power dissipation. As a worst-case example, compute the maximum $T_J$ using an VCA810ID (SO-8 package) in the circuit of Figure 30 operating at maximum gain and at the maximum specified ambient temperature of +85°C.

$P_D = 10V(24.8mA) + 5^2/(4 \bullet 500\Omega) = 260.5mW$

Maximum $T_J$ = +85°C + (0.260W ● +125°C/W) = 117.6°C

This maximum operating junction temperature is well below most system level targets. Most applications will be lower since an absolute worst-case output stage power was assumed in this calculation of $V_S/2$ which is beyond the output voltage range for the VCA810.

## BOARD LAYOUT

Achieving optimum performance with a high-frequency amplifier such as the VCA810 requires careful attention to board layout parasitic and external component types. Recommendations that will optimize performance include:

**a) Minimize parasitic capacitance** to any ac ground for all of the signal I/O pins. This includes the ground pin (pin 2). Parasitic capacitance on the output can cause instability: on both the inverting input and the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board. Place a small series resistance (> 25Ω) with the input pin connected to ground to help decouple package parasitic.

**b) Minimize the distance** (less than 0.25” or 6.35mm) from the power-supply pins to high-frequency 0.1μF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequencies, should also be used on the main supply pins. These capacitors may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

**c) Careful selection and placement** of external components will preserve the high-frequency performance of the VCA810. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Since the output pin is the most sensitive to parasitic capacitance, always position the series output resistor, if any, as close as possible to the output pin. Other network components, such as inverting or noninverting input termination resistors, should also be placed close to the package.

**d) Connections to other wideband devices** on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils, or 1.27mm to 2.54mm) should be used, preferably with ground and power planes opened up around them.

**e) Socketing a high-speed part like the VCA810 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the VCA810 onto the board.

## INPUT AND ESD PROTECTION

The VCA810 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table.

All pins on the VCA810 are internally protected from ESD by means of a pair of back-to-back, reverse-biased diodes to either power supply, as shown in Figure 49. These diodes begin to conduct when the pin voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To ensure long-term reliability, however, diode current should be externally limited to 10mA whenever possible.

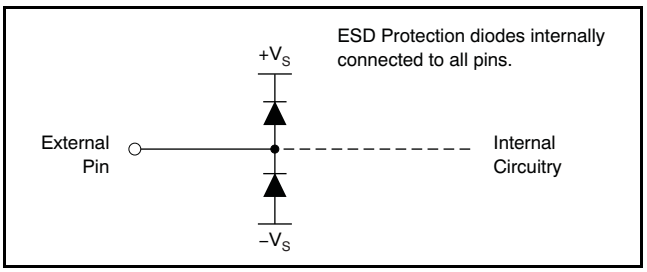



**Figure 49. Internal ESD Protection**

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision E (August, 2008) to Revision F** **Page**

- Updated document format to current standards ..... 1
- Deleted lead temperature specification from *Absolute Maximum Ratings* table ..... 2
- Corrected typo in Figure 30 ..... 11

**Changes from Revision D (February, 2006) to Revision E** **Page**

- Changed rails quantity from 100 to 75. ..... 2
- Changed storage temperature minimum value in *Absolute Maximum Ratings* table from –40°C to –65°C ..... 2

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VCA810AID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | VCA 810 A | Samples |
| VCA810AIDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | VCA 810 A | Samples |
| VCA810AIDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | VCA 810 A | Samples |
| VCA810ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | VCA 810 | Samples |
| VCA810IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | VCA 810 | Samples |
| VCA810IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | VCA 810 | Samples |
| VCA810IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | VCA 810 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

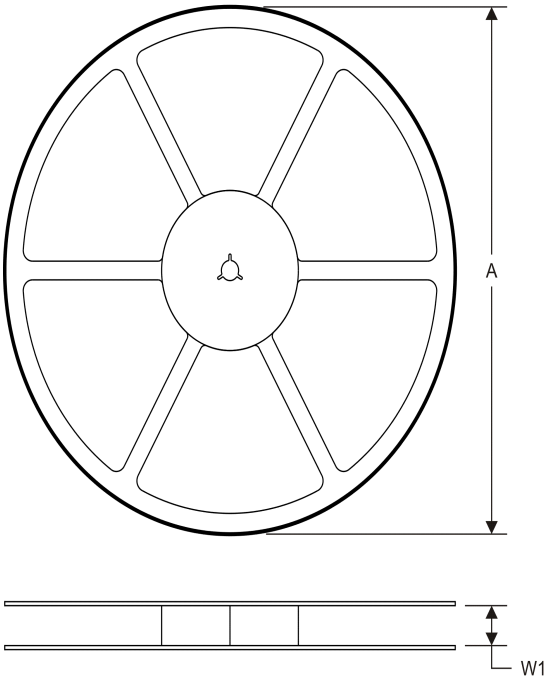
**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

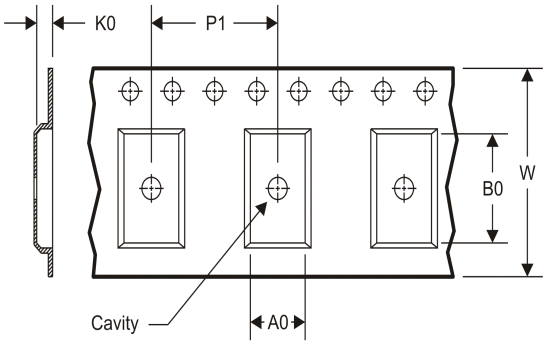
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



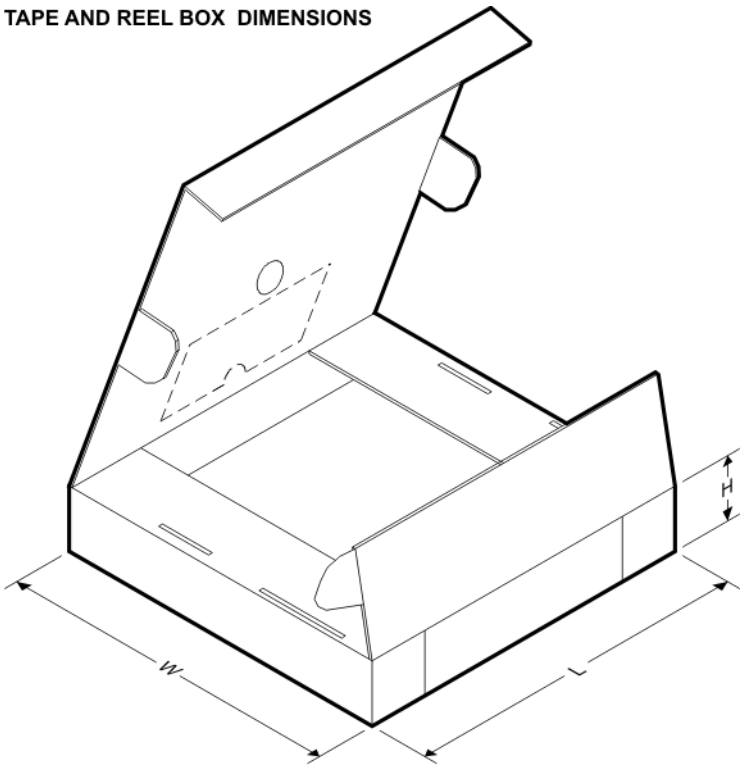

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VCA810AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| VCA810IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

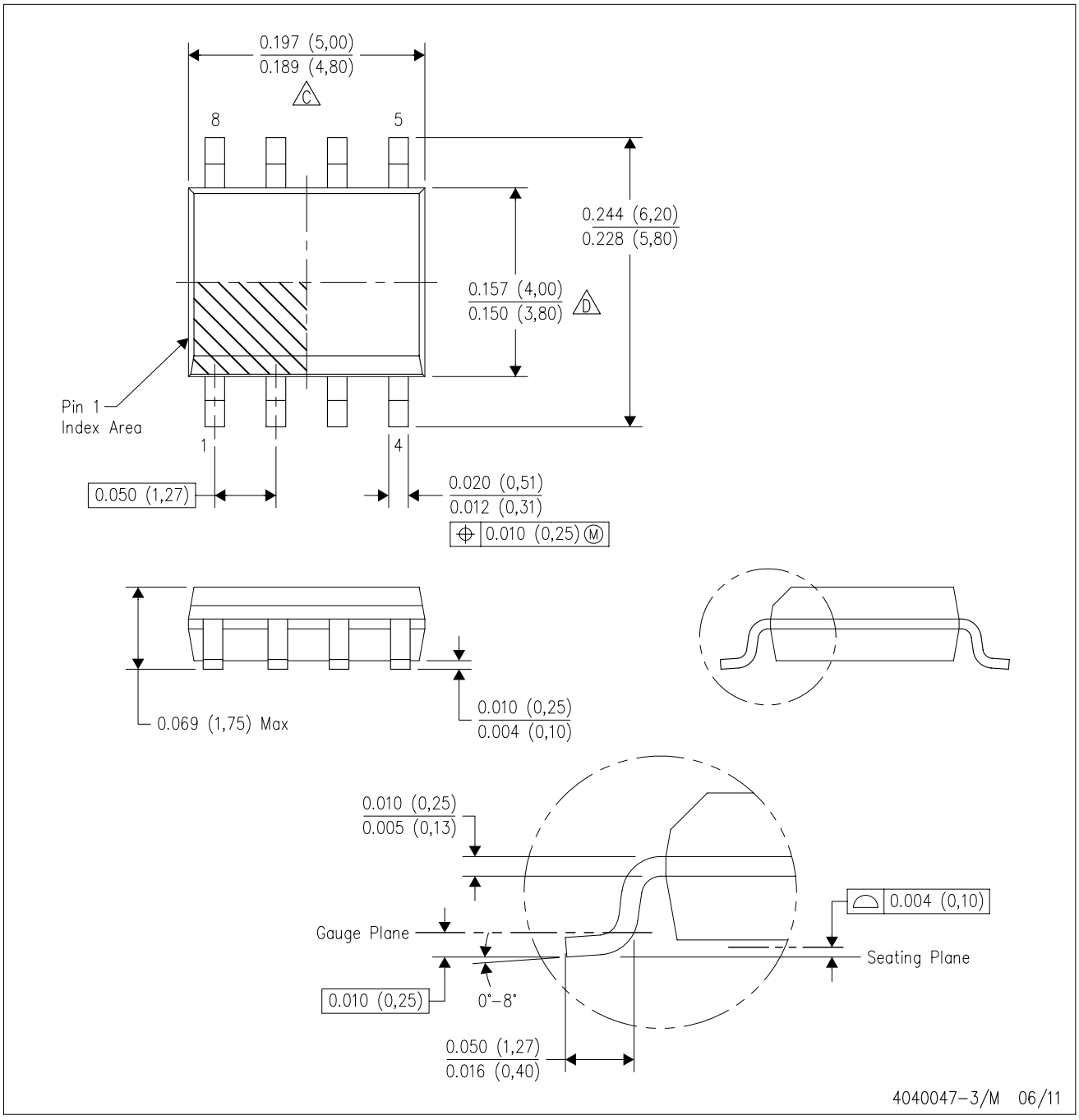
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

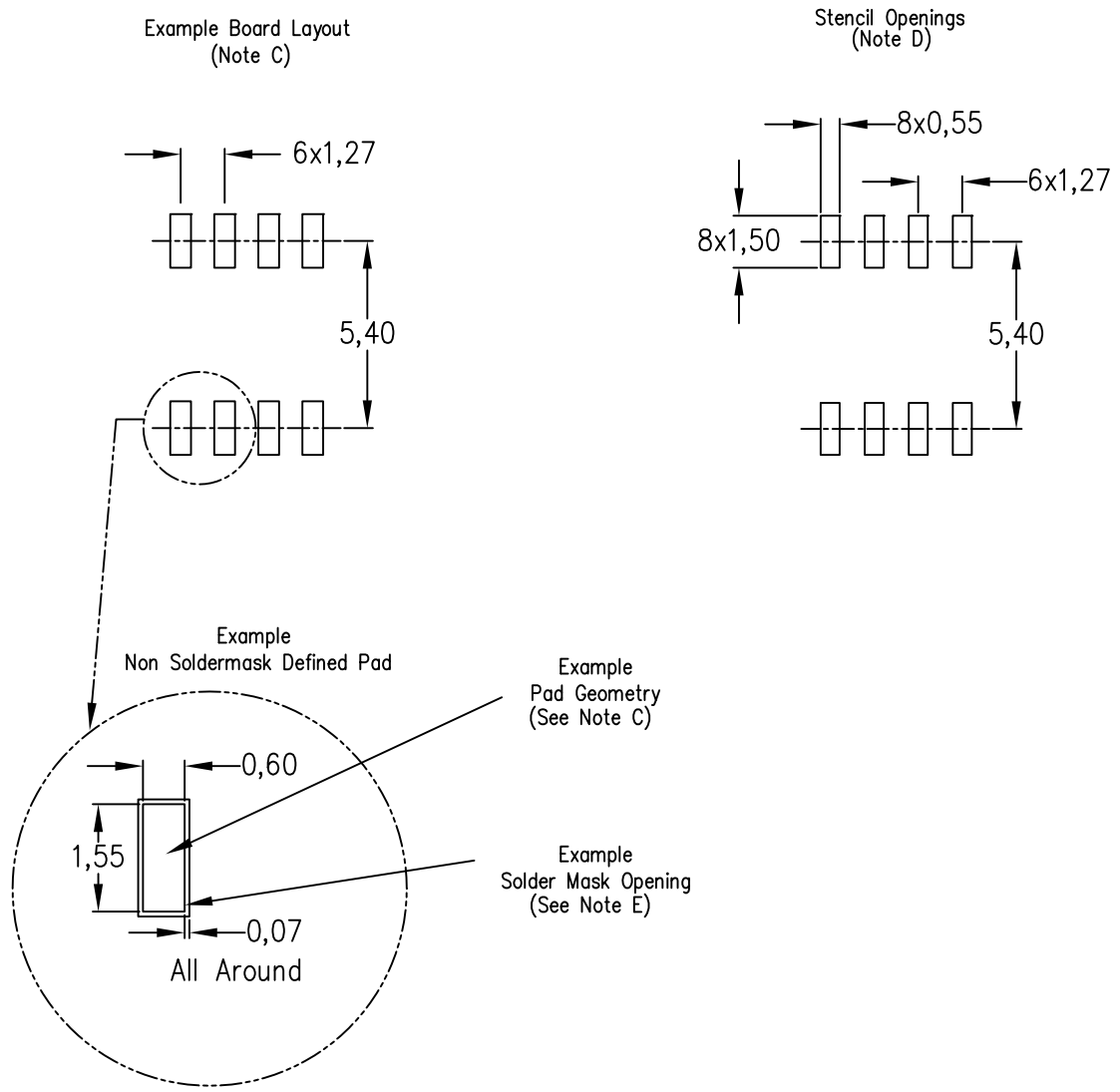
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| VCA810AIDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| VCA810IDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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