CMOS Digital Integrated Circuits Silicon Monolithic

74HC165D

1. Functional Description

- 8-Bit Shift Register (P-IN, S-OUT)

2. General

The 74HC165D is a high speed CMOS 8-BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It consists of parallel-in or serial-in, serial-out 8-bit shift register with a gated clock inputs. When the SHIFT/$\overline{\text{LOAD}}$ input is held high, the serial data input is enabled and the eight frip-frops perform serial shifting with each clock pulse.

When the SHIFT/$\overline{\text{LOAD}}$ input is held low, the parallel data is loaded synchronously into the register at positive going transition of the clock pulse.

The CK-INH input should be shifted high only when the CK input is held high.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

3. Features

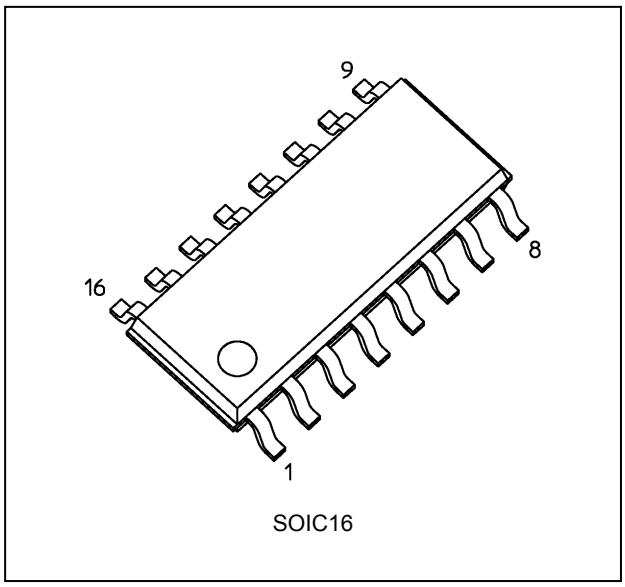
(1) High speed: f_{MAX} = 56 MHz (typ.) at V_{CC} = 5 V

(2) Low power dissipation: I_{CC} = 4.0 μA (max) at T_a = 25 °C

(3) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$

(4) Wide operating voltage range: $V_{CC(opr)}$ = 2.0 V to 6.0 V

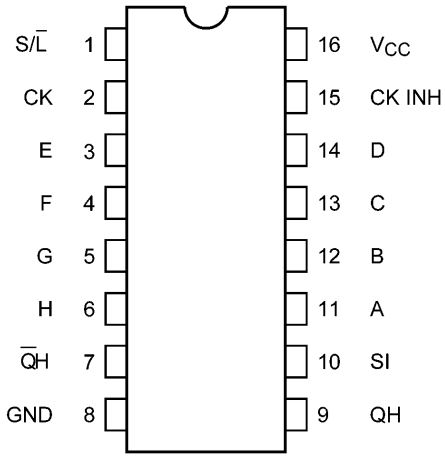
4. Packaging



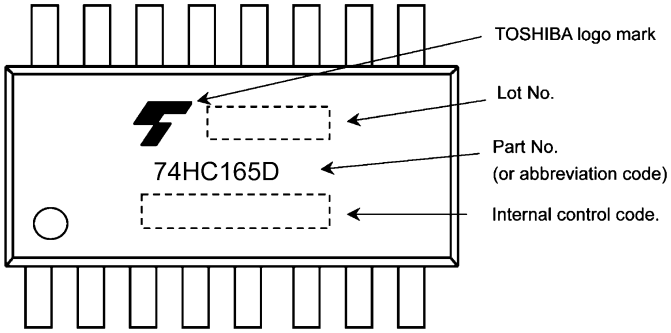
SOIC16

Start of commercial production
2016-05

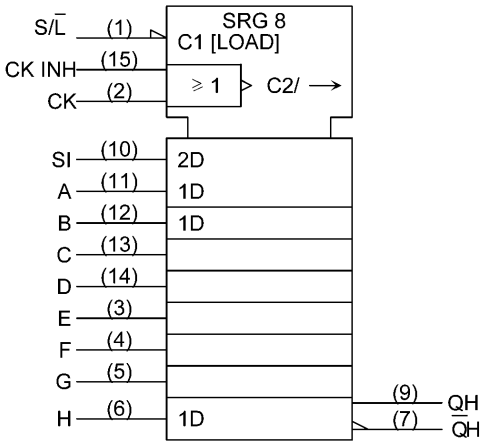
5. Pin Assignment



6. Marking



7. IEC Logic Symbol

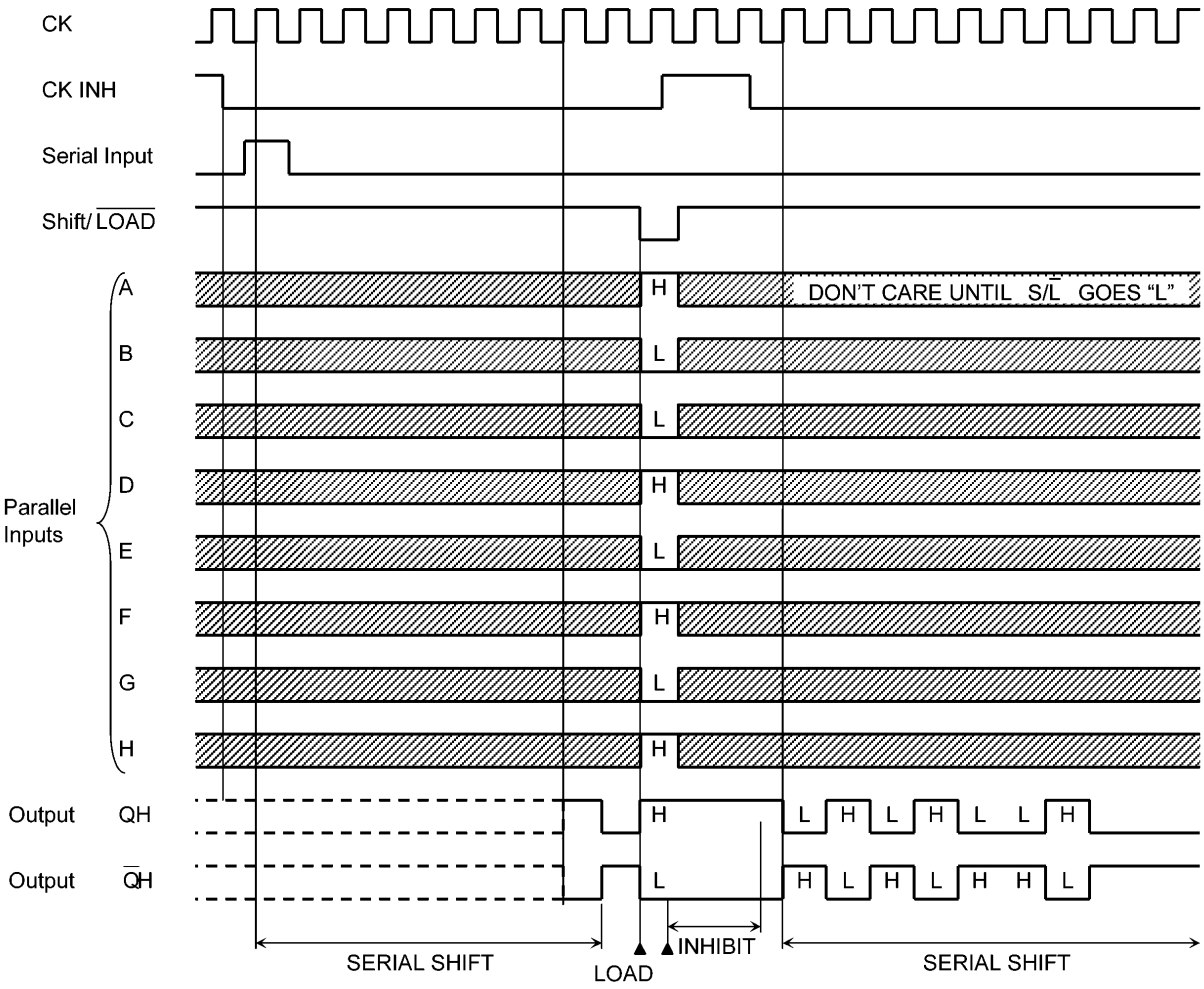


8. Truth Table

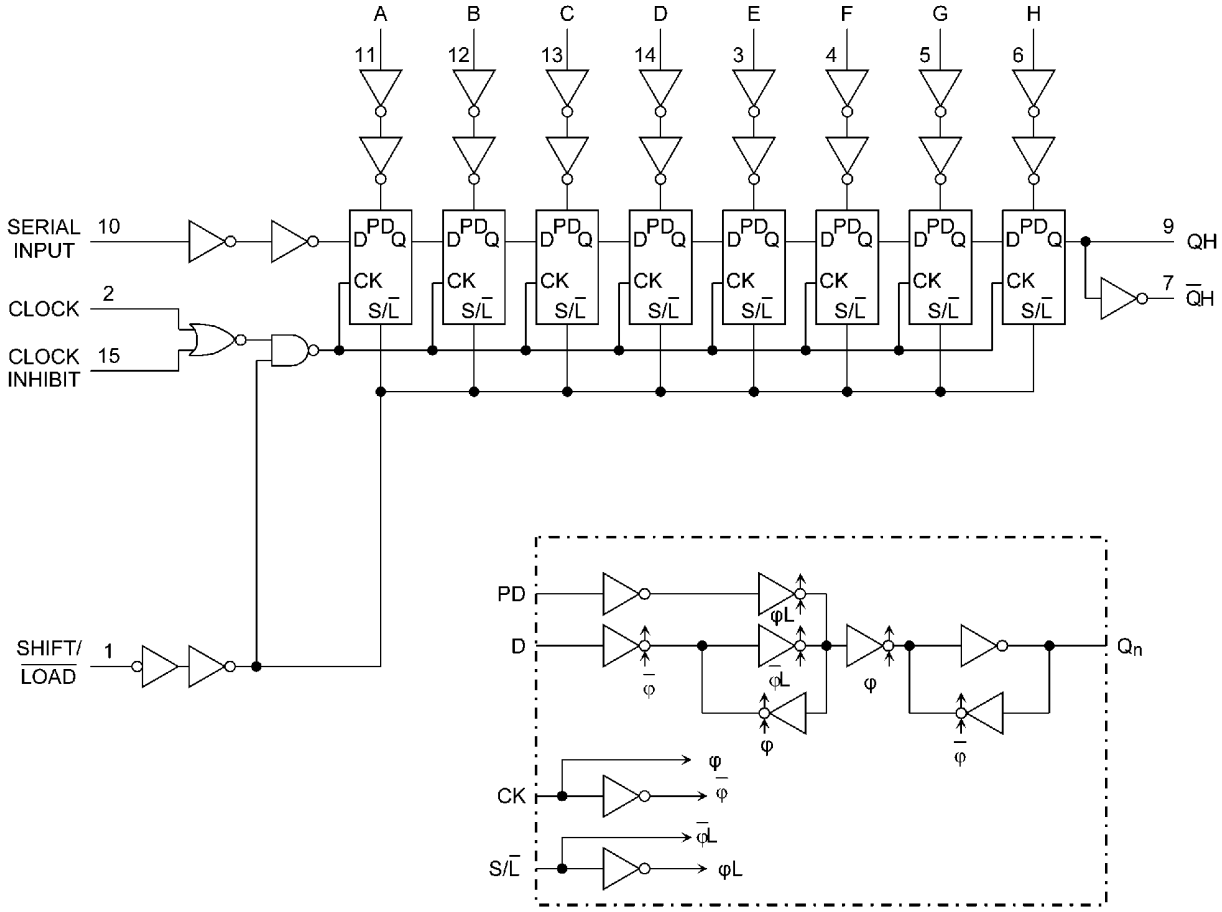
Inputs					Internal Outputs		Outputs	
SHIFT/$\overline{LOAD}$	CK INH	CK	SERIAL IN	PARALLEL A……H	QA	QB	QH	$\overline{QH}$
L	X	X	X	a……h	a	b	h	$\overline{h}$
H	L	↑	H	X	H	QAn	QGn	$\overline{QGn}$
H	L	↑	L	X	L	QAn	QGn	$\overline{QGn}$
H	↑	L	H	X	H	QAn	QGn	$\overline{QGn}$
H	↑	L	L	X	L	QAn	QGn	$\overline{QGn}$
H	X	H	X	X	No Change			
H	H	X	X	X	No Change			

X: Don't care
a.....h: The level of steady state input voltage at inputs A through H respectively.
QAn to QGn: The level of QA to QG, respectively, before the most recent positive transition of the CK.

9. Timing Diagrams



10. System Diagram



11. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		-0.5 to 7.0	V
Input voltage	V_{IN}		-0.5 to V_{CC} + 0.5	V
Output voltage	V_{OUT}		-0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}		±20	mA
Output diode current	I_{OK}		±20	mA
Output current	I_{OUT}		±25	mA
V_{CC}/ground current	I_{CC}		±50	mA
Power dissipation	P_D		500	mW
Storage temperature	T_{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

12. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	V_{CC}		2.0 to 6.0	V
Input voltage	V_{IN}		0 to V_{CC}	V
Output voltage	V_{OUT}		0 to V_{CC}	V
Operating temperature	T_{opr}		-40 to 85	°C
Input rise and fall times	t_r,t_f	V_{CC} = 2.0 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6.0 V	0 to 400	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

13. Electrical Characteristics

13.1. DC Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Typ.	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	V
				4.5	3.15	—	—	
				6.0	4.20	—	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	V
				4.5	—	—	1.35	
				6.0	—	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20 μA	2.0	1.9	2.0	—	V
				4.5	4.4	4.5	—	
				6.0	5.9	6.0	—	
			I_{OH} = -4 mA	4.5	4.18	4.31	—	
			I_{OH} = -5.2 mA	6.0	5.68	5.80	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.0	0.1	V
				4.5	—	0.0	0.1	
				6.0	—	0.0	0.1	
			I_{OL} = 4 mA	4.5	—	0.17	0.26	
			I_{OL} = 5.2 mA	6.0	—	0.18	0.26	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	4.0	μA

13.2. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	V
				4.5	3.15	—	
				6.0	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	0.50	V
				4.5	—	1.35	
				6.0	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20 μA	2.0	1.9	—	V
				4.5	4.4	—	
				6.0	5.9	—	
			I_{OH} = -4 mA	4.5	4.13	—	
			I_{OH} = -5.2 mA	6.0	5.63	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.1	V
				4.5	—	0.1	
				6.0	—	0.1	
			I_{OL} = 4 mA	4.5	—	0.33	
			I_{OL} = 5.2 mA	6.0	—	0.33	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	40.0	μA

13.3. Timing Requirements (Unless otherwise specified, T_a = 25 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Limit	Unit
Minimum pulse width (CK, CK INH)	$t_{w(L)}$,$t_{w(H)}$	—	2.0	75	ns
			4.5	15	
			6.0	13	
Minimum pulse width ($S/\overline{L}$)	$t_{w(L)}$	—	2.0	75	ns
			4.5	15	
			6.0	13	
Minimum setup time (PI-$S/\overline{L}$)	t_S	—	2.0	75	ns
			4.5	15	
			6.0	13	
Minimum setup time (SI-CK, CK INH)	t_S	—	2.0	75	ns
			4.5	15	
			6.0	13	
Minimum setup time ($S/\overline{L}$-CK, CK INH)	t_S	—	2.0	75	ns
			4.5	15	
			6.0	13	
Minimum hold time (PI-$S/\overline{L}$)	t_h	—	2.0	0	ns
			4.5	0	
			6.0	0	
Minimum hold time (SI-CK, CK INH)	t_h	—	2.0	0	ns
			4.5	0	
			6.0	0	
Minimum hold time ($S/\overline{L}$-CK, CK INH)	t_h	—	2.0	0	ns
			4.5	0	
			6.0	0	
Minimum removal time (CK INH-CK), (CK-CK INH)	t_{rem}	—	2.0	75	ns
			4.5	15	
			6.0	13	
Clock frequency	f	—	2.0	7	MHz
			4.5	30	
			6.0	41	

13.4. Timing Requirements (Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Limit	Unit
Minimum pulse width (CK, CK INH)	$t_{w(L)}$,$t_{w(H)}$	—	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum pulse width ($S/\overline{L}$)	$t_{w(L)}$	—	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum setup time (PI-$S/\overline{L}$)	t_s	—	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum setup time (SI-CK, CK INH)	t_s	—	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum setup time ($S/\overline{L}$-CK, CK INH)	t_s	—	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum hold time (PI-$S/\overline{L}$)	t_h	—	2.0	0	ns
			4.5	0	
			6.0	0	
Minimum hold time (SI-CK, CK INH)	t_h	—	2.0	0	ns
			4.5	0	
			6.0	0	
Minimum hold time ($S/\overline{L}$-CK, CK INH)	t_h	—	2.0	0	ns
			4.5	0	
			6.0	0	
Minimum removal time (CK INH-CK), (CK-CK INH)	t_{rem}	—	2.0	95	ns
			4.5	19	
			6.0	16	
Clock frequency	f	—	2.0	6	MHz
			4.5	24	
			6.0	28	

13.5. AC Characteristics (Unless otherwise specified, C_L = 15 pF, V_{CC} = 5 V, T_a = 25 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Note	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH},t_{THL}		—	—	4	8	ns
Propagation delay time (CK, CK INH-QH, $\overline{Q}$H)	t_{PLH},t_{PHL}		—	—	15	25	ns
Propagation delay time (S/$\overline{L}$-QH, $\overline{Q}$H)	t_{PLH},t_{PHL}		—	—	15	25	ns
Propagation delay time (H-QH, $\overline{Q}$H)	t_{PLH},t_{PHL}		—	—	14	26	ns
Maximum clock frequency	f_{MAX}		—	35	56	—	MHz

13.6. AC Characteristics (Unless otherwise specified, C_L = 50 pF, T_a = 25 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit
Output transition time	t_{TLH},t_{THL}		—	2.0	—	25	75	ns
				4.5	—	8	15	
				6.0	—	7	13	
Propagation delay time (CK, CK INH-QH, $\overline{Q}$H)	t_{PLH},t_{PHL}		—	2.0	—	55	150	ns
				4.5	—	18	30	
				6.0	—	15	26	
Propagation delay time (S/$\overline{L}$-QH, $\overline{Q}$H)	t_{PLH},t_{PHL}		—	2.0	—	60	165	ns
				4.5	—	19	33	
				6.0	—	16	28	
Propagation delay time (H-QH, $\overline{Q}$H)	t_{PLH},t_{PHL}		—	2.0	—	52	135	ns
				4.5	—	17	27	
				6.0	—	14	23	
Maximum clock frequency	f_{MAX}		—	2.0	7	14	—	MHz
				4.5	30	46	—	
				6.0	41	65	—	
Input capacitance	C_{IN}		—		—	5	10	pF
Power dissipation capacitance	C_{PD}	(Note 1)	—		—	55	—	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

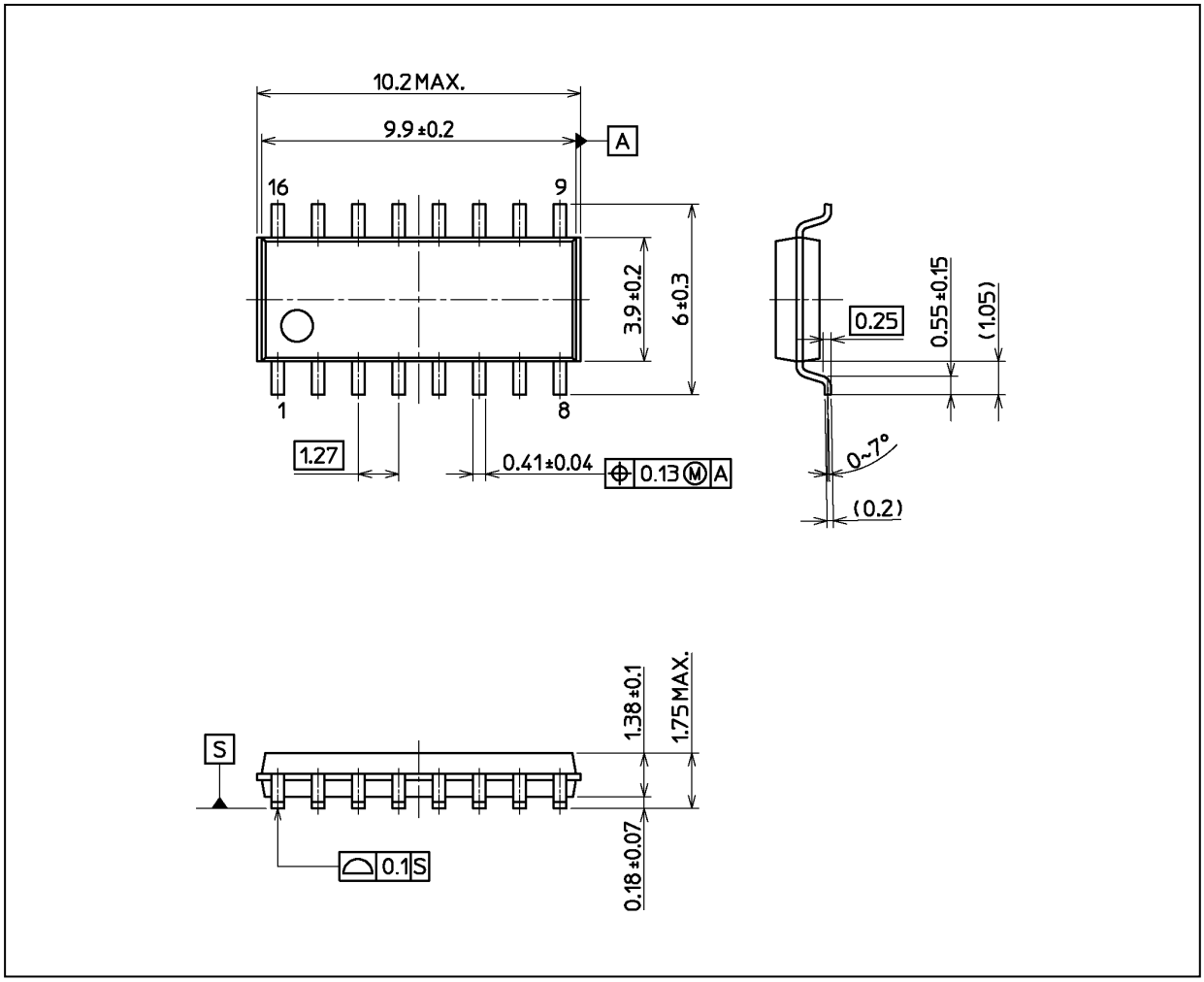
$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

13.7. AC Characteristics
(Unless otherwise specified, C_L = 50 pF, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Output transition time	t_{TLH},t_{THL}	—	2.0	—	95	ns
			4.5	—	19	
			6.0	—	16	
Propagation delay time (CK, CK INH-QH, $\overline{QH}$)	t_{PLH},t_{PHL}	—	2.0	—	190	ns
			4.5	—	38	
			6.0	—	33	
Propagation delay time ($S/\overline{L}$-QH, $\overline{QH}$)	t_{PLH},t_{PHL}	—	2.0	—	205	ns
			4.5	—	41	
			6.0	—	35	
Propagation delay time (H-QH, $\overline{QH}$)	t_{PLH},t_{PHL}	—	2.0	—	170	ns
			4.5	—	34	
			6.0	—	29	
Maximum clock frequency	f_{MAX}	—	2.0	6	—	MHz
			4.5	24	—	
			6.0	28	—	
Input capacitance	C_{IN}	—		—	10	pF

Package Dimensions

Unit: mm



Weight: 0.15 g (typ.)

Package Name(s)
Nickname: SOIC16

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