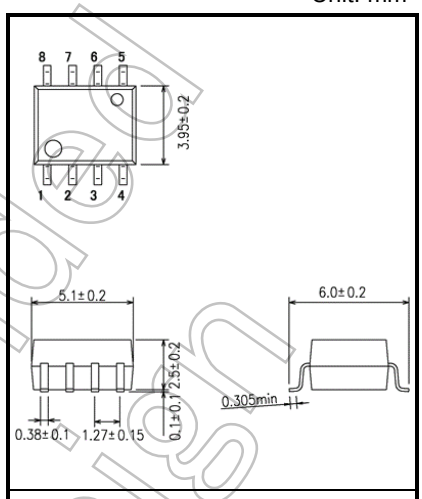
TOSHIBA PHOTOCOUPLER IRED & PHOTO-IC

TLP2116

○ Plasma Display Panels (PDP)
○ High-Speed Interfaces
○ Factory Automation (FA)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	11−5K1S

Weight: 0.11 g (typ.)

The TOSHIBA TLP2116 dual photocoupler consists of a pair of an infrared emitting diodes optically coupled to integrated high gain and high-speed photodetectors.

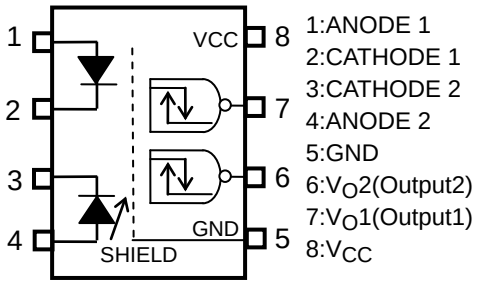
- Inverter logic (totem-pole output)
- Package: SO8
- Guaranteed performance over temperature : -40 to 100°C
- Power supply voltage: 4.5 to 5.5 V
- Input thresholds current: I_{FHL} = 5 mA (max)
- Propagation delay time (tpHL/tpLH): 75 ns (max)
- Switching speed: 15 MBd (typ.) (NRZ)
- Common mode transient immunity: ±10 kV/μs
- Isolation voltage: 2500 Vrms
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A
  File No.E67349
- VDE-approved: EN 60747-5-5 (Note 1)

Note 1 : When a VDE approved type is needed,
Please designate the **Option(V4)**.

Truth Table

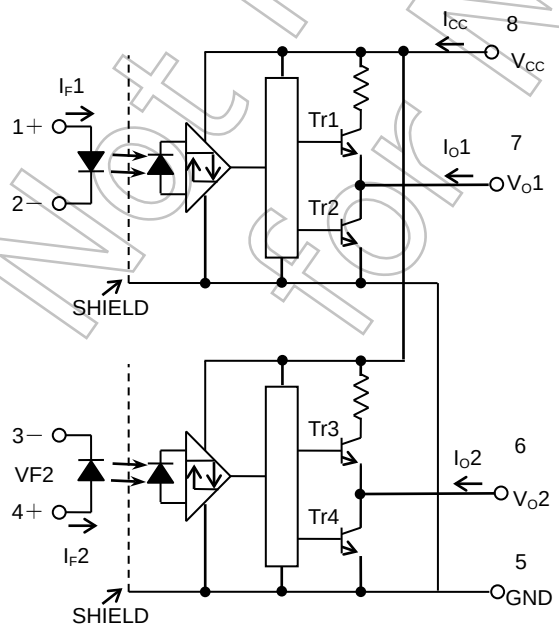
Input	LED1(2)	Tr1(3)	Tr2(4)	Output 1(2)
H	ON	OFF	ON	L
L	OFF	ON	OFF	H

Pin Configuration (Top View)



1:ANODE 1
2:CATHODE 1
3:CATHODE 2
4:ANODE 2
5:GND
6:V_O2(Output2)
7:V_O1(Output1)
8:V_{CC}

Schematic



A bypass capacitor of 0.1 μF must be connected between pins 8 and 5.

Start of commercial production
2008-02

Absolute Maximum Ratings (Ta=25°C)

Characteristic			Symbol	Rating	Unit
LED	Forward current	(Each Channel)	I_F	20	mA
	Forward current derating (Ta ≥ 85°C)	(Each Channel)	$\Delta I_F/\Delta Ta$	-0.5	mA/°C
	Peak transient forward current	(Each Channel) (Note 1)	I_{FPT}	1	A
	Reverse voltage	(Each Channel)	V_R	5	V
	Input Power Dissipation	(Each Channel)	P_D	40	mW
	Input Power Dissipation Derating (Ta≥85°C)	(Each Channel)	$\Delta P_D/°C$	-1.0	mW/°C
DETECTOR	Output current	(Each Channel)	I_O	10	mA
	Output voltage	(Each Channel)	V_O	6	V
	Supply voltage		V_{CC}	6	V
	Output power dissipation (Each Channel)		P_O	40	mW
	Output Power Dissipation Derating (Ta ≥ 85°C)	(Each Channel)	$\Delta PO/°C$	-1.0	mW/°C
Operating temperature range			T_{opr}	-40 to 100	°C
Storage temperature range			T_{stg}	-55 to 125	°C
Lead solder temperature		(10 s)	T_{sol}	260	°C
Isolation voltage (AC,60 s, R.H. ≤ 60 %,)		(Note 2)	BV_S	2500	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width PW ≤ 1 μs, 300 pps.

Note 2: This device is regarded as a two terminal device: pins 1, 2, 3 and 4 are shorted together, as are pins 5, 6, 7 and 8.

Recommended Operating Conditions

Characteristic		Symbol	Min	Typ.	Max	Unit
Input current, ON	(Each Channel)	$I_{F(ON)}$	8	—	18	mA
Input voltage, OFF	(Each Channel)	$V_{F(OFF)}$	0	—	0.8	V
Supply voltage(*)	(Note 3)	V_{CC}	4.5	5.0	5.5	V
Operating temperature		T_{opr}	-40	—	100	°C

(*) This item denotes operating ranges, not meaning of recommended operating conditions.

Note 3: The detector of this product requires power supply voltage (V_{CC}) of 4.5 V or higher for stable operation.
If the V_{CC} is lower than this value, I_{CCH} may increase, or output may be unstable.
Be sure to use the product after checking the supply current, and the operation of a power-on/-off.

Note: A ceramic capacitor (0.1 μF) should be connected from pin 8 (V_{CC}) to pin 5 (GND) to stabilize the operation of the high gain linear amplifier. Failure to provide the bypass may impair the switching property.
The total lead length between capacitor and coupler should not exceed 1 cm.

Electrical Characteristics
(Unless otherwise specified, Ta = -40 to 100°C, V_{CC} = 4.5 to 5.5V)

Characteristic		Symbol	Conditions	Min	Typ.	Max	Unit
Input forward voltage	(Each Channel)	V_F	I_F = 10 mA, Ta = 25 °C	1.3	1.65	1.75	V
Temperature coefficient of forward voltage	(Each Channel)	$\Delta V_F/\Delta Ta$	I_F = 10 mA	—	-2.0	—	mV/°C
Input reverse current	(Each Channel)	I_R	V_R = 5 V, Ta = 25 °C	—	—	10	μA
Input capacitance	(Each Channel)	C_T	V = 0 V, f = 1 MHz, Ta = 25 °C	—	45	—	pF
Logic low output voltage	(Each Channel)	V_{OL}	I_{OL} = 1.6 mA, I_F = 12 mA, V_{CC} = 5 V	—	—	0.4	V
Logic high output voltage	(Each Channel)	V_{OH}	I_{OH} = -0.02 mA, V_F = 1.05 V V_{CC} = 5 V	4.0	—	—	V
Logic low supply current		I_{CCL}	I_F = 12 mA	—	—	10.0	mA
Logic high supply current		I_{CCH}	V_F = 0 V (Note 3)	—	—	10.0	mA
Input current logic low output	(Each Channel)	I_{FHL}	I_O =1.6 mA, V_O < 0.4 V	—	—	5	mA
Input voltage logic high output	(Each Channel)	V_{FLH}	I_O = -0.02 mA, V_O > 4.0 V	0.8	—	—	V

*All typical values are at Ta=25°C, V_{CC}=5 V unless otherwise specified

Isolation Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit
Capacitance input to output	C_S	V_S = 0 V, f = 1 MHz (Note 2)	—	0.8	—	pF
Isolation resistance	R_S	R.H. ≤ 60 %, V_S = 500 V (Note 2)	1×10^{12}	10^{14}	—	Ω
Isolation voltage	BV_S	AC, 60 s (Note 2)	2500	—	—	Vrms

Switching Characteristics
(Unless otherwise specified, Ta = -40 to 100°C, V_{CC} = 4.5 to 5.5V)(Each Channel)

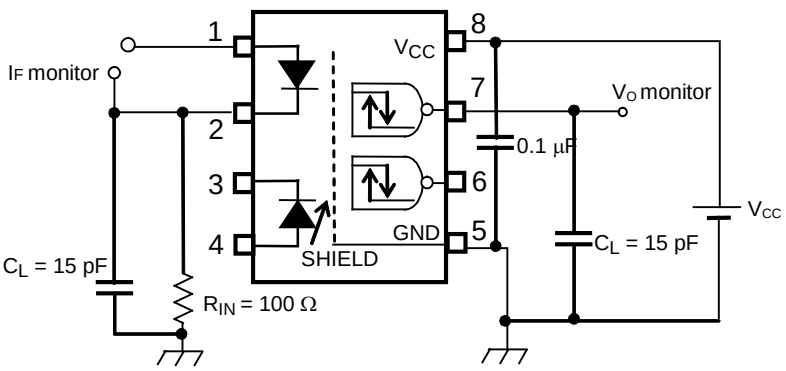
Characteristic	Symbol	Test Circuit	Conditions		Min	Typ.	Max	Unit
Propagation delay time to logic low output	t_{pHL}	1	I_F = 0→12 mA	R_{IN} = 100 Ω, C_L = 15 pF (Note 5)	—	—	75	ns
Propagation delay time to logic high output	t_{pLH}		I_F = 12→0 mA		—	—	75	ns
Propagation delay time to logic low output	t_{pHL}	2	V_{IN} = 0→5 V (I_F = 0→8 mA)	R_{IN} = 430 Ω, C_{IN} = 27 pF, C_L = 15 pF (Note 5)	—	—	75	ns
Propagation delay time to logic high output	t_{pLH}		V_{IN} = 5→0 V (I_F = 8→0 mA)		—	—	75	ns
Switching time dispersion between ON and OFF	$\lvert t_{pHL} - t_{pLH} \rvert$	1	I_F = 12 mA, R_{IN} =100 Ω, C_L =15 pF (Note 5)		—	—	30	ns
Output fall time (90 - 10%)	t_f		I_F = 0→12 mA	R_{IN} =100 Ω, C_L =15 pF (Note 5)	—	15	—	ns
Output rise time (10 - 90%)	t_r		I_F = 12→0 mA		—	15	—	ns
Common mode transient immunity at high level output	CM_H	3	VC_M =1000 Vp-p , I_F = 0 mA, V_O (min) = 4 V , Ta = 25 °C		10000	—	—	V/μs
Common mode transient immunity at low level output	CM_L		VC_M = 1000 Vp-p , I_F = 12 mA, V_O (max) = 0.4 V , Ta = 25 °C		-10000	—	—	V/μs

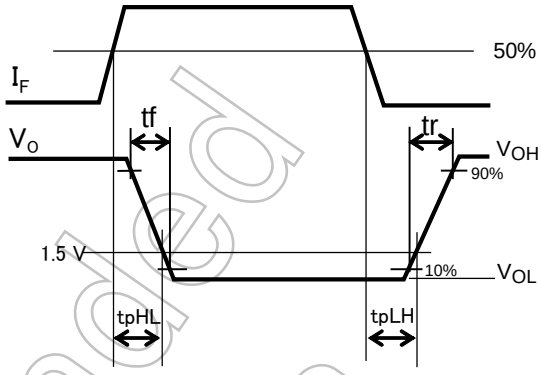
*All typical values are at Ta = 25 °C

Note 5: C_L is approximately 15 pF which includes probe and Jig/stray wiring capacitance.

Test Circuit 1: Switching Time Test Circuit

I_F=12 mA (P.G)
(f=5 MHz, duty=50%,
less than $t_r = t_f$= 5 ns)

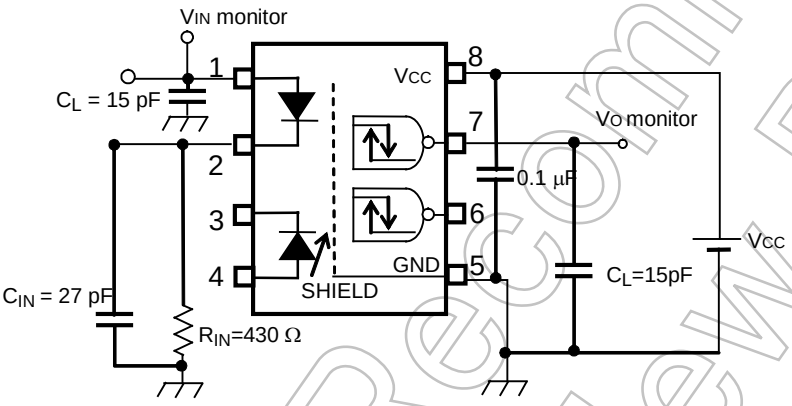


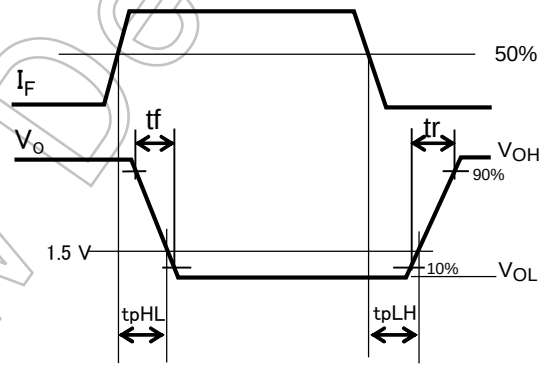


C_L is capacitance of the probe and JIG.
(P.G): Pulse Generator

Test Circuit 2: Switching Time Test Circuit

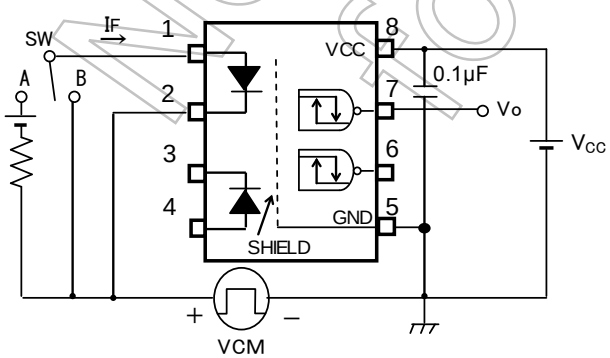
V_{IN}=5V (P.G)
(f=5 MHz, duty=50%,
less than $t_r = t_f$= 5 ns)

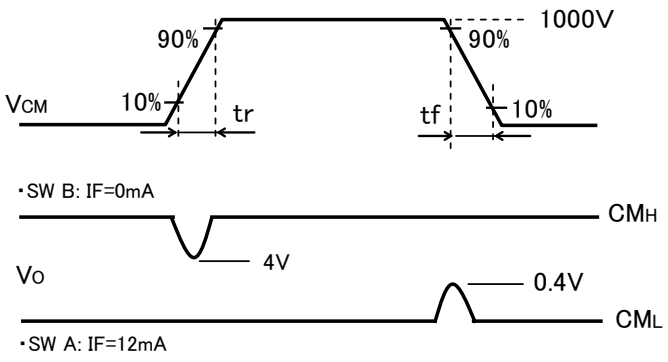




C_L is capacitance of the probe and JIG.
(P.G): Pulse Generator

Test Circuit 3: Common-Mode Transient Immunity Test Circuit





$$CM_H = \frac{800(V)}{tr(\mu s)} \qquad CM_L = -\frac{800(V)}{tf(\mu s)}$$

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