8V to 36Vin Cool-Power® ZVS Buck Regulator Family

Description

The PI33XX is a family of high efficiency, wide input range DC-DC ZVS-Buck regulators integrating controller, power switches, and support components all within a high density System-in-Package (SiP). The integration of a high performance Zero-Voltage Switching (ZVS) topology, within the PI33XX series, increases point of load performance providing best in class power efficiency. The PI33XX requires only an external inductor and minimal capacitors to form a complete DC-DC switching mode buck regulator.

Device	Output Voltage		Iout Max
	Set	Range	
PI3311-X0-LGIZ	1.0V	1.00 to 1.4	10A
PI3312-X0-LGIZ	2.5V	2.0 to 3.1	10A
PI3301-X0-LGIZ	3.3V	2.3 to 4.1	10A
PI3302-X0-LGIZ	5.0V	3.3 to 6.5	10A
PI3303-X0-LGIZ	12V	6.5 to 13.0	8A
PI3305-X0-LGIZ	15V	10.0 to 16.0	8A

Table 1 *- PI33XX Portfolio. Additional versions available for higher 18A current, output voltages (Vout) of 1.5 to 1.9V, and Vout >15.*

The Zero Voltage Switching (ZVS) architecture also enables high frequency operation while minimizing switching losses and maximizing efficiency. The high switching frequency operation reduces the size of the external filtering components, improves power density, and enables very fast dynamic response to line and load transients. The PI33XX series sustains high switching frequency all the way up to the rated input voltage without sacrificing efficiency and, with its 20ns minimum on-time, supports large step down conversions up to 36Vin.

Features

- High efficiency up to 98%
- ZVS-Buck Topology
- Wide input voltage range of 8V to 36V
- Very-Fast transient response
- High accuracy pre-trimmed output voltage
- User adjustable soft-start & tracking
- Power-up into pre-biased load (select versions)
- Parallel capable with single wire current sharing
- Input Over/Under Voltage Lockout (OVLO/UVLO)
- Output Overvoltage Protection (OVP)
- Over Temperature Protection (OTP)
- Fast and slow current limits
- -40°C to 125°C operating range (T_J)
- Optional I^2C functionality & programmability:
    - Vout margining
    - Fault reporting
    - Enable and SYNCI pin polarity
    - Phase delay (for interleaving multiple regulators)

Applications

- High efficiency systems
- Computing, Communications, Industrial, Automotive Equipment
- High voltage battery operation

Package Information

- 10mm x 14mm x 2.6mm LGA SiP

I^2C is a trademark of NXP Semiconductors

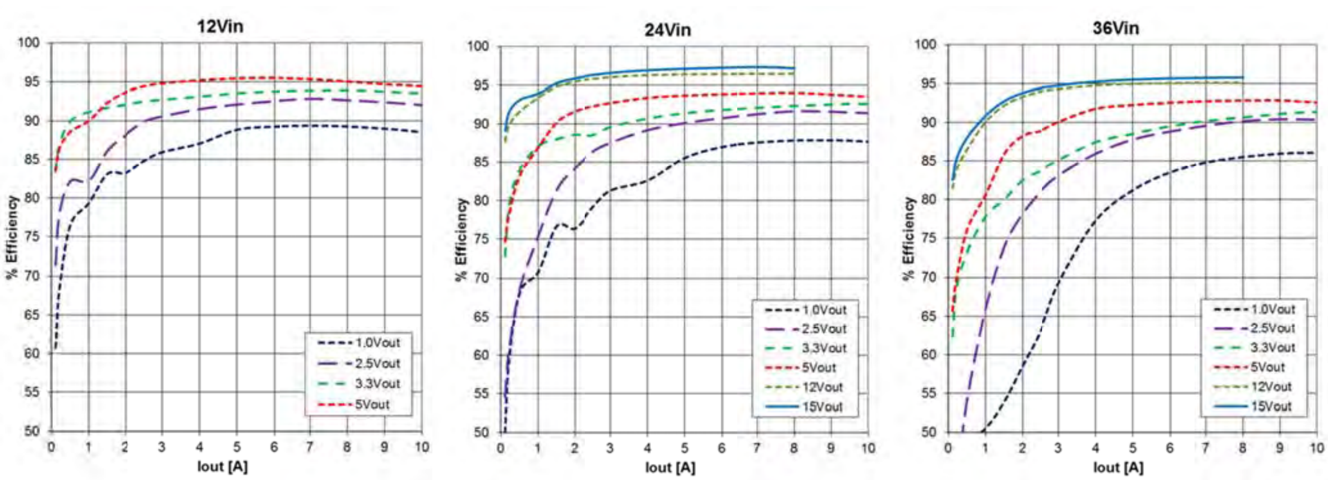
Contents

Order Information

Cool-Power	Output Range		Iout Max	Package	Transport Media
	Set	Range			
PI3311-00-LGIZ	1.0V	1.00 to 1.4V	10A	10mm x 14mm 123-pin LGA	TRAY
PI3312-00-LGIZ	2.5V	2.0V to 3.1V	10A	10mm x 14mm 123-pin LGA	TRAY
PI3301-00-LGIZ	3.3V	2.3 to 4.1V	10A	10mm x 14mm 123-pin LGA	TRAY
PI3302-00-LGIZ	5.0V	3.3 to 6.5V	10A	10mm x 14mm 123-pin LGA	TRAY
PI3303-00-LGIZ	12V	6.5 to 13.0V	8A	10mm x 14mm 123-pin LGA	TRAY
PI3305-00-LGIZ	15V	10.0 to 16.0V	8A	10mm x 14mm 123-pin LGA	TRAY
Higher Current Versions*					
PI3311-01-LGIZ	1.0V	1.0 to 1.4V	18A	10mm x 14mm 123-pin LGA	TRAY
PI3312-01-LGIZ	2.5V	2.0 to 3.1V	18A	10mm x 14mm 123-pin LGA	TRAY
PI3301-01-LGIZ	3.3V	2.3 to 4.1V	18A	10mm x 14mm 123-pin LGA	TRAY
I^2C Functionality & Programmability*					
PI3311-20-LGIZ	1.0V	1.0 to 1.4V	10A	10mm x 14mm 123-pin LGA	TRAY
PI3312-20-LGIZ	2.5V	2.0 to 3.1V	10A	10mm x 14mm 123-pin LGA	TRAY
PI3301-20-LGIZ	3.3V	2.3 to 4.1V	10A	10mm x 14mm 123-pin LGA	TRAY
PI3302-20-LGIZ	5.0V	3.30 to 6.5V	10A	10mm x 14mm 123-pin LGA	TRAY
PI3303-20-LGIZ	12V	6.5 to 13.0V	8A	10mm x 14mm 123-pin LGA	TRAY
PI3305-20-LGIZ	15V	10.0 to 16.0V	8A	10mm x 14mm 123-pin LGA	TRAY
PI3311-21-LGIZ	1.0V	1.0 to 1.4V	18A	10mm x 14mm 123-pin LGA	TRAY
PI3312-21-LGIZ	2.5V	2.0 to 3.1V	18A	10mm x 14mm 123-pin LGA	TRAY
PI3301-21-LGIZ	3.3V	2.3 to 4.1V	18A	10mm x 14mm 123-pin LGA	TRAY

*Please contact Picor for availability

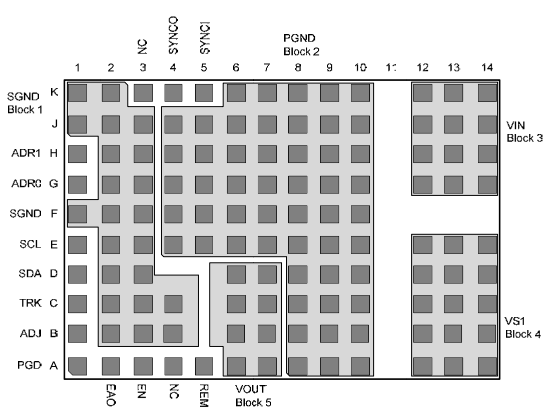
PI33XX Efficiency



Pin Description

Name	Number	Description
SGND	Block 1	**Signal ground:** Internal logic ground for EA, TRK, SYNCI, SYNCO, ADJ and I^2C (options) communication returns. SGND and PGND are star connected within the regulator package.
PGND	Block 2	**Power ground:** VIN and VOUT power returns
VIN	Block 3	**Input voltage:** and sense for UVLO, OVLO and feed forward ramp
VOUT	Block 5	**Output voltage:** and sense for power switches and feed-forward ramp
VS1	Block 4	**Switching node:** and ZVS sense for power switches
PGD	A1	**Parallel Good:** Used for parallel timing management intended for lead regulator.
EAO	A2	**Error amp output:** External connection for additional compensation and current sharing.
EN	A3	**Enable Input:** Regulator enable control. Asserted high or left floating – regulator enabled; Asserted low, regulator output disabled. Polarity is programmable via I^2C interface.
REM	A5	**Remote Sense:** High side connection. Connect to output regulation point.
ADJ	B1	**Adjust input:** An external resistor may be connected between ADJ pin and SGND or VOUT to trim the output voltage up or down.
TRK	C1	**Soft-start and track input:** An external capacitor may be connected between TRK pin and SGND to decrease the rate of rise during soft-start.
NC	K3, A4	**No Connect:** Leave pins floating.
SYNCO	K4	**Synchronization output:** Outputs a low signal for ½ of the minimum period for synchronization of other converters.
SYNCI	K5	**Synchronization input:** Synchronize to the falling edge of external clock frequency. SYNCI is a high impedance digital input node and should always be connected to SGND when not in use.
SDA	D1	**Data Line:** Connect to SGND for PI33XX-10 and -11. For use with PI33XX-20 and -21 only.
SCL	E1	**Clock Line:** Connect to SGND for PI33XX-10 and -11. For use with PI33XX-20 and -21 only.
ADR1	H1	**Tri-state Address** : No connect for PI33XX-10 and -11. For use with PI33XX-20 and -21 only.
ADR0	G1	**Tri-state Address** : No connect for PI33XX-10 and -11. For use with PI33XX-20 and -21 only.

Package Pin-Out



123-Lead LGA (10mm x 14mm)
Top view
T_{Jmax} = 125 °C, θ_{JA} = 22 °C/W

Block 1: B2-4, C2-4, D2-3, E2-3, F1-3, G2-3, H2-3, J1-3, K1-2

Block 2: A8-10, B8-10, C8-10, D8-10, E4-10, F4-10, G4-10, H4-10, J4-10, K6-10

Block 3: G12-14, H12-14, J12-14, K12-14

Block 4: A12-14, B12-14, C12-14, D12-14, E12-14,

Block 5: A6-7, B6-7, C6-7, D6-7

Absolute Maximum Ratings at 25°C

Note: All voltage nodes are referenced to PGND

VIN	-0.7V to 36V / 18A DC
VS1	-0.7 to 36V, -4V for 5ns
VOUT	See relevant product section
SGND	100mA
PGD, SYNCO, SYNCI, EN, EAO, ADJ, TRK, ADR1, ADR2, SCL, SDA	-0.3V to 5.5V / 5mA
Storage Temperature	-65°C to 150°C
Operating Junction Temperature	-40°C to 140°C
Soldering Temperature for 20 seconds	260°C
ESD Rating	2kV HBM

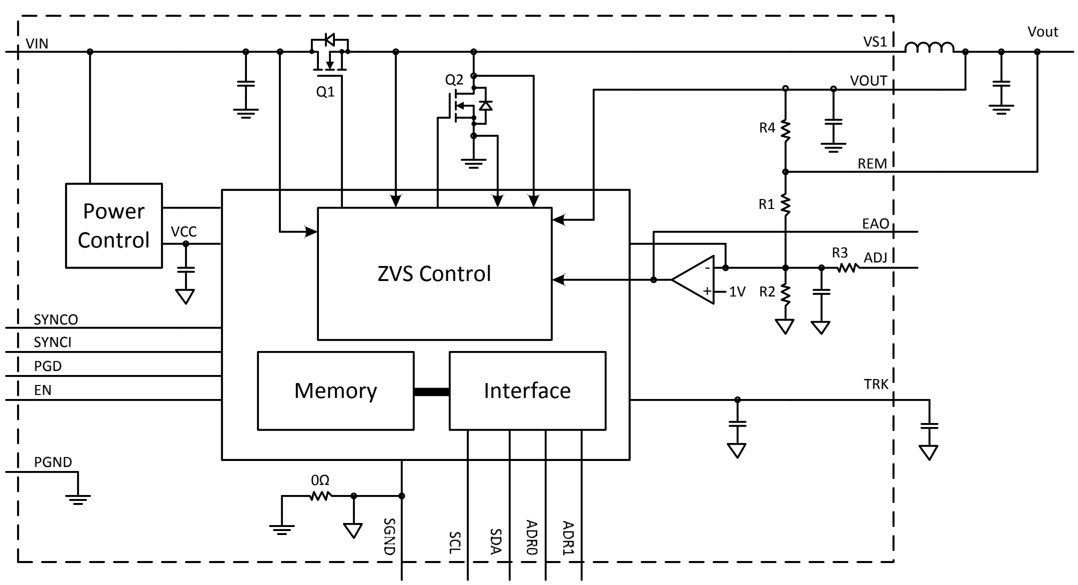


Figure 1: *Simplified Block Diagram*

(I^2C pins SCL, SDA, ADR0, and ADR1 only active for PI33XX-20 and PI33XX-21 versions)

PI3311-X0 (1.0 VOUT) Electrical Characteristics

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, Vin =24V, L1=120nH

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Efficiency			87.7		%	Vin = 24V, T_C = 25°C, Iout = 10 A
Output						
Output Voltage	V_{OUT_DC}		1.0		V	0 °C <T_J <70°C
Output Voltage Total Regulation	V_{OUT_DC}	0.987	1.0	1.013	V	-40 °C <T_J <125°C
Output Voltage Range	V_{OUT_DC}		1.0	1.4	V	
Line Regulation	$\Delta V_{OUT}(\Delta V_{IN})$		0.1	0.15	%	@ 25°C, 12V<Vin<36V
Load Regulation	$\Delta V_{OUT}(\Delta I_{OUT})$		0.1	0.15	%	@ 25°C, 0.5A<Iout<10A
Output Voltage Ripple	V_{OUT_AC}		20		mVp-p	Iout=5A, Cout=8x100µF, 20MHz BW
Continuous Output Current Range	I_{OUT_DC}	0		10	A	See I_{out} vs. T_A Curves
Current Limit	I_{OUT_CL}	10.2		13	A	
Input Current						
Input Current	I_{IN_DC}		476		mA	Vin = 24V, T_C = 25°C, Iout=10A
Inrush Input Current At Soft Start	I_{IN_SS}		200		mA	Vin=24V, Iout=0A Cin=4x4.7µF MLCC
Input Current At Output Short (Fault Condition)	I_{IN_Short}			300	mA	
Protection						
UVLO Threshold	V_{UVLO}	7.08	7.45	7.82	V	
UVLO Hysteresis	V_{UVLO_HYS}		0.37		V	
OVLO Threshold	V_{OVLO}	37	38.4	40	V	
OVLO Hysteresis	V_{OVLO_HYS}		0.77		V	
UVLO/OVLO Fault Delay Time	t_{f_DLY}		128		Cycles	Number of the switching frequency cycles
UVLO/OVLO Response Time	t_f		500		ns	+1% overdrive
OVP	V_{OVP}		20		%	Above VOUT
Over-Temperature Fault Threshold	V_{OTP}	130	135	140	°C	
Over-Temperature Restart Hysteresis	V_{OTP_HYS}		30		°C	
Timing						
Switching Frequency	f_S		380		kHz	Vin ≥ 18V, Iout ≤ 8A (1)
Fault Restart Delay	t_{FR_DLY}		30		ms	

PI3311-X0 Electrical Specifications (continued)

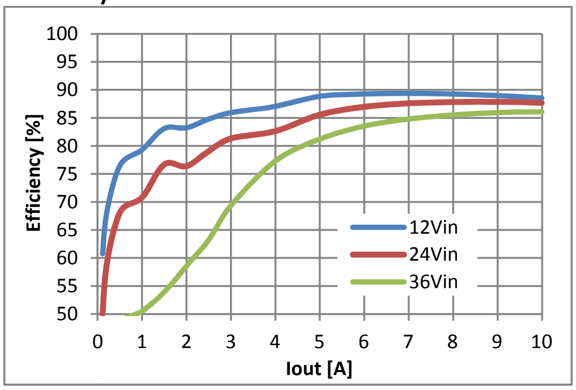
Unless otherwise specified: -40°C < T_J < 125°C, Vin =24V,

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Input Power						
Input Voltage	V_{IN_DC}	8	24	36	V	
Input Voltage Slew Rate	V_{IN_SR}			1	V/µs	
Input Quiescent Current	I_{Q_VIN}		2 2.5		mA	Disabled Enabled
Soft Start And Tracking Function						
TRK Active Range (Nominal)	V_{TRK}	0		1	V	
TRK Offset Voltage / Disable Threshold	V_{TRK_OV}	20	40	60	mV	
Charge Current (Soft – Start)	I_{TRK}	-70	-50	-30	µA	
Discharge Current (Fault)	I_{TRK_DIS}		6.8		mA	
Soft-Start Time	t_{SS}		2.2	2.6	ms	C_{TRK} = 0
Enable						
High Threshold	V_{EN_HI}	0.9	1	1.1	V	
Low Threshold	V_{EN_LO}	0.7	0.8	0.9	V	
Threshold Hysteresis	V_{EN_HYS}	100	200	300	mV	
Enable Pull-Up Voltage	V_{EN_PU}		2		V	
Enable Pull-Down Voltage	V_{EN_PD}		0		V	
Source Current	I_{EN_SO}		-50		uA	
Sink Current	I_{EN_SK}		50		uA	
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	50		110	%	With respect to the set switching frequency
SYNCI Threshold	V_{SYNCI}		2.5		V	
SYNCI Programmable Phase Shift	$\Delta\phi_{SYNCI}$	0		-270	°	
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	4.5		5.2	V	Source 1mA.
SYNCO Low	V_{SYNCO_LO}	0		0.5	V	Sink 1mA.
SYNCO Rise Time	t_{SYNCO_RT}		10	20	ns	20pF load
SYNCO Fall Time	t_{SYNCO_FT}		10	20	ns	20pF load

Note 1: Refer to Switching Frequency vs. Iout graph

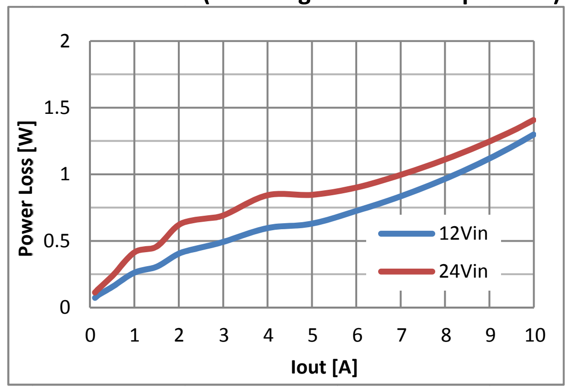
PI3311-X0 Typical Characteristics

Efficiency at 25°C



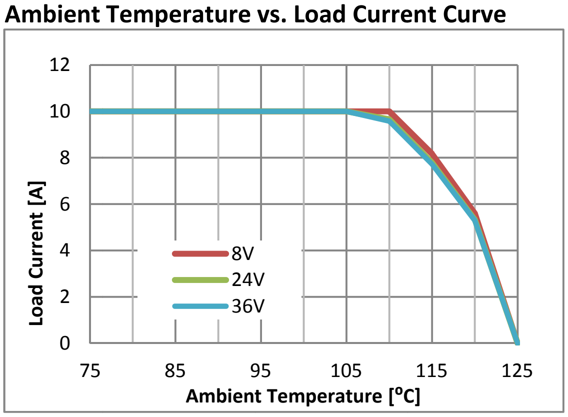
331101

Total Power Loss (including external components)



331102

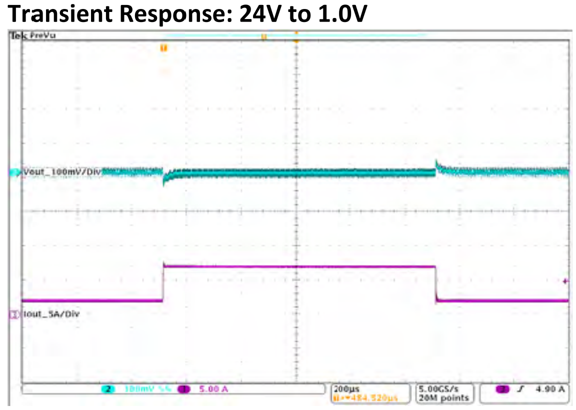
Ambient Temperature vs. Load Current Curve



0 LFM, SiP Only

331103

Transient Response: 24V to 1.0V

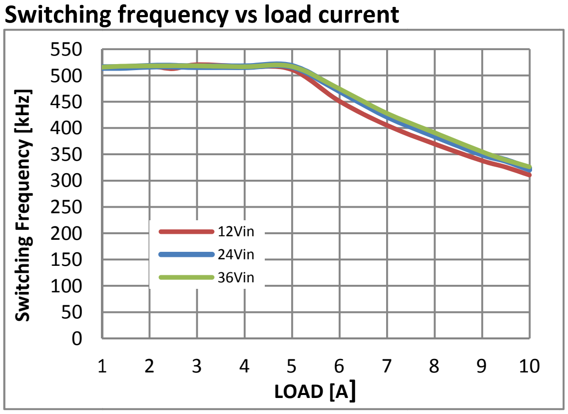


Load Step: 2A to 7A at 5A/us

Cout = 8X 100 µF Ceramic

331104

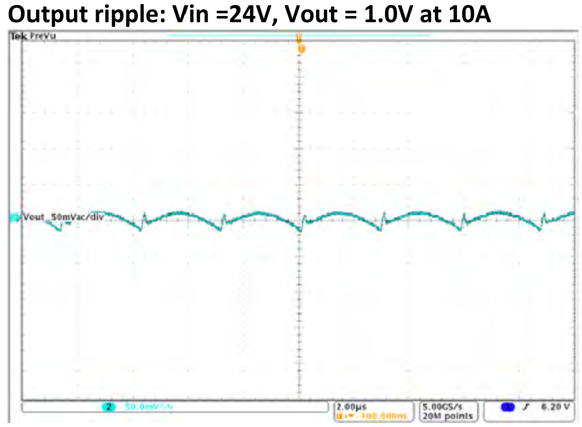
Switching frequency vs load current



L1 = 120nH

331105

Output ripple: Vin =24V, Vout = 1.0V at 10A



Vout = 50mV/Div

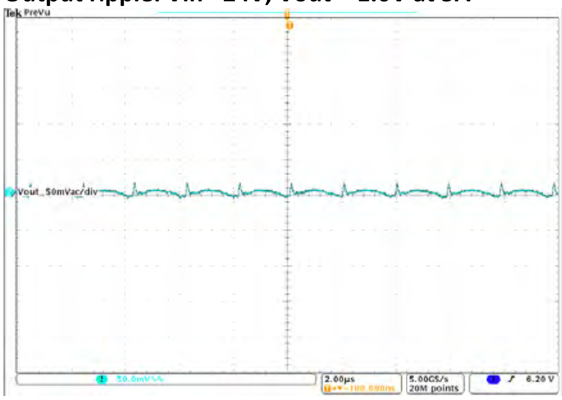
2.0us/Div

Cout = 8X 100 µF Ceramic

331106

PI3311-X0 Typical Characteristics (continued)

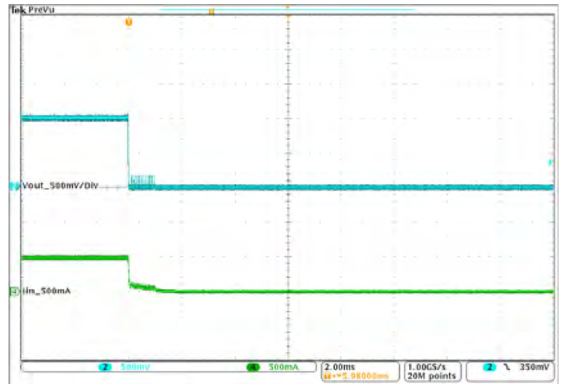
Output ripple: Vin =24V, Vout = 1.0V at 5A



Vout = 50mV/Div
2.0us/Div
Cout = 8X 100 µF Ceramic

331107

Short circuit test



Vout = 500mV/Div =Ch2
Iin = 500mA/Div = Ch4
tdelay_fault = 1ms

331108

PI3312-X0 (2.5 Vout) Electrical Characteristics

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, Vin = 24V, L1=200 nH

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Efficiency			91.3		%	Vin = 24V, T_C = 25°C, Iout = 10 A
Output						
Output Voltage	V_{OUT_DC}		2.50		V	0 °C <T_J <70°C
Output Voltage Total Regulation	V_{OUT_DC}	2.465	2.50	2.535	V	-40 °C <T_J <125°C
Output Voltage Range	V_{OUT_DC}	2.0	2.5	3.1	V	
Line Regulation	$\Delta V_{OUT}(\Delta V_{IN})$		0.1	0.15	%	@ 25°C 12V<Vin<36V
Load Regulation	$\Delta V_{OUT}(\Delta I_{OUT})$		0.1	0.15	%	@ 25°C, 0.5A<Iout<10A
Output Voltage Ripple	V_{OUT_AC}		28		mVp-p	Iout=5A, Cout=4x100µF, 20MHz BW
Continuous Output Current Range	I_{OUT_DC}	0		10	A	
Current Limit	I_{OUT_CL}		12		A	
Input Current						
Input Current	I_{IN_DC}		1.14		A	Vin = 24V, T_C = 25°C, Iout=10A
Soft-Start Current	I_{IN_SS}		200		mA	Vin=24V, Iout=0A Cin=4x4.7µF MLCC
Input Current At Output Short (Fault Condition)	I_{IN_Short}			300	mA	
Protection						
UVLO Threshold	V_{UVLO}	7.08	7.45	7.82	V	
UVLO Hysteresis	V_{UVLO_HYS}		0.37		V	
OVLO Threshold	V_{OVLO}	37	38.4	40	V	
OVLO Hysteresis	V_{OVLO_HYS}		0.77		V	
UVLO/OVLO Fault Delay Time	t_{f_DLY}		128		Cycles	Number of the switching frequency cycles
UVLO/OVLO Response Time	t_f		500		ns	+1% overdrive
OVP Threshold	V_{OVP}		20		%	Above VOUT
Over-Temperature Fault Threshold	V_{OTP}	130	135	140	°C	
Over-Temperature Restart Hysteresis	V_{OTP_HYS}		30		°C	
Timing						
Switching Frequency	f_S		500		kHz	Vin ≥ 18V, Iout ≤ 8A (1)
Fault Restart Delay	t_{FR_DLY}		30		ms	

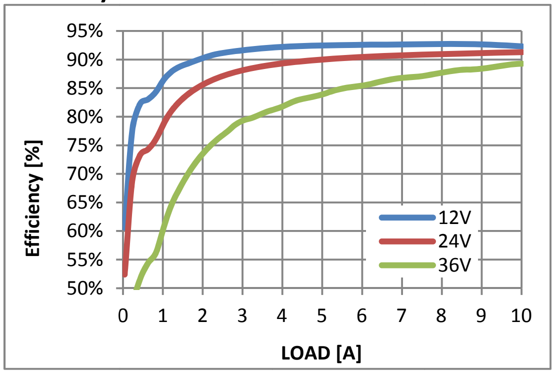
PI3312-X0 Electrical Specifications (continued)

Unless otherwise specified: -40°C < T_J < 125°C, Vin =24V,

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Input Power						
Input Voltage	V_{IN_DC}	8	24	36	V	
Input Voltage Slew Rate	V_{IN_SR}			1	V/µs	
Input Quiescent Current	I_{Q_VIN}		2 2.5		mA	Disabled Enabled
Soft Start And Tracking Function						
TRK Active Range (Nominal)	V_{TRK}	0		1	V	
TRK Offset Voltage / Disable Threshold	V_{TRK_OV}	20	40	60	mV	
Charge Current (Soft –Start)	I_{TRK}	-70	-50	-30	µA	
Discharge Current (Fault)	I_{TRK_DIS}		6.8		mA	
Soft-Start Time	t_{SS}		2.2	2.6	ms	C_{TRK} = 0, 0A< Iout ≤ 8A
Enable						
Enable High Threshold	V_{EN_HI}	0.9	1	1.1	V	
Enable Low Threshold	V_{EN_LO}	0.7	0.8	0.9	V	
Enable Threshold Hysteresis	V_{EN_HYS}	100	200	300	mV	
Enable Pull-Up Voltage	V_{EN_PU}		2		V	
Enable Pull-Down Voltage	V_{EN_PD}		0		V	
Source Current	I_{EN_SO}		-50		uA	
Sink Current	I_{EN_SK}		50		uA	
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	50		110	%	With respect to the set switching frequency
SYNCI Threshold	V_{SYNCI}		2.5		V	
SYNCI Programmable Phase Shift	$\Delta\phi_{SYNCI}$	0		270	°	
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	4.5		5.2	V	Source 1mA.
SYNCO Low	V_{SYNCO_LO}	0		0.5	V	Sink 1mA.
SYNCO Rise Time	t_{SYNCO_RT}		10	20	ns	20pF load
SYNCO Fall Time	t_{SYNCO_FT}		10	20	ns	20pF load

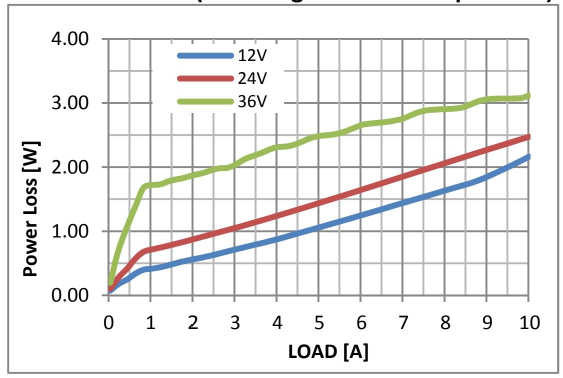
PI3312-X0 Typical Characteristics

Efficiency at 25°C



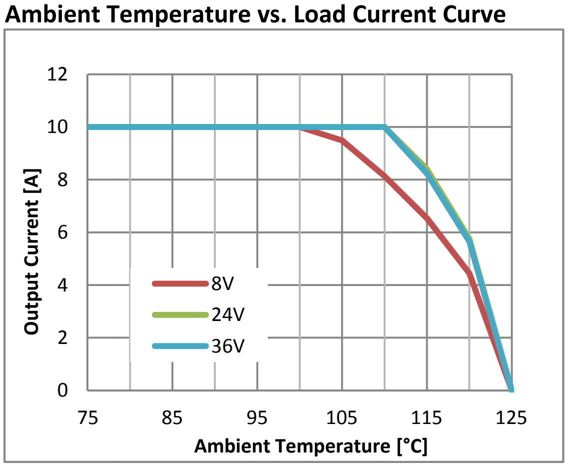
L1=200nH 331201

Total Power Loss (including external components)



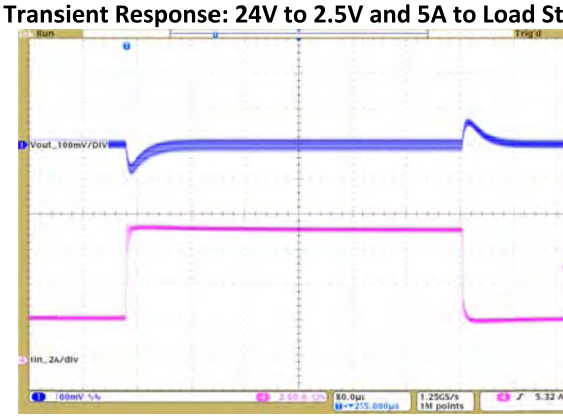
331202

Ambient Temperature vs. Load Current Curve



0 LFM, SiP Only 331203

Transient Response: 24V to 2.5V and 5A to Load Step



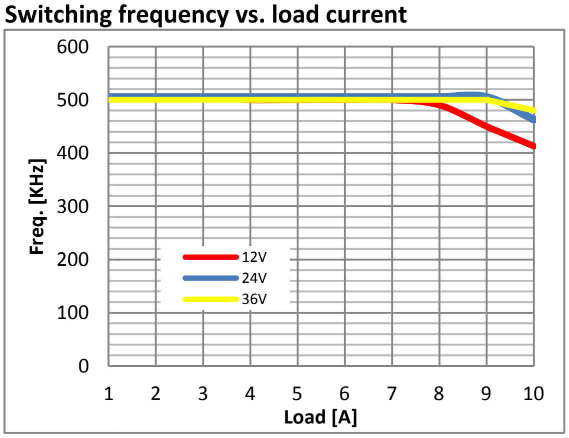
Vout = 100mV/Div. = Ch 1 331204

Iout = 2A/Div. = Ch 4

200us/Div.

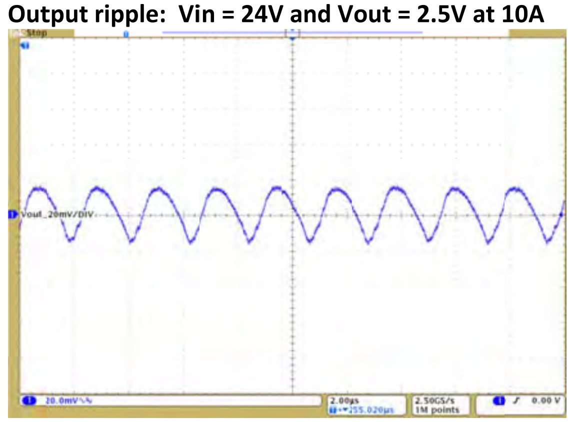
Cout = 4 x 100µF Ceramic

Switching frequency vs. load current



L1 = 200nH 331205

Output ripple: Vin = 24V and Vout = 2.5V at 10A



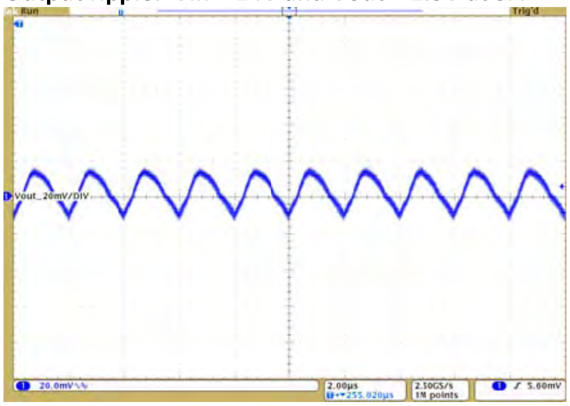
Vout = 20mV/Div. 331206

2.0us/Div.

Cout = 4 x 100µF Ceramic

PI3312-X0 Typical Characteristics (continued)

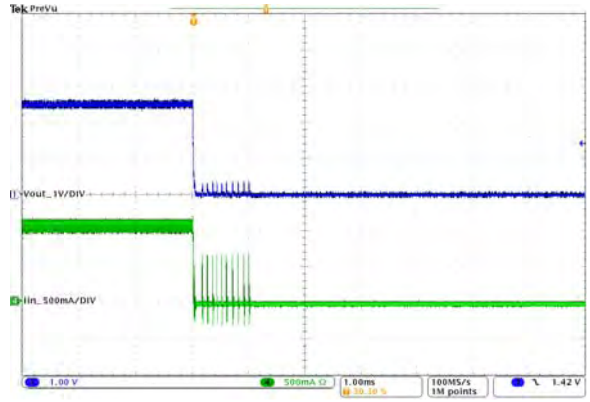
Output ripple: Vin = 24V and Vout = 2.5V at 5A



Vout = 20mV/Div.
2.0us/Div.
Cout = 4 x 100µF Ceramic

331207

Short circuit test



Vout = 1V/Div. = Ch4
Iin = 500mA/Div. = Ch1
tdelay_fault = 1ms

331208

PI3301-X0 (3.3 Vout) Electrical Characteristics

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, Vin =24V, L1=200 nH

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Efficiency			92.2		%	Vin = 24V, T_C = 25°C, Iout = 10 A
Output						
Output Voltage	V_{OUT_DC}		3.30		V	0 °C <T_J <70°C
Output Voltage Total Regulation	V_{OUT_DC}	3.25	3.30	3.36	V	-40 °C <T_J <125°C
Output Voltage Range	V_{OUT_DC}	2.3	3.3	4.1	V	
Line Regulation	$\Delta V_{OUT}(\Delta V_{IN})$		0.10	0.15	%	@ 25°C 12V<Vin<36V
Load Regulation	$\Delta V_{OUT}(\Delta I_{OUT})$		0.10	0.15	%	@ 25°C, 0.5A<Iout<10A
Output Voltage Ripple	V_{OUT_AC}		37.5		mVp-p	Iout=5A, Cout=4x100µF, 20MHz BW
Continuous Output Current Range	I_{OUT_DC}	0		10	A	
Current Limit	I_{OUT_CL}		12		A	
Input Current						
Input Current	I_{IN_DC}		1.49		A	Vin = 24V, T_C = 25°C, Iout=10A
Soft-Start Input Current	I_{IN_SS}		200		mA	Vin=24V, Iout=0A Cin=4x4.7µF MLCC
Input Current At Output Short (Fault Condition)	I_{IN_Short}			300	mA	
Protection						
UVLO Threshold	V_{UVLO}	7.08	7.45	7.82	V	
UVLO Hysteresis	V_{UVLO_HYS}		0.37		V	
OVLO Threshold	V_{OVLO}	37	38.4	40.0	V	
OVLO Hysteresis	V_{OVLO_HYS}		0.77		V	
UVLO/OVLO Fault Delay Time	t_{f_DLY}		128		Cycles	Number of the switching frequency cycles
UVLO/OVLO Response Time	t_f		500		ns	+1% overdrive
OVP	V_{OVP}		20		%	Above VOUT
Over-Temperature Fault Threshold	V_{OTP}	130	135	140	°C	
Over-Temperature Restart Hysteresis	V_{OTP_HYS}		30		°C	
Timing						
Switching Frequency	f_S		650		kHz	Vin ≥ 12V, Iout ≤ 10A (1)
Fault Restart Delay	t_{FR_DLY}		30		ms	

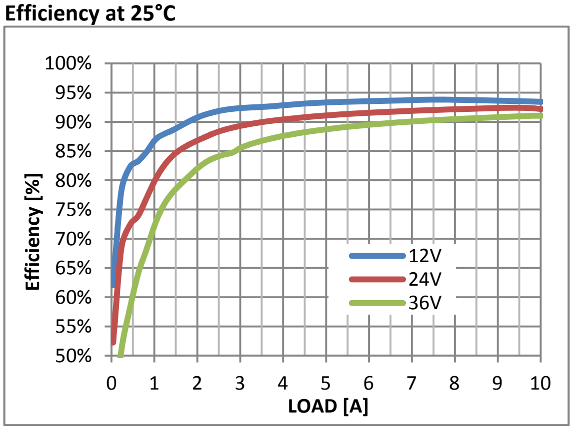
PI3301-X0 Electrical Specifications (continued)

Unless otherwise specified: -40°C < T_J < 125°C, Vin =24V,

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Input Power						
Input Voltage	V_{IN_DC}	8	24	36	V	
Input Voltage Slew Rate	V_{IN_SR}			1	V/µs	
Input Quiescent Current	I_{Q_VIN}		2 2.5		mA	Disabled Enabled
Soft Start And Tracking Function						
TRK Active Range (Nominal)	V_{TRK}	0		1	V	
TRK Offset Voltage / Disable Threshold	V_{TRK_OV}	20	40	60	mV	
Charge Current (Soft –Start)	I_{TRK}	-70	-50	-30	µA	
Discharge Current (Fault)	I_{TRK_DIS}		6.8		mA	
Soft-Start Time	t_{SS}		2.2	2.6	ms	No external **C_{TRK}**, 0A< Iout ≤ 8A
Enable						
Enable High Threshold	V_{EN_HI}	0.9	1	1.1	V	
Enable Low Threshold	V_{EN_LO}	0.7	0.8	0.9	V	
Enable Threshold Hysteresis	V_{EN_HYS}	100	200	300	mV	
Enable Pull-Up Voltage	V_{EN_PU}		2		V	
Enable Pull-Down Voltage	V_{EN_PD}		0		V	
Source Current	I_{EN_SO}		-50		uA	
Sink Current	I_{EN_SK}		50		uA	
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	50		110	%	With respect to the set switching frequency
SYNCI Threshold	V_{SYNCI}		2.5		V	
SYNCI Programmable Phase Shift	$\Delta \phi_{SYNCI}$	0		270	°	
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	4.5		5.2	V	Source 1mA.
SYNCO Low	V_{SYNCO_LO}	0		0.5	V	Sink 1mA.
SYNCO Rise Time	t_{SYNCO_RT}		10	20	ns	20pF load
SYNCO Fall Time	t_{SYNCO_FT}		10	20	ns	20pF load

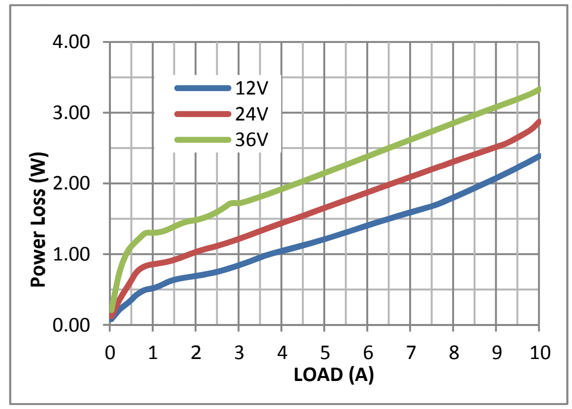
PI3301-X0 Typical Characteristic

Efficiency at 25°C



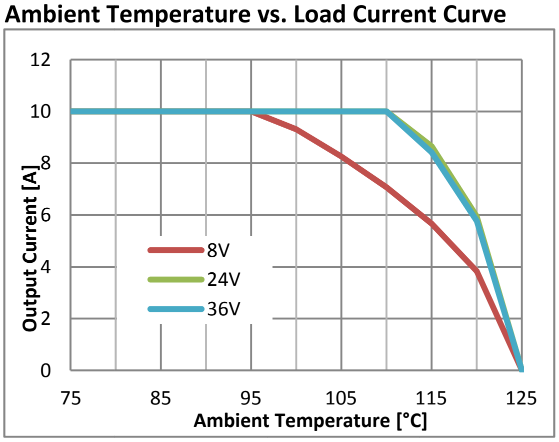
L1=200nH 330101

Total Power Loss (including external components)



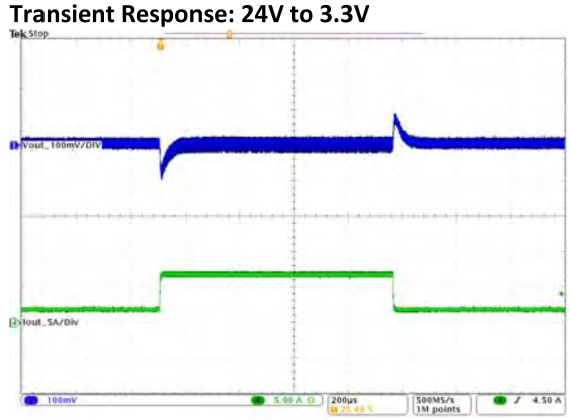
330102

Ambient Temperature vs. Load Current Curve



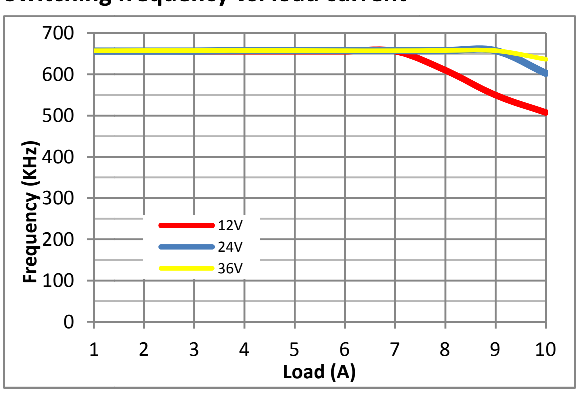
0 LFM, SiP Package Only 330103

Transient Response: 24V to 3.3V



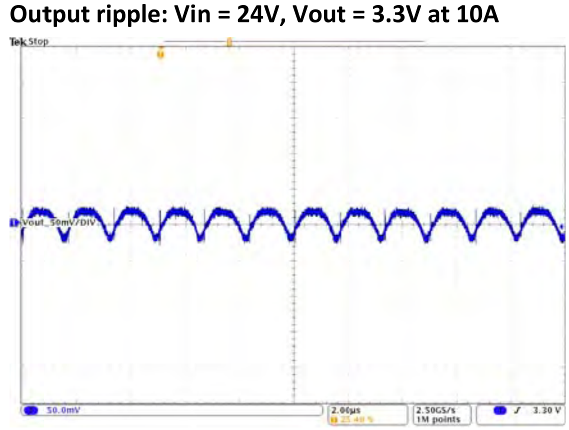
Load Step: 2A to 7A 330104
Cout = 4 x 100µF Ceramic

Switching frequency vs. load current



L1 = 200nH 330105

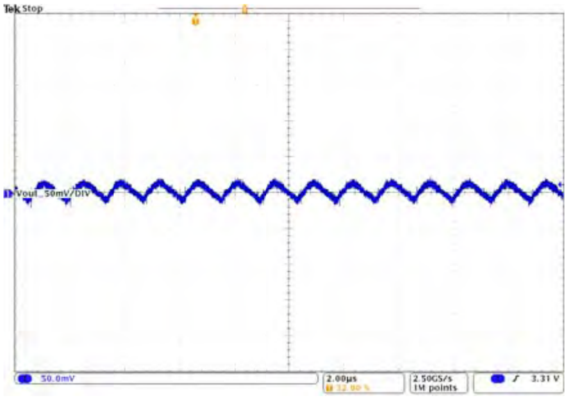
Output ripple: Vin = 24V, Vout = 3.3V at 10A



Vout = 50mV/Div 330106
2.0us/Div
Cout = 4 x 100µF Ceramic

PI3301-X0 Typical Characteristic (continued)

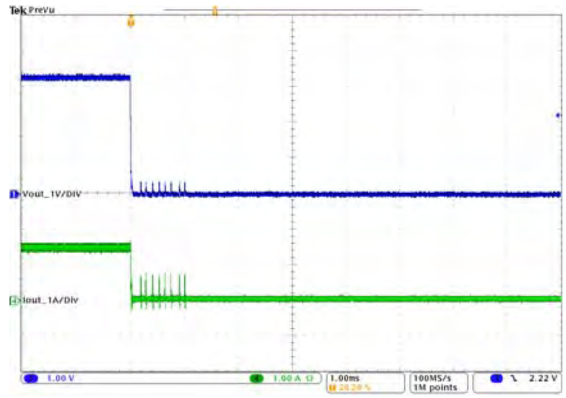
Output ripple Vin = 24V, Vout = 3.3V at 5A



Vout = 50mV/Div
2.0us/Div
Cout = 4 x 100µF Ceramic

330107

Short circuit test



t_{delay_fault} = 1ms

330108

PI3302-X0 (5.0Vout) Electrical Characteristics

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, Vin =24V, L1=200nH

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Efficiency						
Efficiency			93.9		%	Vin = 24V, T_C = 25°C, Iout=10A
Output						
Output Voltage			5.00		V	0 °C <T_J <70°C
Output Voltage Total Regulation	V_{OUT_DC}	4.93	5.00	5.07	V	-40 °C <T_J <125°C
Output Voltage Range		3.3	5.0	6.5	V	
Line Regulation	$\Delta V_{OUT}(\Delta V_{IN})$		0.1	0.15	%	@ 25°C 12V<Vin<36V
Load Regulation	$\Delta V_{OUT}(\Delta I_{OUT})$		0.1	0.15	%	@ 25°C, 0.5A<Iout<10A
Output Voltage Ripple	V_{OUT_AC}		30		mVp-p	Iout=5A, Cout=4x47µF20MHz BW
Continuous Output Current Range	I_{OUT_DC}	0		10	A	
Current Limit	I_{OUT_CL}	10.2	11.2	12.6	A	
Input Current						
Input Current	I_{IN_DC}		2.23		A	Vin = 24V, T_C = 25°C, Iout=10A
Inrush Input Current At Startup	I_{IN_SS}		100		mA	Vin=24V, Iout=0A Cin=4x4.7µF MLCC
Input Current At Output Short (Fault Condition)	I_{IN_Short}			300	mA	
Protection						
UVLO Threshold	V_{UVLO}	7.08	7.45	7.82	V	
UVLO Hysteresis	V_{UVLO_HYS}		0.37		V	
OVLO Threshold	V_{OVLO}	37	38.4	40	V	
OVLO Hysteresis	V_{OVLO_HYS}		0.77		V	
UVLO/OVLO Fault Delay Time	t_{f_DLY}		128		Cycles	Number of the switching frequency cycles
UVLO/OVLO Response Time	t_f		500		ns	+1% overdrive
OVP	V_{OVP}		20		%	Above VOUT
Over-Temperature Fault Threshold	V_{OTP}	130	135	140	°C	
Over-Temperature Restart Hysteresis	V_{OTP_HYS}		30		°C	
Timing						
Switching Frequency	f_S		1.0		MHz	Vin ≥ 18V, Iout ≤ 10A (1)
Fault Restart Delay	t_{FR_DLY}		30		ms	

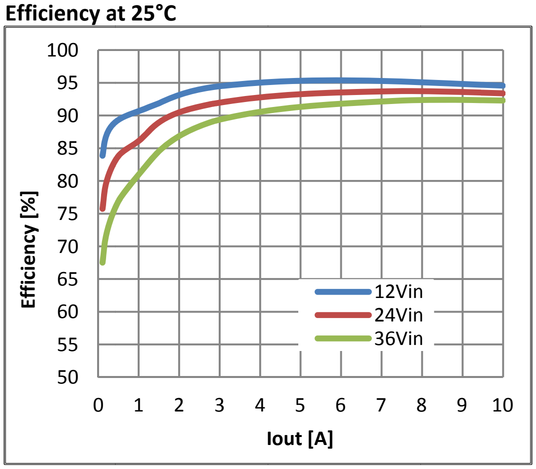
PI3302-X0 Electrical Specifications (continued)

Unless otherwise specified: -40°C < T_J < 125°C, Vin =24V,

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Input Power						
Input Voltage	V_{IN_DC}	8	24	36	V	
Input Voltage Slew Rate	V_{IN_SR}			1	V/µs	
Input Quiescent Current	I_{Q_VIN}		2 2.5		mA	Disabled Enabled
Soft Start And Tracking Function						
TRK Active Range (Nominal)	V_{TRK}	0		1	V	
TRK Offset Voltage / Disable Threshold	V_{TRK_OV}	20	40	60	mV	
Charge Current (Soft –Start)	I_{TRK}	-70	-50	-30	µA	
Discharge Current (Fault)	I_{TRK_DIS}		6.8		mA	
Soft-Start Time	t_{SS}		2.2	2.6	ms	No external **C_{TRK}**, 0A< Iout ≤ 8A
Enable						
Enable High Threshold	V_{EN_HI}	0.9	1	1.1	V	
Enable Low Threshold	V_{EN_LO}	0.7	0.8	0.9	V	
Enable Threshold Hysteresis	V_{EN_HYS}	100	200	300	mV	
Enable Pull-Up Voltage	V_{EN_PU}		2		V	
Enable Pull-Down Voltage	V_{EN_PD}		0		V	
Source Current	I_{EN_SO}		-50		uA	
Sink Current	I_{EN_SK}		50		uA	
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	50		110	%	With respect to the set switching frequency
SYNCI Threshold	V_{SYNCI}		2.5		V	
SYNCI Programmable Phase Shift	$\Delta\phi_{SYNCI}$	0		270	°	
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	4.5		5.2	V	Source 1mA.
SYNCO Low	V_{SYNCO_LO}	0		0.5	V	Sink 1mA.
SYNCO Rise Time	t_{SYNCO_RT}		10	20	ns	20pF load
SYNCO Fall Time	t_{SYNCO_FT}		10	20	ns	20pF load

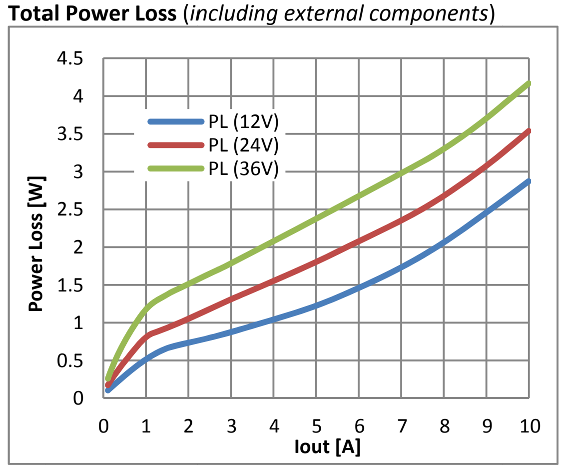
PI3302-X0 Typical Characteristics

Efficiency at 25°C



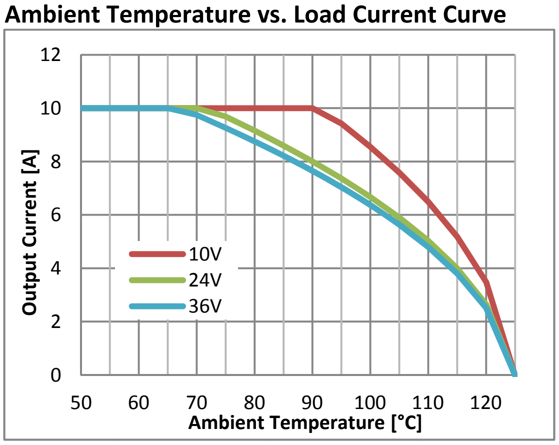
L1=200nH 330201

Total Power Loss (*including external components*)



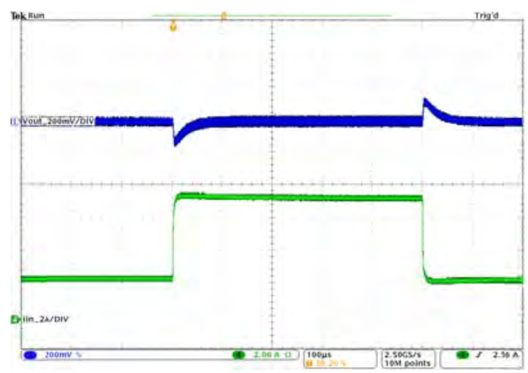
330202

Ambient Temperature vs. Load Current Curve



0 LFM, SiP Only 330203

Transient Response: 24V to 5V

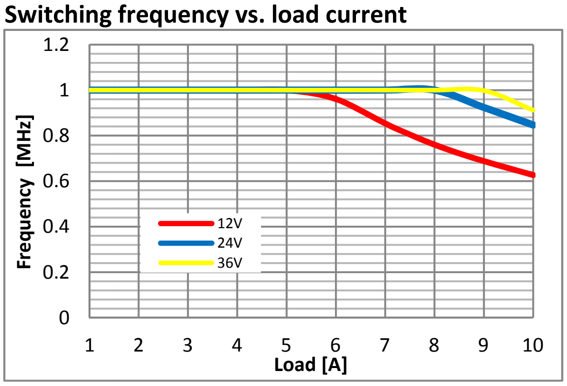


Load Step: 2A to 7A 330204

Cout = 4 X 47uF Ceramic

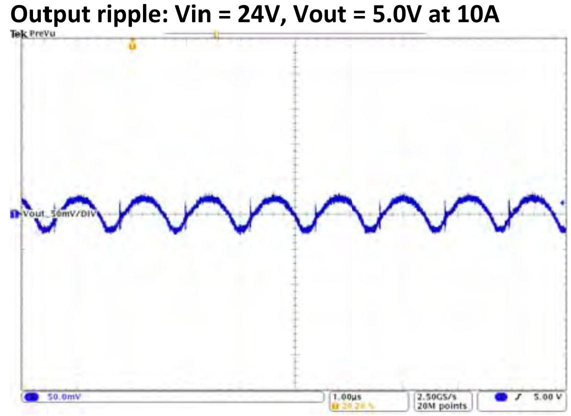
5A/us

Switching frequency vs. load current



L1=200nH 330205

Output ripple: Vin = 24V, Vout = 5.0V at 10A



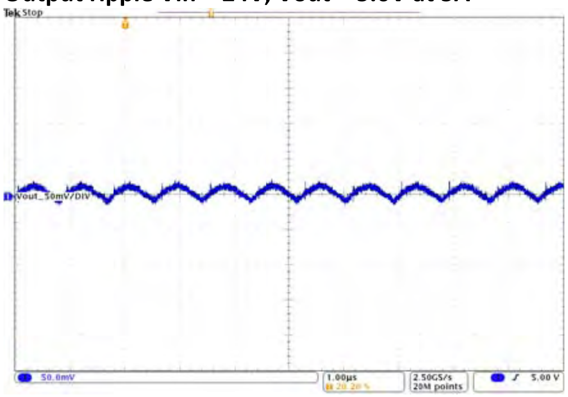
Vout = 50mV/Div 330206

1.0us/Div

Cout = 4 X 47uF Ceramic

PI3302-X0 Typical Characteristic (continued)

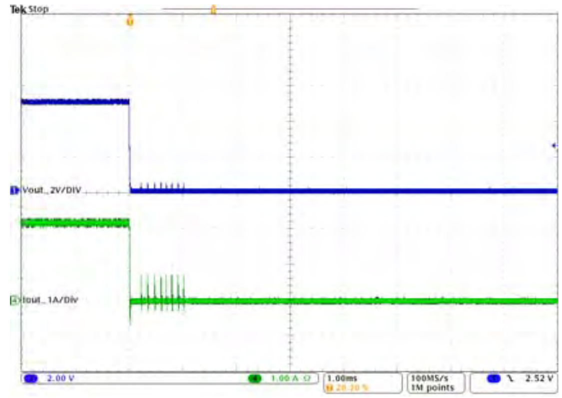
Output ripple Vin = 24V, Vout = 5.0V at 5A



Vout = 50mV/Div
1.0us/Div
Cout = 4 X 47uF Ceramic

330207

Short circuit test



t_{delay_fault} = 1ms

330208

PI3303-X0 (12Vout) Electrical Characteristics

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, Vin =24V, L1=230nH

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Efficiency			96.5		%	Vin = 24V, T_C = 25°C, Iout=8A
Output						
Output Voltage	V_{OUT_DC}		12.0		V	0 °C <T_J <70°C
Output Voltage Total Regulation	V_{OUT_DC}	11.82	12.0	12.18	V	-40 °C <T_J <125°C
Output Voltage Range	V_{OUT_DC}	6.5	12	13.0	V	
Line Regulation	$\Delta V_{OUT}(\Delta V_{IN})$		0.1	0.15	%	@ 25°C 16V<Vin<36V
Load Regulation	$\Delta V_{OUT}(\Delta I_{OUT})$		0.1	0.15	%	@ 25°C, 0.5A<Iout<8A
Output Voltage Ripple	V_{OUT_AC}		60		mVp-p	Iout=4A, Cout=4x22µF, 20MHz BW
Continuous Output Current Range	I_{OUT_DC}	0		8	A	
Current Limit	I_{OUT_CL}	8.1		10	A	
Input Current						
Input Current	I_{IN_DC}		4.15		A	Vin = 24V, T_C = 25°C, Iout=8A
Inrush Input Current At Startup	I_{IN_SS}		200		mA	Vin=24V, Iout=0A Cin=4x4.7µF MLCC
Input Current At Output Short (Fault Condition)	I_{IN_Short}			300	mA	
Protection						
UVLO Threshold	V_{UVLO}	13.57	14.29	15.0	V	
UVLO Hysteresis	V_{UVLO_HYS}		0.37		V	
OVLO Threshold	V_{OVLO}	37	38.4	40	V	
OVLO Hysteresis	V_{OVLO_HYS}		0.77		V	
UVLO/OVLO Fault Delay Time	t_{f_DLY}		128		Cycles	Number of the switching frequency cycles
UVLO/OVLO Response Time	t_f		500		ns	+1% overdrive
OVP	V_{OVP}		20		%	Above VOUT
Over-Temperature Fault Threshold	V_{OTP}	130	135	140	°C	
Over-Temperature Restart Hysteresis	V_{OTP_HYS}		30		°C	
Timing						
Switching Frequency	f_S		1.4		MHz	Vin ≥ 18V, Iout ≤ 8A (1)
Fault Restart Delay	t_{FR_DLY}		30		ms	

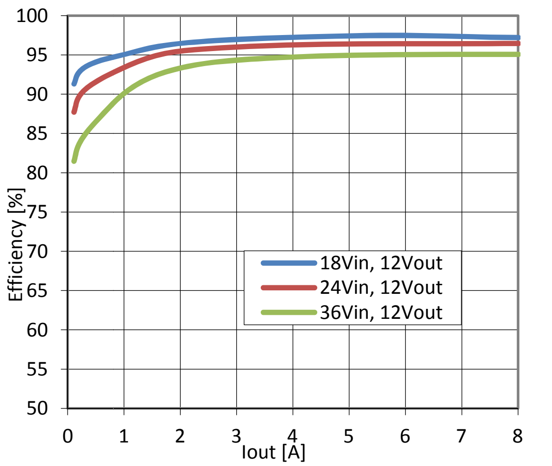
PI3303-X0 Electrical Specifications (continued)

Unless otherwise specified: -40°C < T_J < 125°C, Vin =24V,

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Input Power						
Input Voltage	V_{IN_DC}	15.5	24	36	V	
Input Voltage Slew Rate	V_{IN_SR}			1	V/µs	
Input Quiescent Current	I_{Q_VIN}		2 2.5		mA	Disabled Enabled
Soft Start And Tracking Function						
TRK Active Range (Nominal)	V_{TRK}	0		1	V	
TRK Offset Voltage / Disable Threshold	V_{TRK_OV}	20	40	60	mV	
Charge Current (Soft –Start)	I_{TRK}	-70	-50	-30	µA	
Discharge Current (Fault)	I_{TRK_DIS}		6.8		mA	
Soft-Start Time	t_{SS}		2.2	2.6	ms	No external C_{TRK}, 0A< Iout ≤ 8A
Enable						
Enable High Threshold	V_{EN_HI}	0.9	1	1.1	V	
Enable Low Threshold	V_{EN_LO}	0.7	0.8	0.9	V	
Enable Threshold Hysteresis	V_{EN_HYS}	100	200	300	mV	
Enable Pull-Up Voltage	V_{EN_PU}		2		V	
Enable Pull-Down Voltage	V_{EN_PD}		0		V	
Source Current	I_{EN_SO}		-50		uA	
Sink Current	I_{EN_SK}		50		uA	
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	50		110	%	With respect to the set switching frequency
SYNCI Threshold	V_{SYNCI}		2.5		V	
SYNCI Programmable Phase Shift	$\Delta\phi_{SYNCI}$	0		270	°	
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	4.5		5.2	V	Source 1mA.
SYNCO Low	V_{SYNCO_LO}	0		0.5	V	Sink 1mA.
SYNCO Rise Time	t_{SYNCO_RT}		10	20	ns	20pF load
SYNCO Fall Time	t_{SYNCO_FT}		10	20	ns	20pF load

PI3303-X0 Typical Characteristics

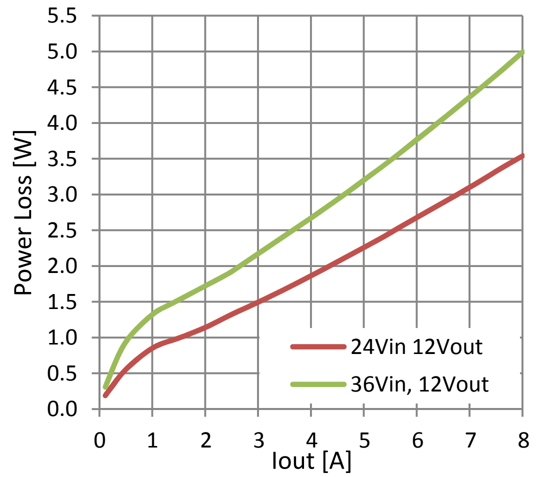
Efficiency at 25°



L1=230nH

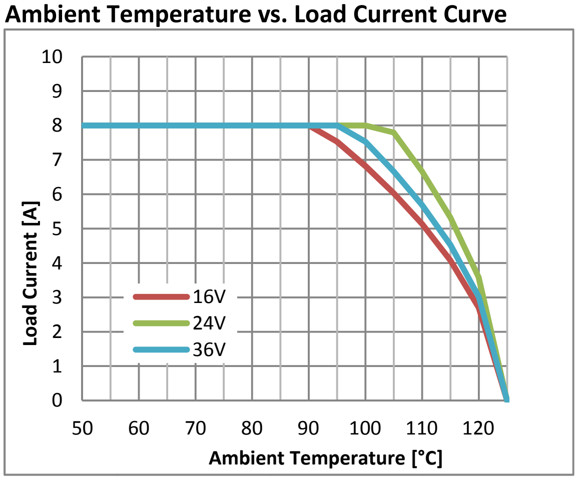
330301

Total Power Loss (*including external components*)



330302

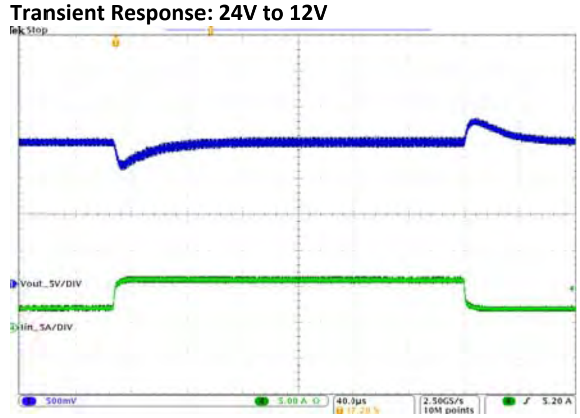
Ambient Temperature vs. Load Current Curve



O LFM SiP Only

330303

Transient Response: 24V to 12V

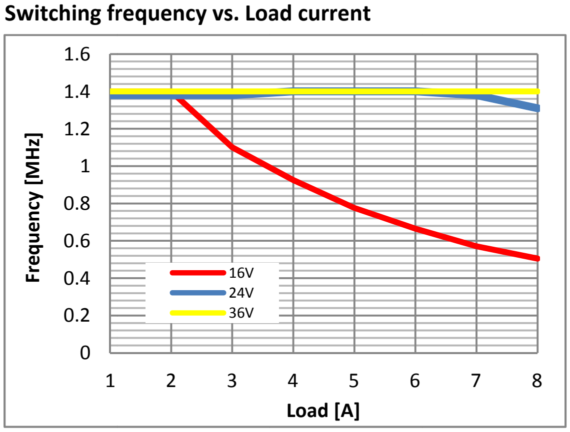


Load Step: 2A to 6A, 5A/us

Cout = 4 X 22uF Ceramic

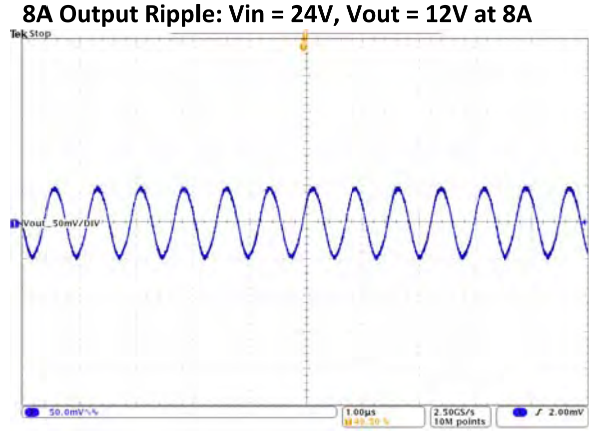
330304

Switching frequency vs. Load current



330305

8A Output Ripple: Vin = 24V, Vout = 12V at 8A



Vout = 50mV/Div

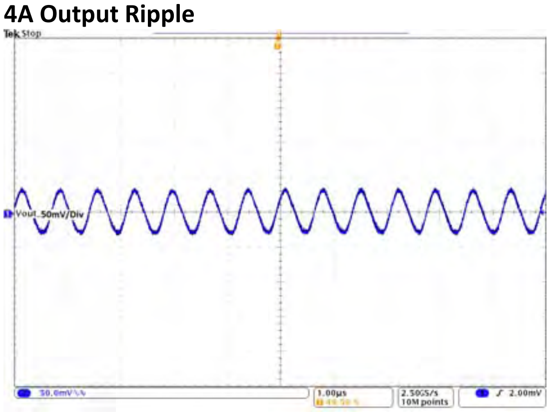
1.0us/Div

Cout = 4 X 22uF Ceramic

330306

PI3303-X0 Typical Characteristics (continued)

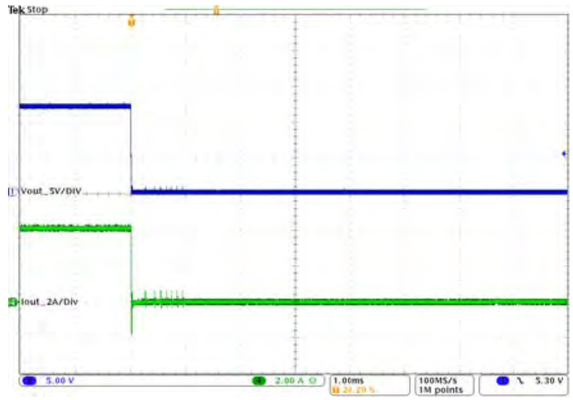
4A Output Ripple



Vout = 50mV/Div
1.0us/Div
Cout = 4 X 22uF Ceramic

330307

Short circuit test



t_{delay_fault} = 1ms

330308

PI3305-X0 (15 Vout) Electrical Characteristics

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, Vin =24V, L1=230nH

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Efficiency			97.2		%	Vin = 24V, T_C = 25°C, Iout = 10 A
Output						
Output Voltage			15.0		V	10 °C <T_J <70°C
Output Voltage Total Regulation	V_{OUT_DC}	14.78	15.0	15.23	V	-40 °C <T_J <125°C
Output Voltage Range		10.0	15	16	V	
Line Regulation	$\Delta V_{OUT}(\Delta V_{IN})$		0.1	0.15	%	@ 25°C 18.5V<Vin<36V
Load Regulation	$\Delta V_{OUT}(\Delta I_{OUT})$		0.1	0.15	%	@ 25°C, 0.5A<Iout< 8A
Output Voltage Ripple	V_{OUT_AC}		60		mVp-p	Iout=4A, Cout=4x22µF, 20MHz BW
Continuous Output Current Range	I_{OUT_DC}	0		8	A	
Current Limit	I_{OUT_CL}	8.1		10	A	
Input Current						
Input Current	I_{IN_DC}		4.12		A	Vin = 24V, T_C = 25°C, Iout=8A
Inrush Input Current At Startup	I_{IN_SS}		200		mA	Vin=24V, Iout=0A Cin=4x4.7µF MLCC
Input Current At Output Short (Fault Condition)	I_{IN_Short}			300	mA	
Protection						
UVLO Threshold	V_{UVLO}	16.38	17.2	18.1	V	
UVLO Hysteresis	V_{UVLO_HYS}		0.37		V	
OVLO Threshold	V_{OVLO}	37	38.4	40	V	
OVLO Hysteresis	V_{OVLO_HYS}		0.77		V	
UVLO/OVLO Fault Delay Time	t_{f_DLY}		128		Cycles	Number of the switching frequency cycles
UVLO/OVLO Response Time	t_f		500		ns	+1% overdrive
OVP	V_{OVP}		20		%	Above Vout
Over-Temperature Fault Threshold	V_{OTP}	130	135	140	°C	
Over-Temperature Restart Hysteresis	V_{OTP_HYS}		30		°C	
Timing						
Switching Frequency	f_S		1.5		MHz	Vin ≥ 18.1V, Iout ≤ 8A (1)
Fault Restart Delay	t_{FR_DLY}		30		ms	

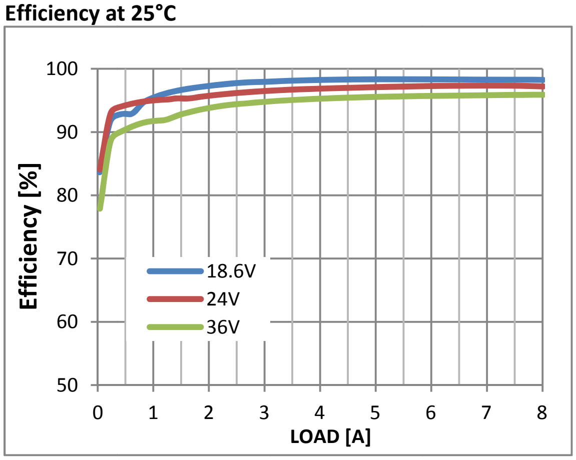
PI3305-X0 Electrical Specifications (continued)

Unless otherwise specified: -40°C < T_J < 125°C, Vin =24V,

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Input Power						
Input Voltage	V_{IN_DC}	18.6	24	36	V	
Input Voltage Slew Rate	V_{IN_SR}			1	V/µs	
Input Quiescent Current	I_{Q_VIN}		2 2.5		mA	Disabled Enabled
Soft Start And Tracking Function						
TRK Active Range (Nominal)	V_{TRK}	0		1	V	
TRK Offset Voltage / Disable Threshold	V_{TRK_OV}	20	40	60	mV	
Charge Current (Soft –Start)	I_{TRK}	-70	-50	-30	µA	
Discharge Current (Fault)	I_{TRK_DIS}		6.8		mA	
Soft-Start Time	t_{SS}		2.2	2.6	ms	No external C_{TRK}, 0A< Iout ≤ 8A
Enable						
Enable High Threshold	V_{EN_HI}	0.9	1	1.1	V	
Enable Low Threshold	V_{EN_LO}	0.7	0.8	0.9	V	
Enable Threshold Hysteresis	V_{EN_HYS}	100	200	300	mV	
Enable Pull-Up Voltage	V_{EN_PU}		2		V	
Enable Pull-Down Voltage	V_{EN_PD}		0		V	
Source Current	I_{EN_SO}		-50		uA	
Sink Current	I_{EN_SK}		50		uA	
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	50		110	%	With respect to the set switching frequency
SYNCI Threshold	V_{SYNCI}		2.5		V	
SYNCI Programmable Phase Shift	$\Delta\phi_{SYNCI}$	0		270	°	
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	4.5		5.2	V	Source 1mA.
SYNCO Low	V_{SYNCO_LO}	0		0.5	V	Sink 1mA.
SYNCO Rise Time	t_{SYNCO_RT}		10	20	ns	20pF load
SYNCO Fall Time	t_{SYNCO_FT}		10	20	ns	20pF load

PI3305-X0 Typical Characteristics

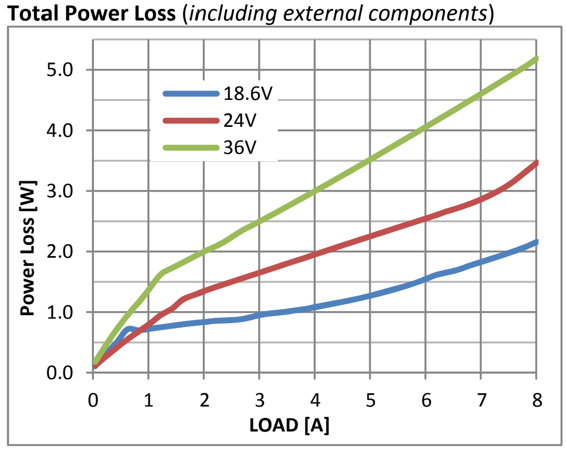
Efficiency at 25°C



L1=230nH

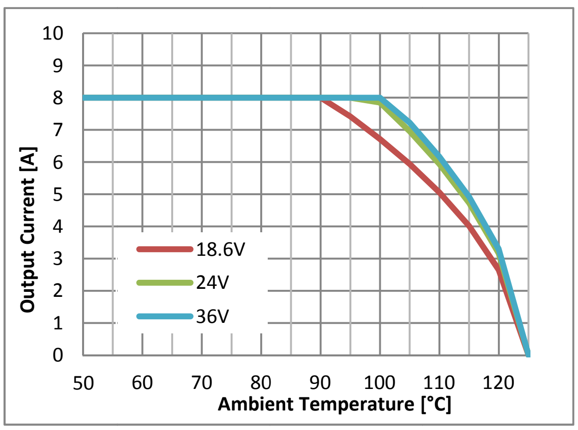
330501

Total Power Loss (*including external components*)



330502

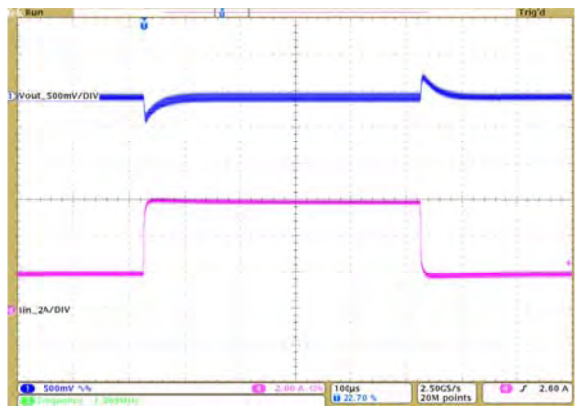
Ambient Temperature vs. Load Current Curve



O LFM, SiP Only

330503

Transient Response: 24 to 15V



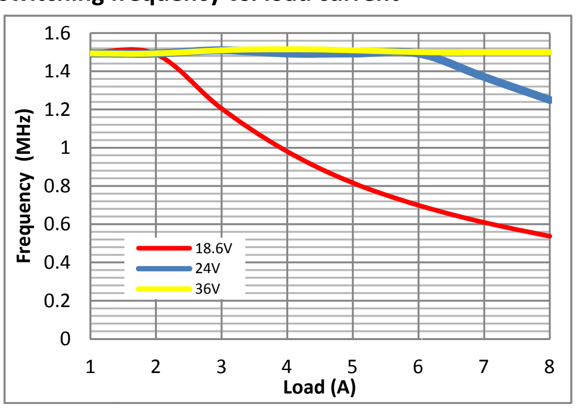
Load Step: 2A to 6A

330504

5A/us

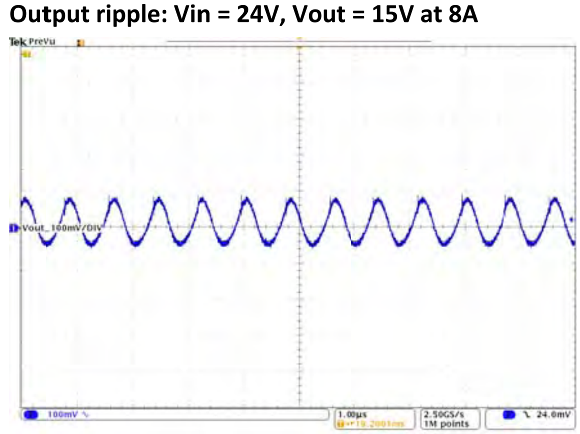
Cout = 4x22µF Ceramic

Switching frequency vs. load current



330505

Output ripple: Vin = 24V, Vout = 15V at 8A



Vout = 100mV/Div

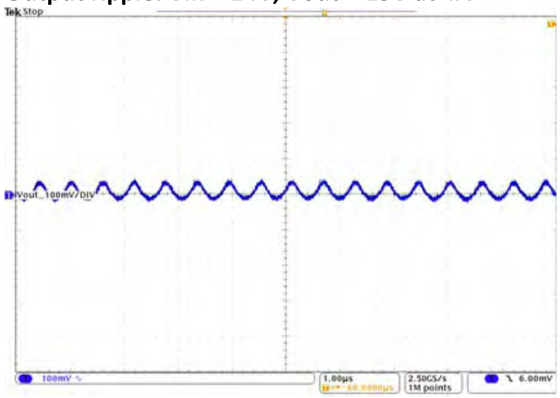
330506

1us/Div

Cout = 4x22µF Ceramic

PI3305-X0 Typical Characteristics (continued)

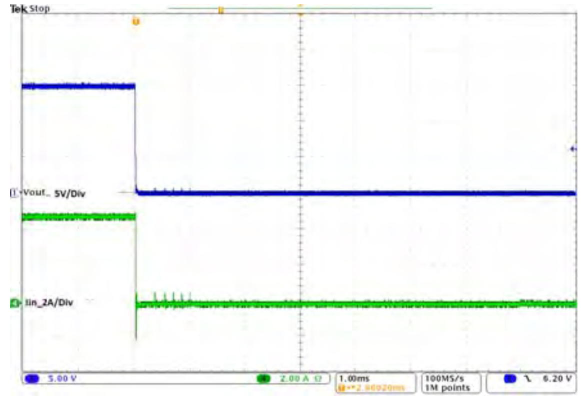
Output ripple: Vin = 24V, Vout = 15V at 4A



330507

Vout = 100mV/Div
1us/Div
Cout = 4x22µF Ceramic

Short circuit test



330508

Functional Description

The PI33XX is a family of highly integrated ZVS-Buck regulators. The PI33XX has a set output voltage that is trimmable within a prescribed range. Performance and maximum output current are characterized with a specific external power inductor (see Table 5).

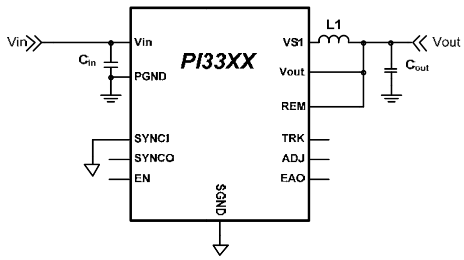


Figure 2 - *ZVS-Buck with required components*

For basic operation, Figure 2 shows the connections and components required. No additional design or settings are required.

ENABLE (EN)

EN is the enable pin of the converter. The EN Pin is referenced to SGND and permits the user to turn the converter on or off. The EN default polarity is a positive logic assertion. If the EN pin is left floating or asserted high, the converter output is enabled. Pulling EN pin below 0.8 Vdc with respect to SGND will disable the regulator output.

The EN input polarity can be programmed (PI33XX-20 and PI33XX-21 versions only) via the I^2C data bus. When the EN pin polarity is programmed for negative logic assertion; and if the EN pin is left floating, the regulator output is enabled. Pulling the EN pin above 1.0 Vdc with respect to SGND, will disable the regulator output.

Switching Frequency Synchronization

The SYNCI input allows the user to synchronize the controller switching frequency by an external clock referenced to SGND. The external clock can synchronize the unit between 50% and 110% of the preset switching frequency (f_S). For PI33XX-20 and PI33XX-21 versions only, the phase delay can be programmed via I^2C bus with respect to the clock applied at SYNCI pin. Phase delay allows PI33XX regulators to be paralleled and operate in an interleaving mode.

The PI33XX default for SYNCI is to sync with respect to the falling edge of the applied clock providing 180° phase shift from SYNCO. This allows for the paralleling of two PI33XX devices without the need for further user programming or external sync clock circuitry. The user can change the SYNCI polarity to sync with the external clock rising edge.

When using the internal oscillator, the SYNCO pin provides a 5V clock that can be used to sync other regulators. Therefore, one PI33XX can act as the lead regulator and have additional PI33XXs running in parallel and interleaved.

Output Voltage Trimming

The PI33XX output voltage can be trimmed up from the preset output by connecting a resistor from ADJ pin to SGND and can be trimmed down by connecting a resistor from ADJ pin to VOUT. The Table 2 defines the voltage ranges for the PI33XX family.

Device	Output Voltage	
	Set	Range
PI3311-X0-LGIZ	1.0V	1.00 to 1.4
PI3312-X0-LGIZ	2.5V	2.0 to 3.1
PI3301-X0-LGIZ	3.3V	2.3 to 4.1
PI3302-X0-LGIZ	5.0V	3.3 to 6.5
PI3303-X0-LGIZ	12V	6.5 to 13.0
PI3305-X0-LGIZ	15V	10.0 to 16.0

Table 2 - *PI33XX family output voltage ranges. Additional versions available for output voltages (Vout) of 1.5 to 1.9V and Vout >15V.*

Soft-Start

The PI33XX includes an internal soft-start capacitor to ramp the output voltage in 2ms from 0V to full output voltage. Connecting an external capacitor from the TRK pin to SGND will increase the start-up ramp period. See, "Soft Start Adjustment and Track," in the Applications Description section for more details.

Remote Sensing

An internal 100Ω resistor is connected between REM pin and VOUT pin to provide regulation when the REM is left open. With REM open, the converter will regulate 100mV above its set point. Connect REM to the desired reference node to be regulated**.**

Output Current Limit Protection

PI33XX has two methods implemented to protect from output short or over current condition.

Slow Current Limit protection: prevents the output load from sourcing current higher than the regulator's maximum rated current. If the output current exceeds the Current Limit (I_{OUT_CL}) for 1024us, a slow current limit fault is initiated and the regulator is shutdown which eliminates output current flow. After Fault Restart Delay (t_{FR_DLY}), a soft-start cycle is initiated. This restart cycle will be repeated indefinitely until the excessive load is removed.

Fast Current Limit protection: PI33XX monitors the regulator inductor current pulse-by-pulse to prevent the output from supplying very high current due to a sudden low impedance short. If the regulator senses a high inductor current pulse, it will initiate a fault and stop switching until Fault Restart Delay ends and then initiate a soft-start cycle.

Both the Fast and Slow current limit faults are stored in a Fault Register and can be read and cleared (PI33XX-20 and PI33XX-21 versions only) via I^2C data bus.

Input Under-Voltage Lockout

If VIN falls below the input Under Voltage Lockout (UVLO) threshold, but remains high enough to power the internal bias supply, the PI33XX will complete the current cycle and stop switching. If VIN recovers within 128 switching cycles, the PI33XX will resume normal operation. If this time limit is exceeded, the system will enter a low power state and initiate a fault. The system will restart once the input voltage is reestablished and after the Fault Restart Delay. A UVLO fault is stored in a Fault Register and can be read and cleared (PI33XX-20 and PI33XX-21 versions only) via I2C data bus.

Input Over Voltage Lockout

If VIN exceeds the input Over Voltage Lockout (OVLO) threshold (V_{OVLO}), while the controller is running, the PI33XX will complete the current cycle and stop switching. If VIN recovers within 128 switching cycles, the PI33XX will resume normal operation. Otherwise, the system will enter a low power state and sets an OVLO fault. The system will resume operation when the input voltage falls below 98% of the OVLO threshold and after the Fault Restart Delay. The OVLO fault is stored in a Fault Register and can be read and cleared (PI33XX-20 and PI33XX-21 versions only) via I^2C data bus.

Output Over Voltage Protection

The PI33XX family is equipped with output Over Voltage Protection (OVP) to prevent damage to input voltage sensitive devices. If the output voltage exceeds 20% of its set regulated value, the regulator will complete the current cycle, stop switching and issue an OVP fault. The system will resume operation once the output voltage falls below the OVP threshold and after Fault Restart Delay. The OVP fault is stored in a Fault Register and can be read and cleared (PI33XX-20 and PI33XX-21 versions only) via I^2C data bus.

Over Temperature Protection

The internal package temperature is monitored to prevent system components from reaching their thermal maximum. If the Over Temperature Protection Threshold (OTP) is exceeded (V_{OTP}), the regulator will complete the current switching cycle, enter a low power mode, set a fault flag, and will soft-start when the internal temperature falls below Over-Temperature Restart Hysteresis (V_{OTP_HYS}). The OTP fault is stored in a Fault Register and can be read and cleared (PI33XX-20 and PI33XX-21 versions only) via I2C data bus.

Pulse Skip Mode (PSM)

PI33XX features a PSM to achieve high efficiency at light loads. The regulators are setup to skip pulses if EAO falls below a PSM threshold. Depending on conditions and component values, this may result in single pulses or several consecutive pulses followed by skipped pulses. Skipping cycles significantly reduces gate drive power and improves light load efficiency. The regulator will leave PSM once the EAO rises above the Skip Mode threshold.

Variable Frequency Operation

Each PI33XX is preprogrammed to a base operating frequency, with respect to the power stage inductor (see Table 5), to operate at peak efficiency across line and load variations. At low line and high load applications, the base frequency will stretch to accommodate these extreme operating ranges. By stretching the frequency, the ZVS operation is preserved throughout the total input line voltage range therefore maintaining optimum efficiency.

Parallel Operation

Paralleling multiple PI33XX modules can be used to increase the output current capability of a single power rail and reduce output voltage ripple.

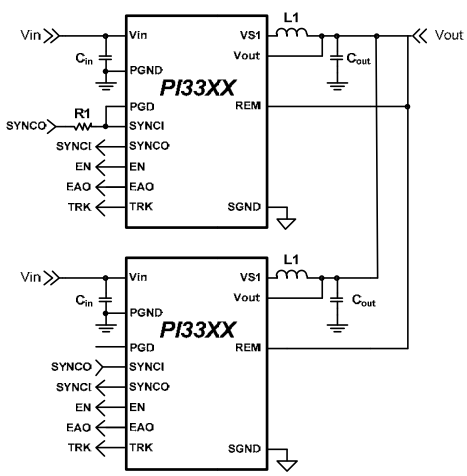


***Figure 3** - PI33XX parallel operation*

By connecting the EAO pins and SGND pins of each module together the units will share the current equally. When the TRK pins of each unit are connected together, the units will track each other during soft-start and all unit EN pins have to be released to allow the units to start (See Figure 3). Also, any fault event in any regulator will disable the other regulators. The two regulators will be out of phase with each other reducing output ripple (refer to Switching Frequency Synchronization).

To provide synchronization between regulators over the entire operational frequency range, the Parallel Good (PGD) pin must be connected to the lead regulator's SYNCI pin and a 2.5kΩ Resistor, R1, must be placed between SYNCO return and the lead regulator's SYNCI pin, as shown in Figure 3. In this configuration, at system soft-start, the PGD pin pulls SYNCI low forcing the lead regulator to initialize the open-loop startup synchronization. Once the regulators reach regulation, SYNCI is released and the system is now synchronized in a closed-loop configuration which allows the system to adjust, on the fly, when any of the individual regulators begin to enter variable frequency mode in the loop.

Multi-phasing three regulators is possible (PI33XX-20 and PI33XX-21 only) with no change to the basic single-phase design. For more information about how to program phase delays within the regulator, please refer to Picor application note *PI33XX-2X Multi-Phase Design Procedure.*

I^{2}C Bus (PI33XX-20 and PI33XX-21 only)

PI33XX-20 and PI33XX-21 provide an I^{2}C digital interface that enables the user to program the EN pin polarity (from high to low assertion) and switching frequency synchronization phase/delay. These are one time programmable options to the device.

Also, the PI33XX-20 and PI33XX-21 allow for dynamic Vout margining via I^{2}C that is useful during development (settings stored in volatile memory only and not retained by the device). The PI33XX-20 and PI33XX-21 also have the option for extended fault telemetry:

Fault registry list:

- Over temperature protection
- Fast/Slow current limit
- Output voltage high
- Input overvoltage
- Input undervoltage

For more information about how to utilize the I^2C interface please refer to Picor application note *PI33XX-2X I^2C Interface Guide.*

Application Description

Output Voltage Programming

The PI33XX family of Buck Regulators provides six common output voltages: 1.0V, 2.5V, 3.3V, 5.0V, 12V and 15V. A post-package trim step is implemented to offset any resistor divider network errors ensuring maximum output accuracy. With a single resistor connected from the ADJ pin to SGND or REM, each device's output can be varied above or below the nominal set voltage (with the exception of the PI3311-X0 which can only be above the set voltage of 1V).

Device	Output Voltage	
	Set	Range
PI3311-X0-LGIZ	1.0V	1.00 to 1.4
PI3312-X0-LGIZ	2.5V	2.0 to 3.1
PI3301-X0-LGIZ	3.3V	2.3 to 4.1
PI3302-X0-LGIZ	5.0V	3.3 to 6.5
PI3303-X0-LGIZ	12V	6.5 to 13.0
PI3305-X0-LGIZ	15V	10.0 to 16.0

***Table 3** - PI33XX family output voltage ranges*

The remote pin (REM) should always be connected to the VOUT pin, if not used, to prevent an output voltage offset. Figure 4 shows the internal feedback voltage divider network.

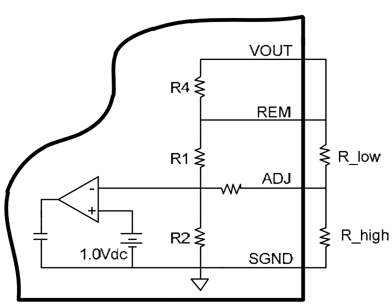


***Figure 4** - Internal resistor divider network*

R1, R2, R3 and R4 are all internal 1.0 % resistors and R_low and R_high are external resistors for which the designer can add to modify VOUT to a desired output. The internal resistor value for each regulator is listed below in Table 4.

Device	R1	R2	R3	R4
PI3311-X0-LGIZ	1k	Open	0	100
PI3312-X0-LGIZ	1.5k	1.0k	2.0k	100
PI3301-X0-LGIZ	2.61k	1.13k	3.0k	100
PI3302-X0-LGIZ	4.53k	1.13k	3.0k	100
PI3303-X0-LGIZ	11.0k	1.0k	3.0k	100
PI3305-X0-LGIZ	14.0k	1.0k	3.0k	100

***Table 4** - PI33XX Internal divider values*

By choosing an output voltage value within the ranges stated in Table 3, VOUT can simply be adjusted up or down by selecting the proper R_high or R_low value, respectively. The following equations can be used to calculate R_high and R_low values:

$$R_{high} = \frac{1}{\frac{(Vout-1)}{R1} - \left(\frac{1}{R2}\right)} - R3 \ \ and \qquad (1)$$

$$R_{low} = \frac{1}{\frac{1}{R2(Vout-1)} - \left(\frac{1}{R1}\right)} - R3. \qquad (2)$$

If, for example, a 6.0V output is needed, the user should choose the proper regulator from Table 3. For this example, we will select the PI3302 (5.0V) and use Equation (1) to calculate R_high to increase the PI3302's output. From Table 4, the resistor-divider network values for the PI3302 are: R1=4.53Ωk, R2=1.13kΩ, and R3 = 3.0kΩ. Inserting these values in to Equation (1), R_high is calculated as follows:

$$1.57k = \frac{1}{\frac{(6.0-1)}{4.53k} - \left(\frac{1}{1.13k}\right)} - 3.0k.$$

The value calculated is ideal and may not be available for purchase; therefore, select a standard

1% value close to the value calculated. A 1.56kΩ, 1%, resistor is a standard value. Check your results by using the voltage divider equation.

Soft-Start Adjust and Tracking

The TRK pin offers a means to increase the regulator's soft-start time or to track with additional regulators. The soft-start slope is controlled by an internal 100nF and a fixed charge current to provide a minimum startup time of 2ms (typical) for all PI33XX regulators. By adding an additional external capacitor to the TRK pin, the soft-start time can be increased further. The following equation can be used to calculate the proper capacitor for a desired soft-start times:

$$C_{TRK} = (t_{TRK} \times I_{TRK}) - 100x10^{-9},$$

Where, t_{TRK} is the soft-start time and I_{TRK} is a 50uA internal charge current (see Electrical Characteristics for limits).

There is typically either proportional or direct tracking implemented within a design. For proportional tracking between several regulators at startup, simply connect all devices TRK pins together. This type of tracking will force all connected regulators to startup and reach regulation at the same time (see Figure 5 (a)).

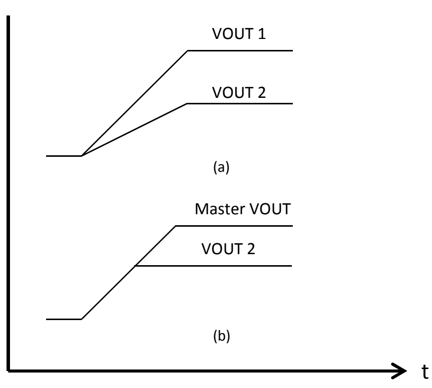


Figure 5 - *PI33XX tracking methods*

For Direct Tracking, choose the regulator with the highest output voltage as the master and connect the master to the TRK pin of the other regulators through a divider (Figure 6) with the same ratio as the slave's feedback divider (see Table 4 for values).

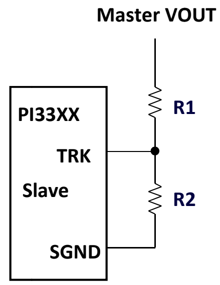


Figure 6 - *Voltage divider connections for direct tracking*

All connected regulators' soft-start slopes will track with this method. Direct tracking timing is demonstrated in Figure 5 (b). All tracking regulators should have their Enable (EN) pins connected together to work properly.

Inductor Pairing

The PI33XX utilizes an external inductor. This inductor has been optimized for maximum efficiency performance. Table 5 details the specific inductor value and part number utilized for each PI33XX device and are manufactured by Cooper Bussman Coiltronics.

Device	Inductor [nH]	Inductor Part Number
PI3311-X0-LGIZ	120	TBD-120-R
PI3312-X0-LGIZ	200	FPT705-200-R
PI3301-X0-LGIZ	200	FPT705-200-R
PI3302-X0-LGIZ	200	FPT705-200-R
PI3303-X0-LGIZ	230	FPT705-230-R
PI3305-X0-LGIZ	230	FPT705-230-R

Table 5 - *PI33XX Inductor pairing*

Input and Output Filter Considerations

The PI33XX requires input bulk storage capacitance as well as low impedance ceramic X5R input capacitors to ensure proper start up and high frequency decoupling for the power stage. The PI33XX will draw nearly all of the high frequency current from the low impedance ceramic capacitors when the main high side MOSFET is conducting. During the time the high side MOSFET is off, they are replenished from the bulk capacitor. If the input impedance is high at the switching frequency of the converter, the bulk capacitor must supply all of the average current into the converter, including replenishing the ceramic capacitors. This value has been chosen to be 100µF so that the PI33XX can start up into a full resistive load and supply the output capacitive load with the default minimum soft start capacitor when the input source impedance is 50 Ohms at 1MHz. The ESR for this capacitor should be approximately 20mΩ. The RMS ripple current in this capacitor is small, so it should not be a concern if the input recommended ceramic capacitors are used. Table 6 shows the recommended input and output capacitors to be used for the various models as well as expected transient response, RMS ripple currents per capacitor, and input and output ripple voltages. Table 7 includes the recommended input and output ceramic capacitors.

Device	V_{IN} (V)	I_{LOAD} (A)	C_{INPUT} Bulk Elec.	C_{INPUT} Ceramic X5R	C_{OUTPUT} Ceramic X5R	C_{INPUT} Ripple Current (I_{RMS})	C_{OUTPUT} Ripple Current (I_{RMS})	Input Ripple (mVpp)	Output Ripple (mVpp)	Transient Deviation (mVpk)	Recovery Time (µs)	Load Step (A) (Slew/µs)
PI3311	24	10	100µF 50V	4X4.7µF 50V	8X100µF 2X1 µF 1X0.1 µF	0.5	0.8	120	20	-/+40	40	5 (5A/µs)
		5						100	15			
PI3312	24	10	100µF 50V	4X4.7µF	4X100µF 2X1 µF 1X0.1 µF	1	1.75	150	50	-/+80	25	5 (10A/µs)
		5						100	24			
PI3301	24	10	100µF 50V	4X4.7µF	4X100µF 2X1 µF 1X0.1 µF	1.05	1.625	200	40	-/+100	20	5 (10A/µs)
		5						125	33			
PI3302	24	10	100µF 50V	4X4.7µF	4X100µF 2X1 µF 1X0.1 µF	1.2	1.5	220	50	-/+170	30	5 (5A/µs)
		5						140	30			
PI3303	24	8	100µF 50V	4X4.7µF	4X22µF 2X1 µF 1X0.1 µF	1.3	1.36	275	100	-/+300	30	4 (10A/µs)
		4						150	60			
PI3305	24	8	100µF 50V	4X4.7µF	4X22µF 2X1 µF 1X0.1 µF	1.38	1.2	280	150	-/+400	30	4 (10A/µs)
		4						160	75			

Table 6 *- Recommended input and output capacitance*

MURATA PART NUMBER	DESCRIPTION	MURATA PART NUMBER	DESCRIPTION
GRM188R71C105KA12D	1uF 16V 0603 X7R	GRM31CR71H475KA12K	4.7uF 50V 1206 X7R
GRM319R71H104KA01D	0.1uF 50V 1206 X7R	GRM31CR61A476ME15L	47uF 10V 1206 X5R
GRM31CR60J107ME39L	100uF 6.3V 1206 X5R	GRM31CR61E226KE15L	22uF 25V 1206 X5R

Table 7 *- Capacitor manufacturer part numbers*

Layout Guidelines

To optimize maximum efficiency and a low noise performance from a PI33XX design, layout considerations are necessary. Reducing trace resistance and minimizing high current loop returns along with proper component placement will reduce parasitic resistance and inductance.

A typical buck converter circuit is shown in Figure 9. The potential areas of high parasitic inductance and resistance are the circuit return paths, shown as LR below.

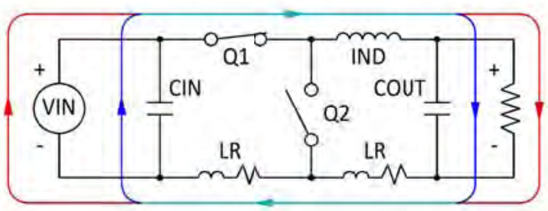


Figure 9 - *Typical Buck Converter*

The path between the COUT and CIN capacitors is of particular importance since the AC currents are flowing through both of them when Q1 is turned on. Figure 10, schematically, shows the reduced trace length between input and output capacitors. The shorter path lessens the effects that copper trace parasitics can have on the PI33XX performance.

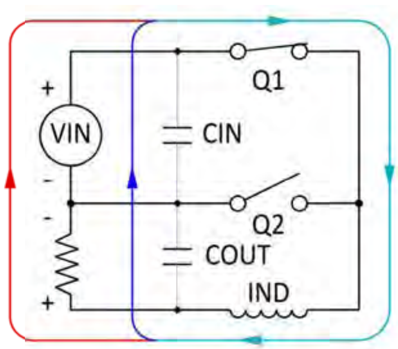


Figure 10 *- Current flow: Q1 closed*

When Q1 is on and Q2 is off, the majority of CIN's current is used to satisfy the static output load and to recharge the COUT capacitors. When Q1 is off and Q2 is on, the load current is supplied by the inductor and the COUT capacitor. During this period CIN is also being recharged by the VIN. Low CIN loop inductance is important to minimize peak voltage when Q1 turns off. Also, the difference in area between the CIN loop and COUT loop is vital to minimize switching and GND noise.

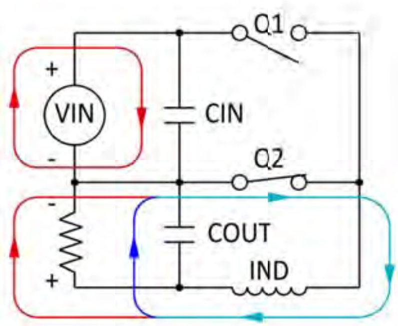


Figure 11 - *Current flow: Q2 closed*

The recommended component placement, shown in Figure 11, illustrates the tight path between CIN and COUT (and VIN and VOUT) for the high AC return current. This optimized layout is the same that is used on the PI33XX evaluation board.

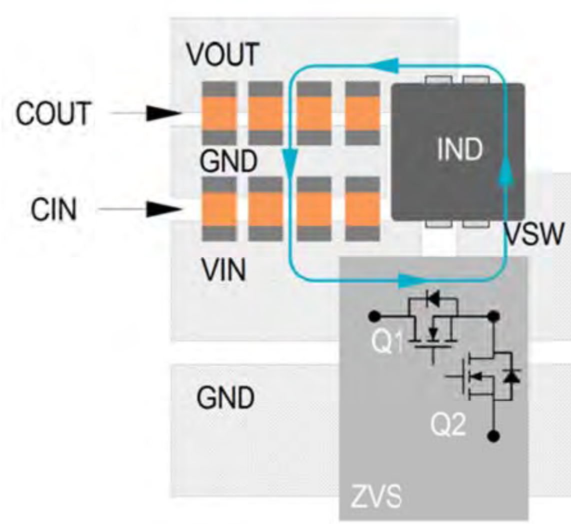


Figure 12 - *Recommended component placement and metal routing*

Recommended PCB Footprint and Stencil

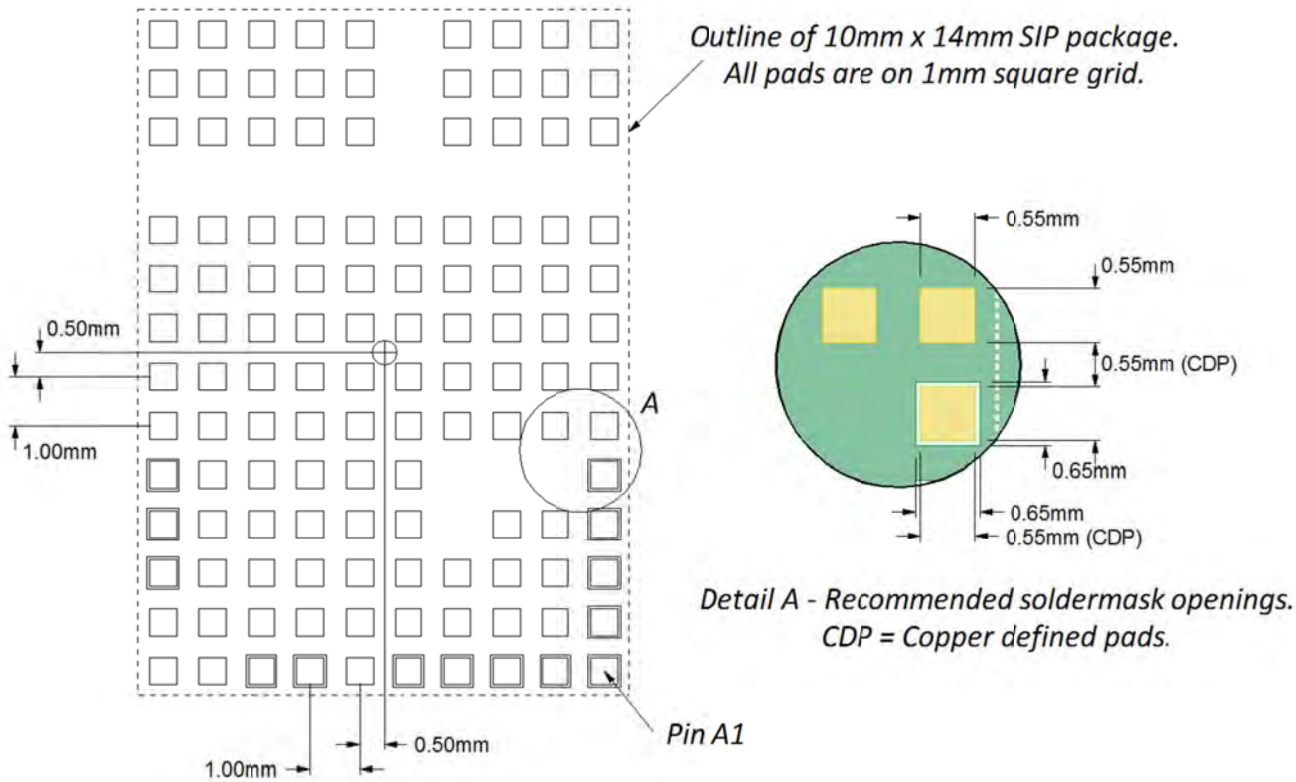
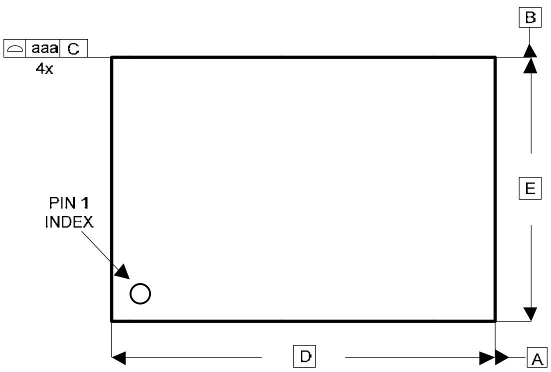


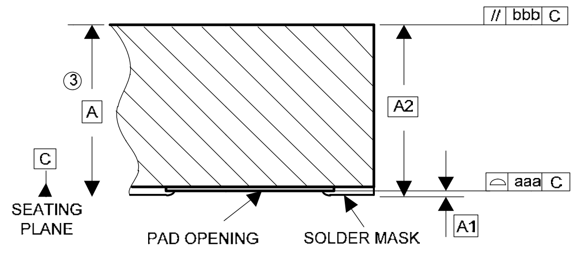
Figure 13 - *Recommended Receiving PCB footprint.*

Figure 133 details the recommended receiving footprint for PI33XX 10mm x 14mm package. All pads should have a final copper size of 0.55mm x 0.55mm, whether they are solder-mask defined or copper defined, on a 1mm x 1mm grid. All stencil openings are 0.55mm when using a 6mil stencil.

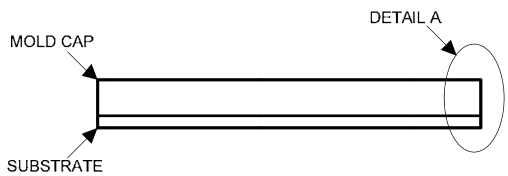
Package Drawings



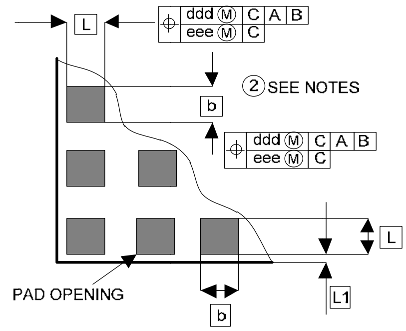
PACKAGE TOP VIEW



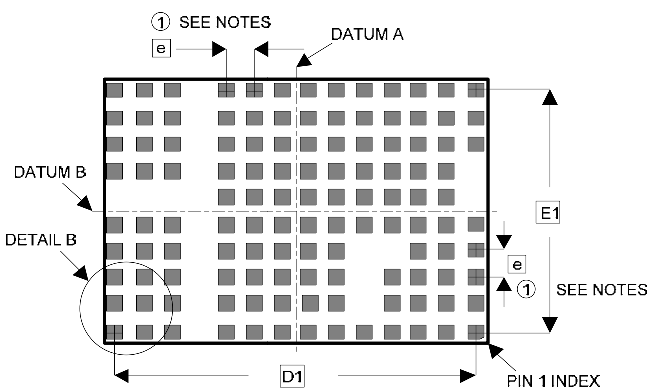
DETAIL A



PACKAGE SIDE VIEW



DETAIL B



PACKAGE BOTTOM VIEW

NOTES

① 'e' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS.

② DIMENSION 'b' APPLIES TO METALLIZED PAD OPENING.

③ DIMENSION 'A' INCLUDES PACKAGE WARPAGE.

④ EXPOSED METALLIZED PADS ARE CU PADS WITH SURFACE FINISH PROTECTION.

5 ALL DIMENSIONS IN MILLIMETERS.

SYMBOL	MIN	NOM	MAX
A	2.50	2.56	2.62
A1	--	--	0.05
A2	--	--	2.57
b	0.50	0.55	0.60
L	0.50	0.55	0,60
D	14.00 BSC		
E	10.00 BSC		
D1	13.00 BSC		
E1	9.00 BSC		
e	1.00 BSC		
L1	0.10	0.15	0.20
aaa			0.10
bbb			0.10
ccc			0.08
ddd			0.10
eee			0.08

DIMENSIONS

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